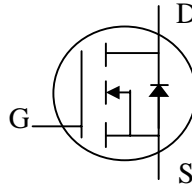


N-CHANNEL ENHANCEMENT-MODE POWER MOSFET

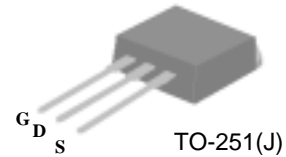
Low on-resistance
 Capable of 2.5V gate drive
 Low drive current
 Simple drive requirement



BV_{DSS} 18V
 $R_{DS(ON)}$ 25m Ω
 I_D 35A

Description

Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.



Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|-------------------------------|--|------------|---------------------|
| V_{DS} | Drain-Source Voltage | 18 | V |
| V_{GS} | Gate-Source Voltage | ± 12 | V |
| $I_D @ T_C=25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 4.5\text{V}$ | 35 | A |
| $I_D @ T_C=125^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 4.5\text{V}$ | 16 | A |
| I_{DM} | Pulsed Drain Current ¹ | 90 | A |
| $P_D @ T_C=25^\circ\text{C}$ | Total Power Dissipation | 50 | W |
| | Linear Derating Factor | 0.4 | W/ $^\circ\text{C}$ |
| T_{STG} | Storage Temperature Range | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating Junction Temperature Range | -55 to 150 | $^\circ\text{C}$ |

Thermal Data

| Symbol | Parameter | Value | Unit |
|--------|-------------------------------------|----------|---------------------------|
| Rthj-c | Thermal Resistance Junction-case | Max. 2.5 | $^\circ\text{C}/\text{W}$ |
| Rthj-a | Thermal Resistance Junction-ambient | Max. 110 | $^\circ\text{C}/\text{W}$ |

Electrical Characteristics @ T_j=25°C (unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|-------------------------------------|--|--|------|------|------|-------|
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V, I _D =250uA | 18 | - | - | V |
| ΔBV _{DSS} /ΔT _j | Breakdown Voltage Temperature Coefficient | Reference to 25°C, I _D =1mA | - | 0.03 | - | V/°C |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =4.5V, I _D =6A | - | - | 25 | mΩ |
| | | V _{GS} =2.5V, I _D =5.2A | - | - | 40 | mΩ |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250uA | 0.5 | - | 1 | V |
| g _{fs} | Forward Transconductance | V _{DS} =10V, I _D =6A | - | 18 | - | S |
| I _{DSS} | Drain-Source Leakage Current (T _j =25°C) | V _{DS} =18V, V _{GS} =0V | - | - | 1 | uA |
| | Drain-Source Leakage Current (T _j =125°C) | V _{DS} =18V, V _{GS} =0V | - | - | 25 | uA |
| I _{GSS} | Gate-Source Leakage | V _{GS} = ± 12V | - | - | ±100 | nA |
| Q _g | Total Gate Charge ² | I _D =18A | - | 17.5 | - | nC |
| Q _{gs} | Gate-Source Charge | V _{DS} =18V | - | 1.2 | - | nC |
| Q _{gd} | Gate-Drain ("Miller") Charge | V _{GS} =5V | - | 7.9 | - | nC |
| t _{d(on)} | Turn-on Delay Time ² | V _{DS} =10V | - | 7.3 | - | ns |
| t _r | Rise Time | I _D =18A | - | 98 | - | ns |
| t _{d(off)} | Turn-off Delay Time | R _G =3.3 Ω, V _{GS} =5V | - | 25.6 | - | ns |
| t _f | Fall Time | R _D =0.56Ω | - | 98 | - | ns |
| C _{iss} | Input Capacitance | V _{GS} =0V | - | 527 | - | pF |
| C _{oss} | Output Capacitance | V _{DS} =18V | - | 258 | - | pF |
| C _{riss} | Reverse Transfer Capacitance | f=1.0MHz | - | 112 | - | pF |

Source-Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|-----------------|---|--|------|------|------|-------|
| I _S | Continuous Source Current (Body Diode) | V _D =V _G =0V, V _S =1.3V | - | - | 35 | A |
| I _{SM} | Pulsed Source Current (Body Diode) ¹ | | - | - | 90 | A |
| V _{SD} | Forward On Voltage ² | T _j =25°C, I _S =35A, V _{GS} =0V | - | - | 1.3 | V |

Notes:

- 1.Pulse width limited by safe operating area.
- 2.Pulse width ≤300us, duty cycle ≤2%.

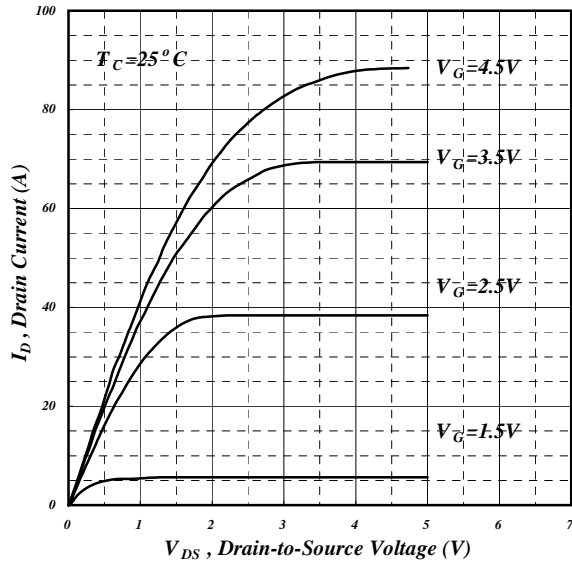


Fig 1. Typical Output Characteristics

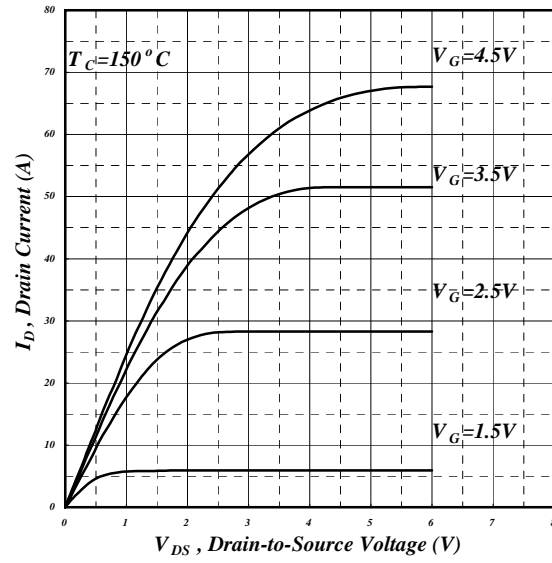


Fig 2. Typical Output Characteristics

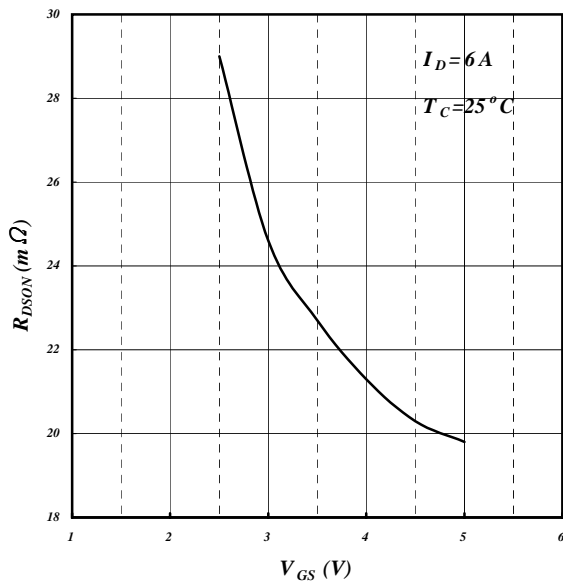


Fig 3. On-Resistance vs. Gate Voltage

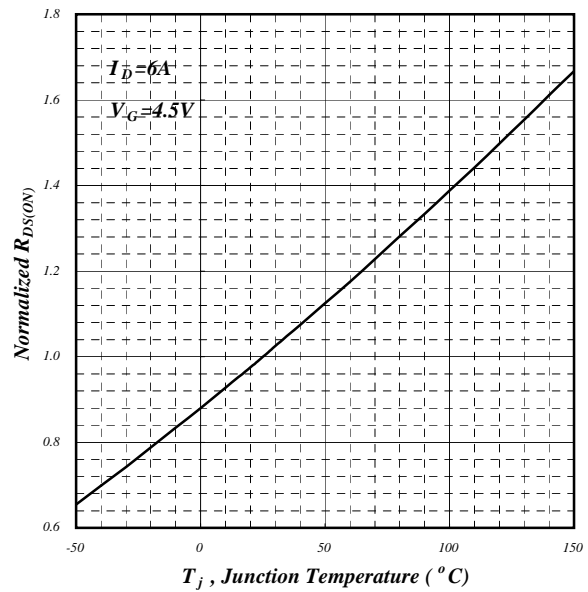


Fig 4. Normalized On-Resistance vs. Junction Temperature

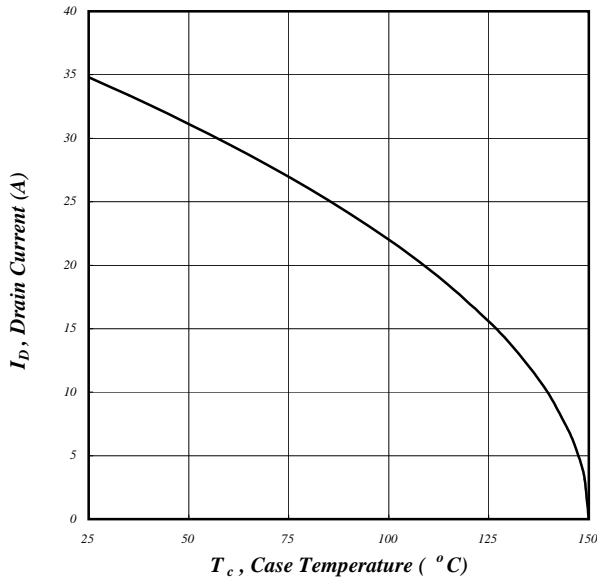


Fig 5. Maximum Drain Current vs. Case Temperature

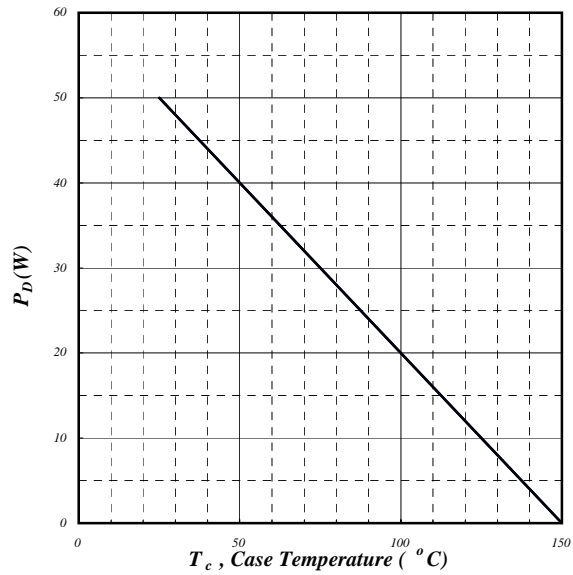


Fig 6. Typical Power Dissipation

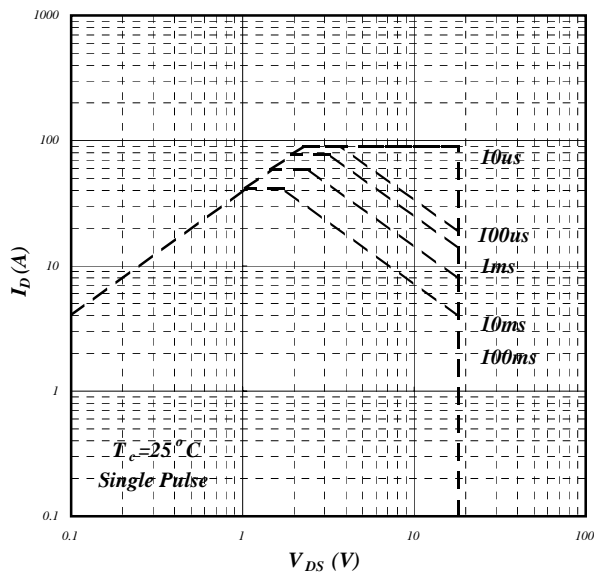


Fig 7. Maximum Safe Operating Area

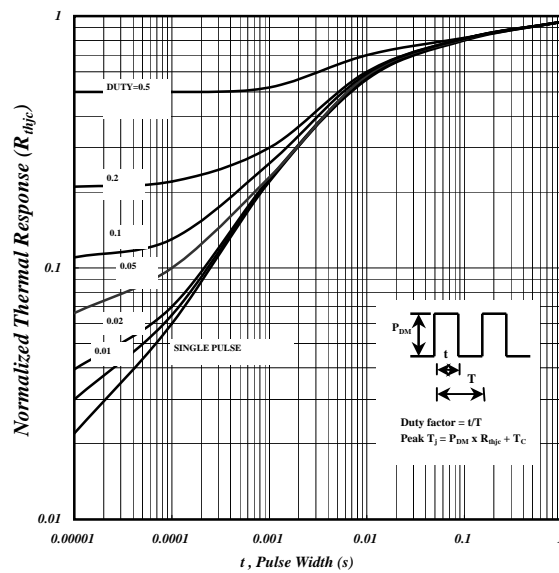


Fig 8. Effective Transient Thermal Impedance

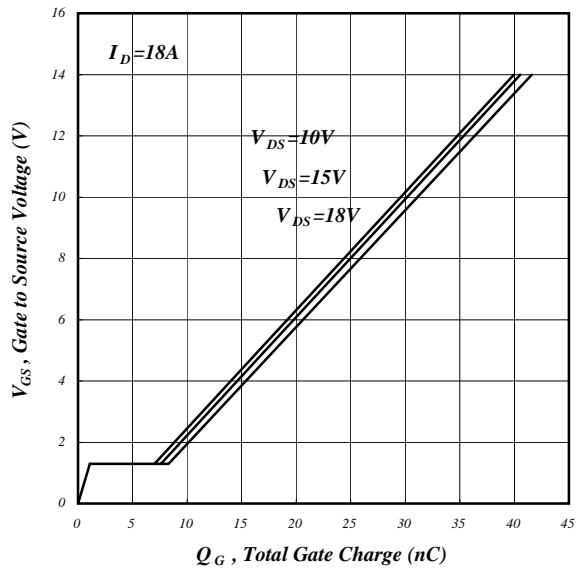


Fig 9. Gate Charge Characteristics

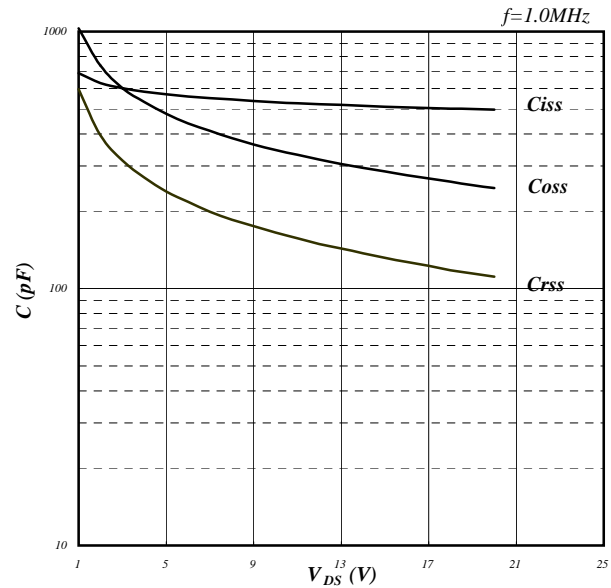


Fig 10. Typical Capacitance Characteristics

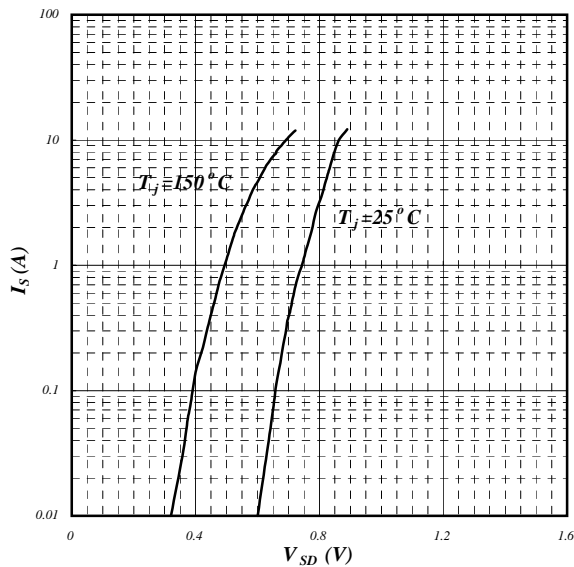


Fig 11. Forward Characteristic of Reverse Diode

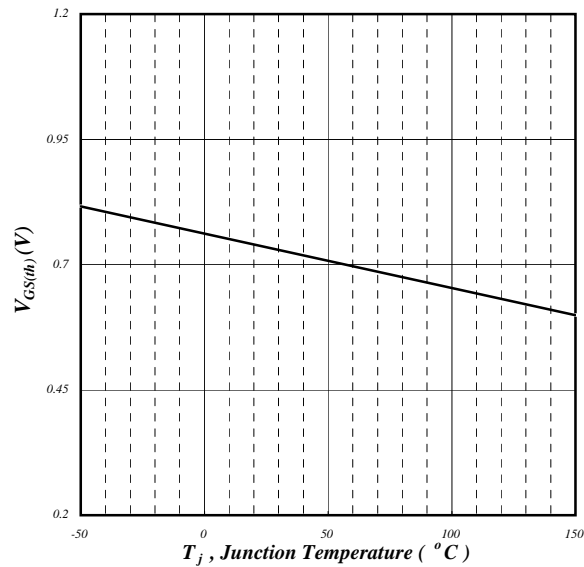


Fig 12. Gate Threshold Voltage vs. Junction Temperature

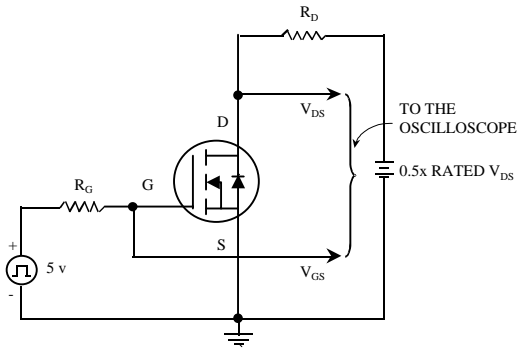


Fig 13. Switching Time Circuit

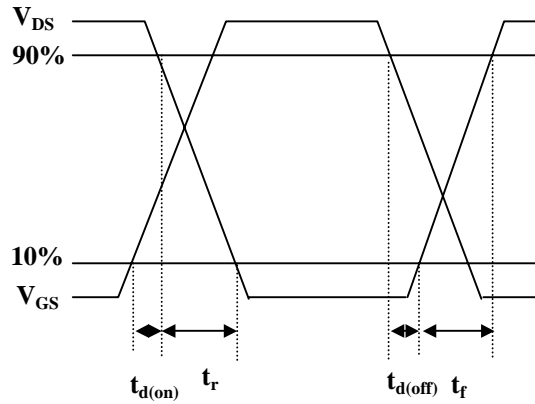


Fig 14. Switching Time Waveform

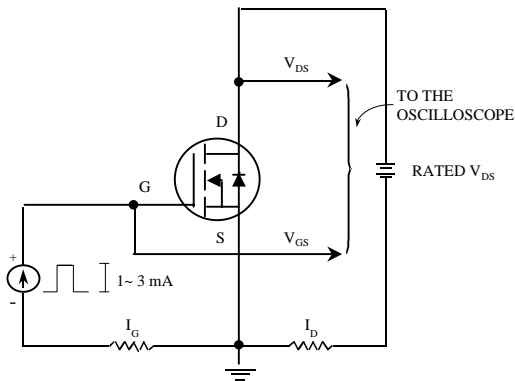


Fig 15. Gate Charge Circuit

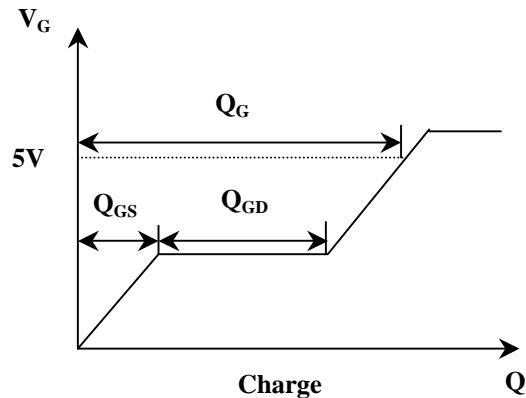


Fig 16. Gate Charge Waveform

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, express or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.