SSD1788

Advance Information

98 RGB x 68 CSTN
LCD Segment / Common COLOR Driver with Controller

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1 General Description

SSD1788 is a single-chip CMOS color STN LCD driver with controller for dot-matrix graphic liquid crystal display system. SSD1788 consists of 362 high voltage driving output pins for driving maximum 98 RGB Segments and 68 Commons.

SSD1788 consists of 294 (98 RGB) x 68 x 4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from common MCU through 8-bit 6800-series / 8080-series compatible Parallel Interface or 3-wires / 4-wires Serial Peripheral Interface by pins selection.

SSD1788 embeds DC-DC Converter, On-Chip Oscillator and Bias Divider so as to reduce the number of external components. With the advanced design, low power consumption, stable LCD operating voltage and flexible die package layout, SSD1788 is suitable for any portable battery-driven applications requiring long operation period with compact size.

2 FEATURES

- Power Supply: V_{DD} = 2.4 V – 3.6V
  V_{DDIO} = 1.2 V – 3.6V
  V_{CI} = 2.4V – 3.6V
- LCD Driving Output Voltage: 13.5V
- Low Current Sleep Mode
- Maximum display size: 98 RGB columns by 68 rows.
- Maximum display colors: 256 colors or 4096 colors graphical display
- 256-colors Position Control and simultaneous RGB display control
- 8-bit 6800-series / 8080-series Parallel Interface, 3-wires /4-wires Serial Peripheral Interface
- On-Chip 294 (98 RGB) X 68 x 4 = 79,968 bits Graphic Display Data RAM
- Programmable partial display function
- Column Re-mapping and RAM Page scan direction control
- Software selection on Center Screen Scrolling, Top Screen Scrolling, Bottom Screen Scrolling and Whole Screen Scrolling
- On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
- 3X/ 4X / 5X / 6X On-Chip DC-DC Converter with internal flying capacitor
- 64 Levels Internal Contrast Control
- Programmable LCD Driving Voltage Temperature Compensation Coefficients
- On-Chip Bias Divider with internal flying capacitor (expect V_{OUT})
- Programmable drive duty ratio: 1 /8 to 1 /68
- On-Chip Oscillator
- 2-D Graphic Acceleration Engine
- Non-Volatile Memory (OTP) for calibration

3 ORDERING INFORMATION

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1788Z	98x3 (294)	68	Gold Bump Die	Figure 2 on Page 7	

Table 1 - Ordering Information

4 BLOCK DIAGRAM

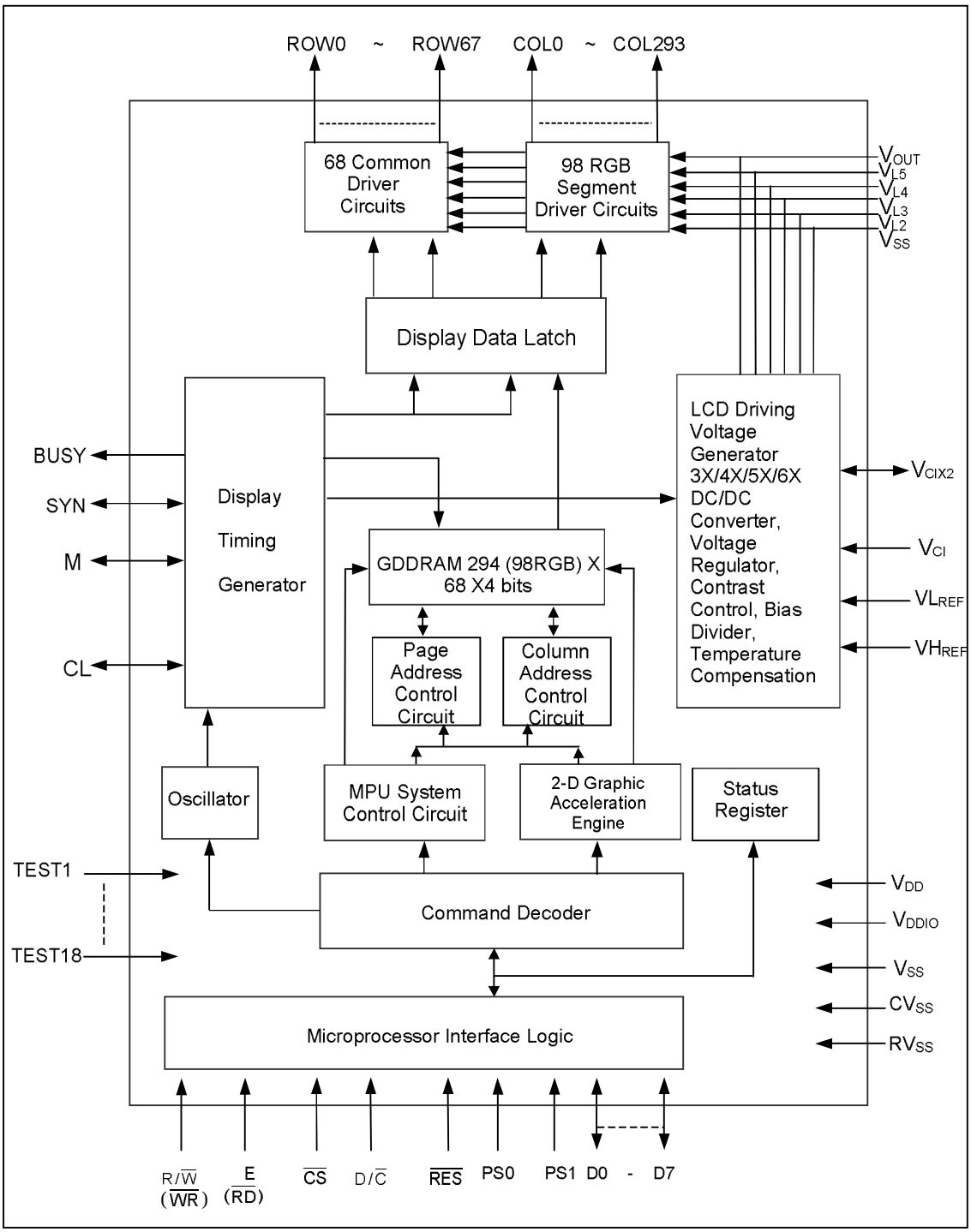
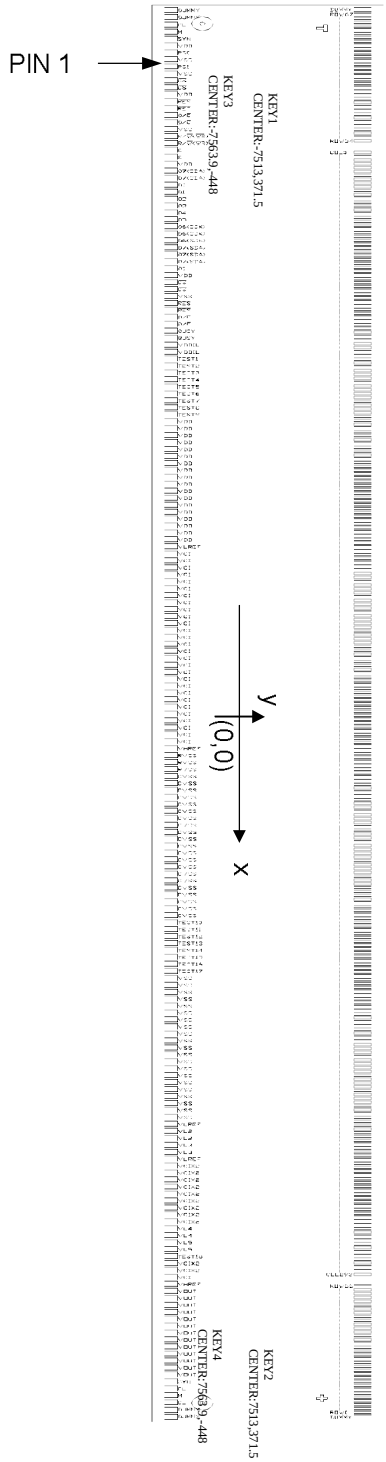
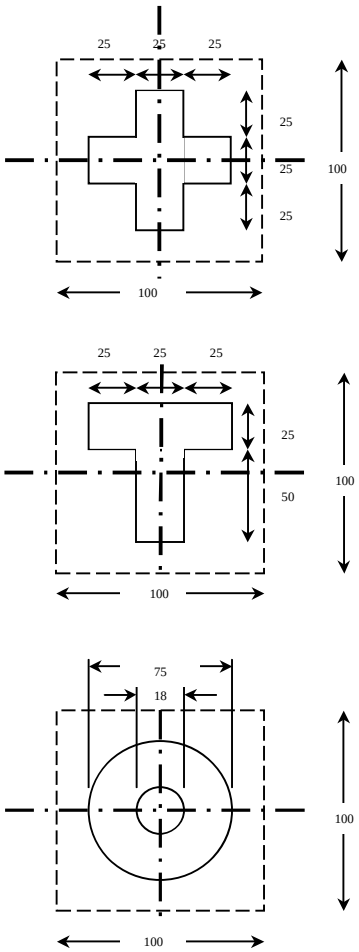


Figure 1 - SSD1788 Block Diagram

5 DIE PAD FLOOR PLAN



Note:
1. Diagram showing the die face up.
2. Coordinates are reference to center of the chip.
3. Unit of coordinates and Size of all alignment marks are in um.
4. All alignment keys do not contain gold bump.



Die Size	15.68 x 1.65	mm^2
Die Thickness	457±25	µm
Typical Bump Height	15	µm
Bump Co-planarity (within die)	<3	µm

Figure 2 - SSD1788 Die Pad Floor Plan

Table 2 - SSD1788 Series Bump Die Pad Coordinates (Bump center)

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1	DUMMY	-7714.5	-663	51	TEST1	-3891.3	-663	101	V_{CI}	-76.3	-663
2	DUMMY	-7638.2	-663	52	TEST2	-3815	-663	102	V_{CI}	0	-663
3	CL	-7553.7	-663	53	TEST3	-3738.7	-663	103	V_{CI}	76.3	-663
4	M	-7477.4	-663	54	TEST4	-3662.4	-663	104	V_{CI}	152.6	-663
5	SYN	-7401.1	-663	55	TEST5	-3586.1	-663	105	V_{CI}	228.9	-663
6	V_{DD}	-7324.8	-663	56	TEST6	-3509.8	-663	106	V_{CI}	305.2	-663
7	PS0	-7248.5	-663	57	TEST7	-3433.5	-663	107	VH_{REF}	381.5	-663
8	V_{SS}	-7172.2	-663	58	TEST8	-3357.2	-663	108	RV_{SS}	457.8	-663
9	PS1	-7095.9	-663	59	TEST9	-3280.9	-663	109	RV_{SS}	534.1	-663
10	V_{SS}	-7019.6	-663	60	V_{DD}	-3204.6	-663	110	RV_{SS}	610.4	-663
11	$\overline{CS}$	-6943.3	-663	61	V_{DD}	-3128.3	-663	111	CV_{SS}	686.7	-663
12	$\overline{CS}$	-6867	-663	62	V_{DD}	-3052	-663	112	CV_{SS}	763	-663
13	V_{DD}	-6790.7	-663	63	V_{DD}	-2975.7	-663	113	CV_{SS}	839.3	-663
14	$\overline{RES}$	-6714.4	-663	64	V_{DD}	-2899.4	-663	114	CV_{SS}	915.6	-663
15	$\overline{RES}$	-6638.1	-663	65	V_{DD}	-2823.1	-663	115	CV_{SS}	991.9	-663
16	D/$\overline{C}$	-6561.8	-663	66	V_{DD}	-2746.8	-663	116	CV_{SS}	1068.2	-663
17	D/$\overline{C}$	-6485.5	-663	67	V_{DD}	-2670.5	-663	117	CV_{SS}	1144.5	-663
18	V_{SS}	-6409.2	-663	68	V_{DD}	-2594.2	-663	118	CV_{SS}	1220.8	-663
19	R/$\overline{W}$ ($\overline{WR}$)	-6332.9	-663	69	V_{DD}	-2517.9	-663	119	CV_{SS}	1297.1	-663
20	R/$\overline{W}$ ($\overline{WR}$)	-6256.6	-663	70	V_{DD}	-2441.6	-663	120	CV_{SS}	1373.4	-663
21	E ($\overline{RD}$)	-6180.3	-663	71	V_{DD}	-2365.3	-663	121	CV_{SS}	1449.7	-663
22	E ($\overline{RD}$)	-6104	-663	72	V_{DD}	-2289	-663	122	CV_{SS}	1526	-663
23	V_{DD}	-6027.7	-663	73	V_{DD}	-2212.7	-663	123	CV_{SS}	1602.3	-663
24	D7 (SDA)	-5951.4	-663	74	V_{DD}	-2136.4	-663	124	CV_{SS}	1678.6	-663
25	D7 (SDA)	-5875.1	-663	75	V_{DD}	-2060.1	-663	125	CV_{SS}	1754.9	-663
26	D0	-5798.8	-663	76	V_{DD}	-1983.8	-663	126	CV_{SS}	1831.2	-663
27	D1	-5722.5	-663	77	V_{DD}	-1907.5	-663	127	CV_{SS}	1907.5	-663
28	D2	-5646.2	-663	78	VL_{REF}	-1831.2	-663	128	CV_{SS}	1983.8	-663
29	D3	-5569.9	-663	79	V_{CI}	-1754.9	-663	129	CV_{SS}	2060.1	-663
30	D4	-5493.6	-663	80	V_{CI}	-1678.6	-663	130	CV_{SS}	2136.4	-663
31	D5	-5417.3	-663	81	V_{CI}	-1602.3	-663	131	CV_{SS}	2212.7	-663
32	D6 (SCK)	-5341	-663	82	V_{CI}	-1526	-663	132	TEST10	2289	-663
33	D6 (SCK)	-5264.7	-663	83	V_{CI}	-1449.7	-663	133	TEST11	2365.3	-663
34	D6 (SCK)	-5188.4	-663	84	V_{CI}	-1373.4	-663	134	TEST12	2441.6	-663
35	D7 (SDA)	-5112.1	-663	85	V_{CI}	-1297.1	-663	135	TEST13	2517.9	-663
36	D7 (SDA)	-5035.8	-663	86	V_{CI}	-1220.8	-663	136	TEST14	2594.2	-663
37	D7 (SDA)	-4959.5	-663	87	V_{CI}	-1144.5	-663	137	TEST15	2670.5	-663
38	D0	-4883.2	-663	88	V_{CI}	-1068.2	-663	138	TEST16	2746.8	-663
39	V_{DD}	-4806.9	-663	89	V_{CI}	-991.9	-663	139	TEST17	2823.1	-663
40	$\overline{CS}$	-4730.6	-663	90	V_{CI}	-915.6	-663	140	V_{SS}	2899.4	-663
41	$\overline{CS}$	-4654.3	-663	91	V_{CI}	-839.3	-663	141	V_{SS}	2975.7	-663
42	V_{SS}	-4578	-663	92	V_{CI}	-763	-663	142	V_{SS}	3052	-663
43	$\overline{RES}$	-4501.7	-663	93	V_{CI}	-686.7	-663	143	V_{SS}	3128.3	-663
44	$\overline{RES}$	-4425.4	-663	94	V_{CI}	-610.4	-663	144	V_{SS}	3204.6	-663
45	D/$\overline{C}$	-4349.1	-663	95	V_{CI}	-534.1	-663	145	V_{SS}	3280.9	-663
46	D/$\overline{C}$	-4272.8	-663	96	V_{CI}	-457.8	-663	146	V_{SS}	3357.2	-663
47	BUSY	-4196.5	-663	97	V_{CI}	-381.5	-663	147	V_{SS}	3433.5	-663
48	BUSY	-4120.2	-663	98	V_{CI}	-305.2	-663	148	V_{SS}	3509.8	-663
49	V_{DDIO}	-4043.9	-663	99	V_{CI}	-228.9	-663	149	V_{SS}	3586.1	-663
50	V_{DDIO}	-3967.6	-663	100	V_{CI}	-152.6	-663	150	V_{SS}	3662.4	-663

Pad #	Signal	X-pos	Y-pos
151	V_{SS}	3738.7	-663
152	V_{SS}	3815	-663
153	V_{SS}	3891.3	-663
154	V_{SS}	3967.6	-663
155	V_{SS}	4043.9	-663
156	V_{SS}	4120.2	-663
157	V_{SS}	4196.5	-663
158	V_{SS}	4272.8	-663
159	V_{SS}	4349.1	-663
160	V_{SS}	4425.4	-663
161	VL_{REF}	4501.7	-663
162	V_{L2}	4578	-663
163	V_{L2}	4654.3	-663
164	V_{L3}	4730.6	-663
165	V_{L3}	4806.9	-663
166	VL_{REF}	4883.2	-663
167	V_{CIX2}	4959.5	-663
168	V_{CIX2}	5035.8	-663
169	V_{CIX2}	5112.1	-663
170	V_{CIX2}	5188.4	-663
171	V_{CIX2}	5264.7	-663
172	V_{CIX2}	5341	-663
173	V_{CIX2}	5417.3	-663
174	V_{CIX2}	5493.6	-663
175	V_{CIX2}	5569.9	-663
176	V_{L4}	5646.2	-663
177	V_{L4}	5722.5	-663
178	V_{L5}	5798.8	-663
179	V_{L5}	5875.1	-663
180	TEST18	5951.4	-663
181	V_{CIX2}	6027.7	-663
182	V_{CIX2}	6104	-663
183	V_{CI}	6180.3	-663
184	VH_{REF}	6256.6	-663
185	V_{OUT}	6332.9	-663
186	V_{OUT}	6409.2	-663
187	V_{OUT}	6485.5	-663
188	V_{OUT}	6561.8	-663
189	V_{OUT}	6638.1	-663
190	V_{OUT}	6714.4	-663
191	V_{OUT}	6790.7	-663
192	V_{OUT}	6867	-663
193	V_{OUT}	6943.3	-663
194	V_{OUT}	7019.6	-663
195	V_{OUT}	7095.9	-663
196	V_{OUT}	7172.2	-663
197	V_{OUT}	7248.5	-663
198	SYN	7324.8	-663
199	CL	7401.1	-663
200	M	7477.4	-663

Pad #	Signal	X-pos	Y-pos
201	CL	7553.7	-663
202	DUMMY	7638.2	-663
203	DUMMY	7714.5	-663
204	DUMMY	7718.5	651
205	ROW0	7665	651
206	ROW1	7623	651
207	ROW2	7581	651
208	ROW3	7539	651
209	ROW4	7497	651
210	ROW5	7455	651
211	ROW6	7413	651
212	ROW7	7371	651
213	ROW8	7329	651
214	ROW9	7287	651
215	ROW10	7245	651
216	ROW11	7203	651
217	ROW12	7161	651
218	ROW13	7119	651
219	ROW14	7077	651
220	ROW15	7035	651
221	ROW16	6993	651
222	ROW17	6951	651
223	ROW18	6909	651
224	ROW19	6867	651
225	ROW20	6825	651
226	ROW21	6783	651
227	ROW22	6741	651
228	ROW23	6699	651
229	ROW24	6657	651
230	ROW25	6615	651
231	ROW26	6573	651
232	ROW27	6531	651
233	ROW28	6489	651
234	ROW29	6447	651
235	ROW30	6405	651
236	ROW31	6363	651
237	ROW32	6321	651
238	ROW33	6279	651

Pad #	Pad Name	Signal	Color	X-pos	Y-pos
239	COL293	SEG97	B	6153	651
240	COL292		G	6111	651
241	COL291		R	6069	651
242	COL290	SEG96	B	6027	651
243	COL289		G	5985	651
244	COL288		R	5943	651
245	COL287	SEG95	B	5901	651
246	COL286		G	5859	651
247	COL285		R	5817	651
248	COL284	SEG94	B	5775	651
249	COL283		G	5733	651
250	COL282		R	5691	651
251	COL281	SEG93	B	5649	651
252	COL280		G	5607	651
253	COL279		R	5565	651
254	COL278	SEG92	B	5523	651
255	COL277		G	5481	651
256	COL276		R	5439	651
257	COL275	SEG91	B	5397	651
258	COL274		G	5355	651
259	COL273		R	5313	651
260	COL272	SEG90	B	5271	651
261	COL271		G	5229	651
262	COL270		R	5187	651
263	COL269	SEG89	B	5145	651
264	COL268		G	5103	651
265	COL267		R	5061	651
266	COL266	SEG88	B	5019	651
267	COL265		G	4977	651
268	COL264		R	4935	651
269	COL263	SEG87	B	4893	651
270	COL262		G	4851	651
271	COL261		R	4809	651
272	COL260	SEG86	B	4767	651
273	COL259		G	4725	651
274	COL258		R	4683	651
275	COL257	SEG85	B	4641	651
276	COL256		G	4599	651
277	COL255		R	4557	651
278	COL254	SEG84	B	4515	651
279	COL253		G	4473	651
280	COL252		R	4431	651
281	COL251	SEG83	B	4389	651
282	COL250		G	4347	651
283	COL249		R	4305	651
284	COL248	SEG82	B	4263	651
285	COL247		G	4221	651
286	COL246		R	4179	651

Pad #	Pad Name	Signal	Color	X-pos	Y-pos	Pad #	Pad Name	Signal	Color	X-pos	Y-pos
287	COL245		B	4137	651	335	COL197		B	2121	651
288	COL244	SEG81	G	4095	651	336	COL196	SEG65	G	2079	651
289	COL243		R	4053	651	337	COL195		R	2037	651
290	COL242		B	4011	651	338	COL194		B	1995	651
291	COL241	SEG80	G	3969	651	339	COL193	SEG64	G	1953	651
292	COL240		R	3927	651	340	COL192		R	1911	651
293	COL239		B	3885	651	341	COL191		B	1869	651
294	COL238	SEG79	G	3843	651	342	COL190	SEG63	G	1827	651
295	COL237		R	3801	651	343	COL189		R	1785	651
296	COL236		B	3759	651	344	COL188		B	1743	651
297	COL235	SEG78	G	3717	651	345	COL187	SEG62	G	1701	651
298	COL234		R	3675	651	346	COL186		R	1659	651
299	COL233		B	3633	651	347	COL185		B	1617	651
300	COL232	SEG77	G	3591	651	348	COL184	SEG61	G	1575	651
301	COL231		R	3549	651	349	COL183		R	1533	651
302	COL230		B	3507	651	350	COL182		B	1491	651
303	COL229	SEG76	G	3465	651	351	COL181	SEG60	G	1449	651
304	COL228		R	3423	651	352	COL180		R	1407	651
305	COL227		B	3381	651	353	COL179		B	1365	651
306	COL226	SEG75	G	3339	651	354	COL178	SEG59	G	1323	651
307	COL225		R	3297	651	355	COL177		R	1281	651
308	COL224		B	3255	651	356	COL176		B	1239	651
309	COL223	SEG74	G	3213	651	357	COL175	SEG58	G	1197	651
310	COL222		R	3171	651	358	COL174		R	1155	651
311	COL221		B	3129	651	359	COL173		B	1113	651
312	COL220	SEG73	G	3087	651	360	COL172	SEG57	G	1071	651
313	COL219		R	3045	651	361	COL171		R	1029	651
314	COL218		B	3003	651	362	COL170		B	987	651
315	COL217	SEG72	G	2961	651	363	COL169	SEG56	G	945	651
316	COL216		R	2919	651	364	COL168		R	903	651
317	COL215		B	2877	651	365	COL167		B	861	651
318	COL214	SEG71	G	2835	651	366	COL166	SEG55	G	819	651
319	COL213		R	2793	651	367	COL165		R	777	651
320	COL212		B	2751	651	368	COL164		B	735	651
321	COL211	SEG70	G	2709	651	369	COL163	SEG54	G	693	651
322	COL210		R	2667	651	370	COL162		R	651	651
323	COL209		B	2625	651	371	COL161		B	609	651
324	COL208	SEG69	G	2583	651	372	COL160	SEG53	G	567	651
325	COL207		R	2541	651	373	COL159		R	525	651
326	COL206		B	2499	651	374	COL158		B	483	651
327	COL205	SEG68	G	2457	651	375	COL157	SEG52	G	441	651
328	COL204		R	2415	651	376	COL156		R	399	651
329	COL203		B	2373	651	377	COL155		B	357	651
330	COL202	SEG67	G	2331	651	378	COL154	SEG51	G	315	651
331	COL201		R	2289	651	379	COL153		R	273	651
332	COL200		B	2247	651	380	COL152		B	231	651
333	COL199	SEG66	G	2205	651	381	COL151	SEG50	G	189	651
334	COL198		R	2163	651	382	COL150		R	147	651

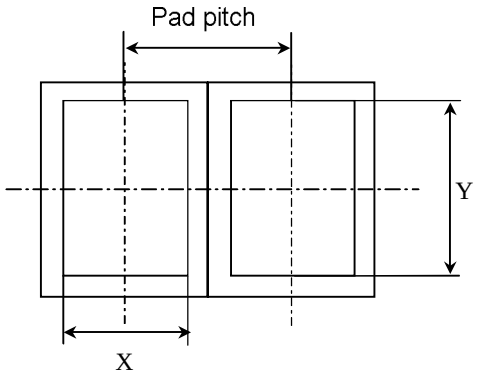
Pad #	Pad Name	Signal	Color	X-pos	Y-pos	Pad #	Pad Name	Signal	Color	X-pos	Y-pos
383	COL149		B	105	651	431	COL101		B	-1911	651
384	COL148	SEG49	G	63	651	432	COL100	SEG33	G	-1953	651
385	COL147		R	21	651	433	COL99		R	-1995	651
386	COL146		B	-21	651	434	COL98		B	-2037	651
387	COL145	SEG48	G	-63	651	435	COL97	SEG32	G	-2079	651
388	COL144		R	-105	651	436	COL96		R	-2121	651
389	COL143		B	-147	651	437	COL95		B	-2163	651
390	COL142	SEG47	G	-189	651	438	COL94	SEG31	G	-2205	651
391	COL141		R	-231	651	439	COL93		R	-2247	651
392	COL140		B	-273	651	440	COL92		B	-2289	651
393	COL139	SEG46	G	-315	651	441	COL91	SEG30	G	-2331	651
394	COL138		R	-357	651	442	COL90		R	-2373	651
395	COL137		B	-399	651	443	COL89		B	-2415	651
396	COL136	SEG45	G	-441	651	444	COL88	SEG29	G	-2457	651
397	COL135		R	-483	651	445	COL87		R	-2499	651
398	COL134		B	-525	651	446	COL86		B	-2541	651
399	COL133	SEG44	G	-567	651	447	COL85	SEG28	G	-2583	651
400	COL132		R	-609	651	448	COL84		R	-2625	651
401	COL131		B	-651	651	449	COL83		B	-2667	651
402	COL130	SEG43	G	-693	651	450	COL82	SEG27	G	-2709	651
403	COL129		R	-735	651	451	COL81		R	-2751	651
404	COL128		B	-777	651	452	COL80		B	-2793	651
405	COL127	SEG42	G	-819	651	453	COL79	SEG26	G	-2835	651
406	COL126		R	-861	651	454	COL78		R	-2877	651
407	COL125		B	-903	651	455	COL77		B	-2919	651
408	COL124	SEG41	G	-945	651	456	COL76	SEG25	G	-2961	651
409	COL123		R	-987	651	457	COL75		R	-3003	651
410	COL122		B	-1029	651	458	COL74		B	-3045	651
411	COL121	SEG40	G	-1071	651	459	COL73	SEG24	G	-3087	651
412	COL120		R	-1113	651	460	COL72		R	-3129	651
413	COL119		B	-1155	651	461	COL71		B	-3171	651
414	COL118	SEG39	G	-1197	651	462	COL70	SEG23	G	-3213	651
415	COL117		R	-1239	651	463	COL69		R	-3255	651
416	COL116		B	-1281	651	464	COL68		B	-3297	651
417	COL115	SEG38	G	-1323	651	465	COL67	SEG22	G	-3339	651
418	COL114		R	-1365	651	466	COL66		R	-3381	651
419	COL113		B	-1407	651	467	COL65		B	-3423	651
420	COL112	SEG37	G	-1449	651	468	COL64	SEG21	G	-3465	651
421	COL111		R	-1491	651	469	COL63		R	-3507	651
422	COL110		B	-1533	651	470	COL62		B	-3549	651
423	COL109	SEG36	G	-1575	651	471	COL61	SEG20	G	-3591	651
424	COL108		R	-1617	651	472	COL60		R	-3633	651
425	COL107		B	-1659	651	473	COL59		B	-3675	651
426	COL106	SEG35	G	-1701	651	474	COL58	SEG19	G	-3717	651
427	COL105		R	-1743	651	475	COL57		R	-3759	651
428	COL104		B	-1785	651	476	COL56		B	-3801	651
429	COL103	SEG34	G	-1827	651	477	COL55	SEG18	G	-3843	651
430	COL102		R	-1869	651	478	COL54		R	-3885	651

Pad #	Pad Name	Signal	Color	X-pos	Y-pos
479	COL53	SEG17	B	-3927	651
480	COL52		G	-3969	651
481	COL51		R	-4011	651
482	COL50	SEG16	B	-4053	651
483	COL49		G	-4095	651
484	COL48		R	-4137	651
485	COL47	SEG15	B	-4179	651
486	COL46		G	-4221	651
487	COL45		R	-4263	651
488	COL44	SEG14	B	-4305	651
489	COL43		G	-4347	651
490	COL42		R	-4389	651
491	COL41	SEG13	B	-4431	651
492	COL40		G	-4473	651
493	COL39		R	-4515	651
494	COL38	SEG12	B	-4557	651
495	COL37		G	-4599	651
496	COL36		R	-4641	651
497	COL35	SEG11	B	-4683	651
498	COL34		G	-4725	651
499	COL33		R	-4767	651
500	COL32	SEG10	B	-4809	651
501	COL31		G	-4851	651
502	COL30		R	-4893	651
503	COL29	SEG9	B	-4935	651
504	COL28		G	-4977	651
505	COL27		R	-5019	651
506	COL26	SEG8	B	-5061	651
507	COL25		G	-5103	651
508	COL24		R	-5145	651
509	COL23	SEG7	B	-5187	651
510	COL22		G	-5229	651
511	COL21		R	-5271	651
512	COL20	SEG6	B	-5313	651
513	COL19		G	-5355	651
514	COL18		R	-5397	651
515	COL17	SEG5	B	-5439	651
516	COL16		G	-5481	651
517	COL15		R	-5523	651
518	COL14	SEG4	B	-5565	651
519	COL13		G	-5607	651
520	COL12		R	-5649	651
521	COL11	SEG3	B	-5691	651
522	COL10		G	-5733	651
523	COL9		R	-5775	651
524	COL8	SEG2	B	-5817	651
525	COL7		G	-5859	651
526	COL6		R	-5901	651
527	COL5	SEG1	B	-5943	651
528	COL4		G	-5985	651
529	COL3		R	-6027	651
530	COL2	SEG0	B	-6069	651
531	COL1		G	-6111	651
532	COL0		R	-6153	651

Pad #	Signal	X-pos	Y-pos
533	ROW34	-6279	651
534	ROW35	-6321	651
535	ROW36	-6363	651
536	ROW37	-6405	651
537	ROW38	-6447	651
538	ROW39	-6489	651
539	ROW40	-6531	651
540	ROW41	-6573	651
541	ROW42	-6615	651
542	ROW43	-6657	651
543	ROW44	-6699	651
544	ROW45	-6741	651
545	ROW46	-6783	651
546	ROW47	-6825	651
547	ROW48	-6867	651
548	ROW49	-6909	651
549	ROW50	-6951	651
550	ROW51	-6993	651
551	ROW52	-7035	651
552	ROW53	-7077	651
553	ROW54	-7119	651
554	ROW55	-7161	651
555	ROW56	-7203	651
556	ROW57	-7245	651
557	ROW58	-7287	651
558	ROW59	-7329	651
559	ROW60	-7371	651
560	ROW61	-7413	651
561	ROW62	-7455	651
562	ROW63	-7497	651
563	ROW64	-7539	651
564	ROW65	-7581	651
565	ROW66	-7623	651
566	ROW67	-7665	651
567	DUMMY	-7718.5	651

Bump Size

PAD#	X [um]	Y [um]	Pad pitch [um] (Min)
Pad 1-203	56	92	76.3
Pad 204	50	118	53.5
Pad 205 - 566	27	118	42
Pad 567	50	118	53.5



6 PIN DESCRIPTION

6.1 $\overline{CS}$

This pin is the chip selection input. The chip is enabled for MCU communication only when $\overline{CS}$ is pulled low.

6.2 $\overline{RES}$

This pin is the reset signal input. Initialization of the chip is started once the reset pin is pulled low. The minimum pulse width for reset sequence is 10us.

6.3 D/$\overline{C}$

This pin is Data/Command control pin. When the pin is pulled high, the input at D7-D0 is treated as display data. When the pin is pulled low, the input at D7-D0 will be transferred to the command register.

6.4 R/$\overline{W}$ ($\overline{WR}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as Read/Write R/$\overline{W}$ selection input. Read mode will be carried out when this pin is pulled high and write mode when this pin is pulled low.

When 8080 interface mode is selected, this pin is the Write ($\overline{WR}$) control signal input. Data write operation is initiated when this pin is pulled low and the chip is selected.

6.5 E($\overline{RD}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/ write operation is initiated when this pin is pulled high and the chip is selected.

When 8080 interface mode is selected, this pin is the Read ($\overline{RD}$) control signal input. Data read operation is initiated when this pin is pulled low and the chip is selected.

6.6 PS0 – PS1

These pins are the bus interface mode selection input. Different bus interface can be selected changing the setting of these pins.

PS1	PS0	MPU Interface
L	H	8-bit 8080 parallel interface
H	H	8-bit 6800 parallel interface
H	L	3-lines serial peripheral interface (SPI) – 9 bits SPI
L	L	4-lines serial peripheral interface (SPI)

Note1: For serial applications, D0 – D5, R/$\overline{W}$ ($\overline{WR}$), E($\overline{RD}$) are recommended to connect V_{DD}.
Note2: Read back operation is only available in parallel mode

6.7 D7-D0

These pins are the 8-bit bi-directional data bus in parallel interface mode. D7 is the MSB while D0 is the LSB. When serial mode selected, D7 is the serial data input SDA and D6 is the serial clock input SCK.

6.8 VL_{REF}

This pin is the ground of operation amplifier V_{L4} and V_{L5}. It must connect to V_{SS}.

6.9 VH_{REF}

This pin is the power supply pin of the operation amplifier V_{L3}.It must connect to V_{OUT}

6.10 V_{CIX2}

This pin is internal reference pin. It must connect to V_{CI}

6.11 V_{DD}

This pin is the system power supply pin of the logic block.

6.12 V_{DDIO}

This pin is the system power supply pin of I/O buffer. Please refer to Figure on page 69 for connection example.

6.13 V_{CI}

This pin is the reference voltage input for internal DC-DC converter. The DC-DC converter output is equals to the multiple factor (3X, 4X, 5X or 6X) times of V_{CI} with respect to V_{SS}. The maximum output voltage will limit by the max. V_{OUT} characteristic.
Note: Voltage at this input pin must be larger than or equal to V_{DD}. ($V_{CI} \geq V_{DD}$)

6.14 V_{SS}

This pin is the ground of logic.

6.15 RV_{SS}

This pin is the ground of Vref.

6.16 CV_{SS}

This pin is the ground of analog.

6.17 V_{OUT}

This is the most positive voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter. If the internal DC-DC converter generates the voltage level at V_{OUT}, the voltage level is used for internal referencing only. The voltage level at V_{OUT} pin is not used for driving external circuitry.

6.18 V_{L5}, V_{L4}, V_{L3} and V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:

$V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$

	1 : a bias
V_{L5}	(a-1)/a * V_{out}
V_{L4}	(a-2)/a * V_{out}
V_{L3}	2/a * V_{out}
V_{L2}	1/a * V_{out}

Table 3 - $V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$ Relationship

6.19 ROW0 – ROW67

These pins provide the driving signals, COMMON, to the LCD panel.

6.20 COL0 – COL293

These pins provide the LCD driving signals, SEGMENT, to the LCD panel. The Red, Green, Blue colors signal are sent out from the SEGMENT output at the same time. The output voltage level of these pins is V_{DD} during sleep mode or standby mode.

6.21 CL

This pin is the system clock I/O. This pin is the external clock input for the device, which is enabled by using extended command. It should be left open under normal operation. The internal oscillator will be used after power on reset.

6.22 M

This pin is used for cascade purpose only. It should be left open under normal operation.

6.23 SYN

This pin is used for cascade purpose only. It should be left open under normal operation.

6.24 BUSY

This pin will be high during RAM buffer read/write operation and during graphic commands executing. System programmer should read this pin (low is ready, high is busy) before sending next RAM buffer related command (e.g. RAM write – 5CH; RAM read – 5DH OR any graphic commands)

6.25 TEST1 ~ TEST18

These pins are used for internal only and should be left open, any connection is not allowed.

6.26 Dummy

This is a floating dummy pad without any internal circuitry connection.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Microprocessor Interface Logic

The Microprocessor Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS0 to PS1 pins. Please refer to the pin descriptions on page 14.

a) MPU Parallel 6800-series Interface

The parallel Interface consists of 8 bi-directional data pins (D7 – D0), R/$\overline{W}$, D/$\overline{C}$, E, $\overline{CS}$. R/$\overline{W}$ ($\overline{WR}$) input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. R/$\overline{W}$ input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E input serves as data latch signal (clock) when high provided that $\overline{CS}$ is low. Please refer to Figure 19 & Figure 20 on page 57 to 58 for Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

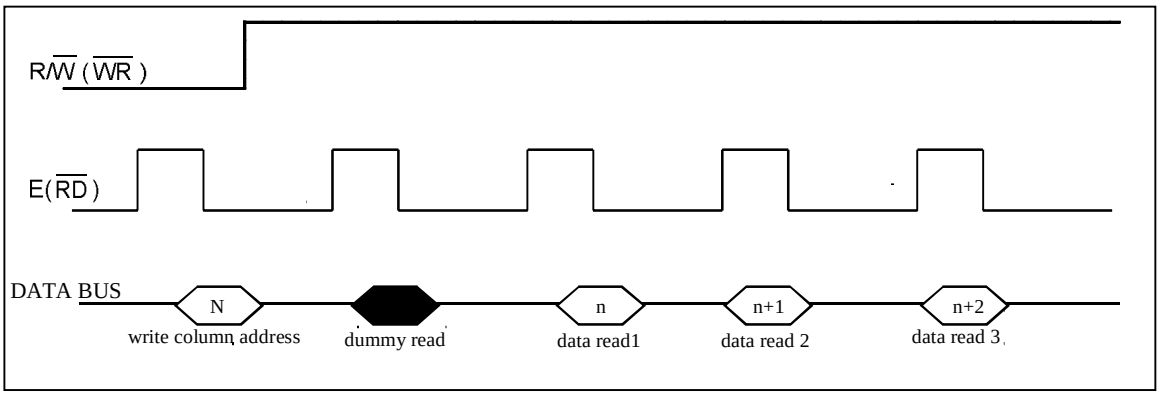


Figure 3 - Display Data

b) MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins D7 – D0, $\overline{RD}$, $\overline{WR}$, D/$\overline{C}$, $\overline{CS}$. $\overline{RD}$ input serves as data read latch signal (clock) when low provided that $\overline{CS}$ is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by D/$\overline{C}$. $\overline{WR}$ input serves as data write latch signal (clock) when low provided that $\overline{CS}$ is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by D/$\overline{C}$. A dummy read is also required before the first actual display data read for 8080-series interface.

c) MPU 4-lines Serial Peripheral Interface

The 4-lines serial peripheral Interface consists of serial clock SCK, serial data SDA, D/$\overline{C}$, $\overline{CS}$. SDA is shifted into 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6 …… data bit 0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock. Please refer to Figure 23 on page 61 for serial interface timing.

d) MPU 3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while D/$\overline{C}$ is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/$\overline{C}$ bit, D7 to D0 bit. The D/$\overline{C}$ bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/$\overline{C}$ bit = 1) or the command register (D/$\overline{C}$ bit = 0).

	6800 – series Parallel Interface	**8080 – series Parallel Interface**	**3-lines or 4-lines Serial peripheral Interface**
Data Read	8-bits	8-bits	No
Data Write	8-bits	8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes

Table 4 - Data bus selection modes

7.2 Reset Circuit

This block is integrated into the Microprocessor Interface Logic which includes Power On Reset circuitry and the hardware reset pin, $\overline{RES}$. Both of these having the same reset function. Once the $\overline{RES}$ pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10us. The status of the chip after reset is given by:

When $\overline{RES}$ input is low, the chip is initialized to the following:

1.	Display ON/OFF:	Display is OFF
2.	Normal/Inverse Display:	Normal Display
3.	COM Scan Direction:	COM0 -> COM67
4.	Internal Oscillator:	Disable
5.	Reference Voltage Generation Circuit:	Disable
6.	Voltage regulator and Voltage Follower:	Disable
7.	Booster level:	6X
8.	Bias ratio:	1/7(68 Mux)
9.	Multiplex ratio:	68 Mux
10.	Contrast Level:	32
11.	Internal regulator gain:	2.84
12.	Average temperature gradient:	-0.2%/^{o}C
13.	Partial display mode:	Disable
	Start COM address:	0
	End COM address:	0
14.	Area Scroll set	
	Top block address:	0
	Bottom block address:	0
	Number of specified block:	0
	Area scroll mode:	Whole screen scroll mode
15.	Scroll start set	
	Start block address:	0
16.	Data Scan Direction	
	Normal/inverse display of page address:	Normal
	Normal/inverse display of column address:	Normal
	Address-scan direction:	Column direction
	RGB arrangement:	RGB
	Gray-scale setup:	8 gray-scale
17.	Start Page Address set:	0
18.	End Page Address set:	0
19.	Start Column address set:	0
20.	End Column address set:	0
21.	Select PWM/FRC	2-bit PWM + 2 bit FRC mode

7.3 Command Decoder

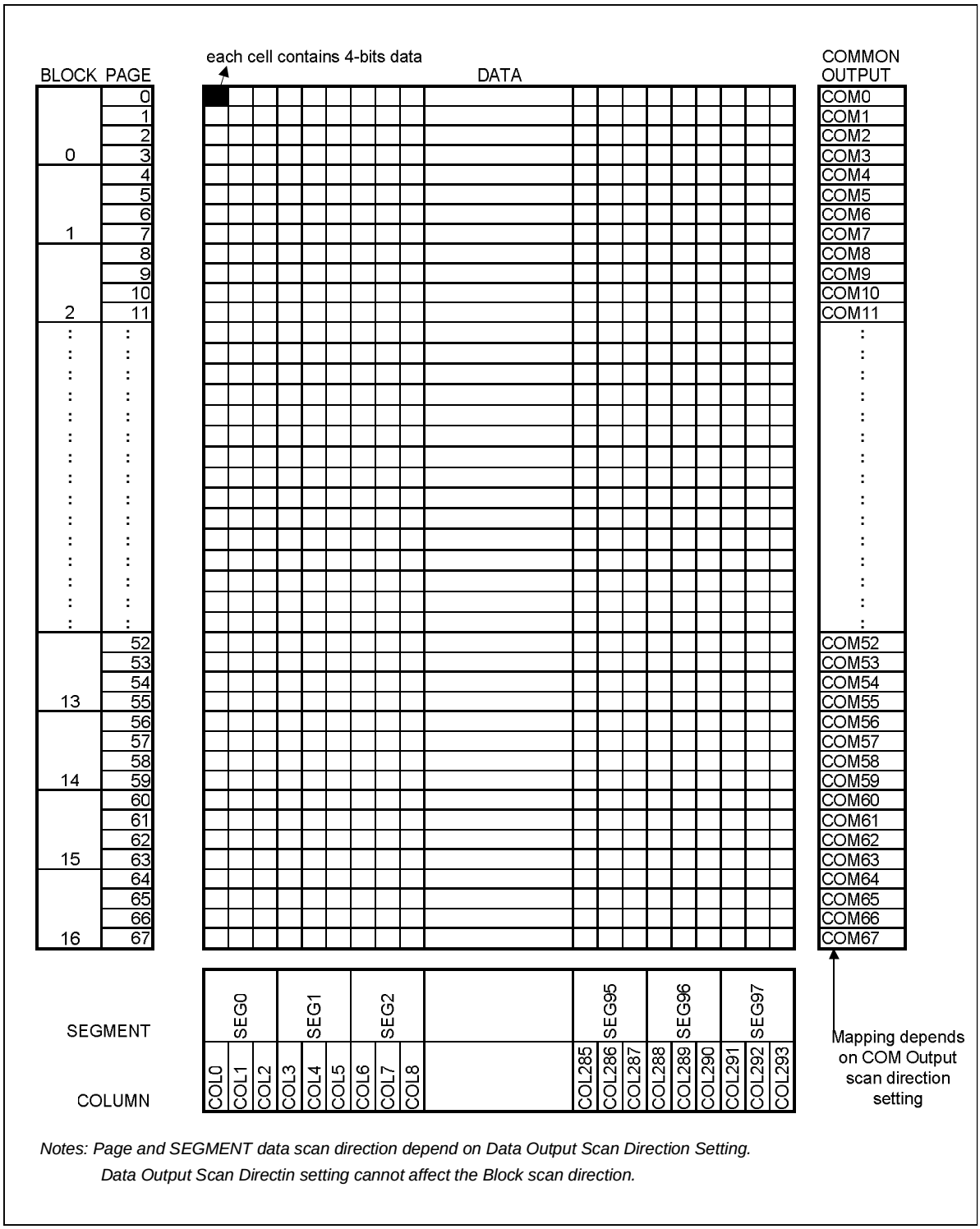
This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/$\overline{C}$ pin. If D/$\overline{C}$ pin is high, data is written to Graphic Display data RAM (GDDRAM). If it is low, the input at D7 – D0 is interpreted as a Command and it will be decoded. The decoded command will be written to the corresponding command register.

7.4 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 294 (98 RGB) x 68 x 4 = 79,968 bits. Figure 4 on page 21 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command “Data Output/Scan direction” in Table 5 on page 24 for detail description.

Four pages of display data form a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command “Set area Scroll” and “Set Scroll Start” in Table 11 on page 39.

In order to ease the access of the red, green and blue color data; the 8-bits color data (Red: 3 bits, Green: 3 bits, Blue: 2 bits) is converted to 4-bits data (P10, P11, P12, P13). The 4-bits data are stored into the GDDRAM such that the data are located in the appropriate RAM locations according to the gray scale settings. Please refer to the description section of the command “Set Data Output/Scan Direction” on page 24.



Notes: Page and SEGMENT data scan direction depend on Data Output Scan Direction Setting.
Data Output Scan Directin setting cannot affect the Block scan direction.

Figure 4 - Display Data RAM Map

7.5 LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages. It consists of:

1. 3X, 4X, 5X and 6X DC-DC voltage converter
2. Bias Divider - If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{OUT}) to give the LCD driving levels (V_{L2} - V_{L5}). The divider does not require external capacitors to reduce the external hardware and pin counts, power configuration of op-amp is shown on Figure 5 on page 22.
   Contrast Control -Software control of 64 voltage levels of LCD voltage.
3. Bias Ratio Selection circuitry – Software control of 1/4 to 1/8 bias ratio to match the characteristic of LCD panel.
4. Self adjust temperature compensation circuitry - Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is -0.2%/°C.

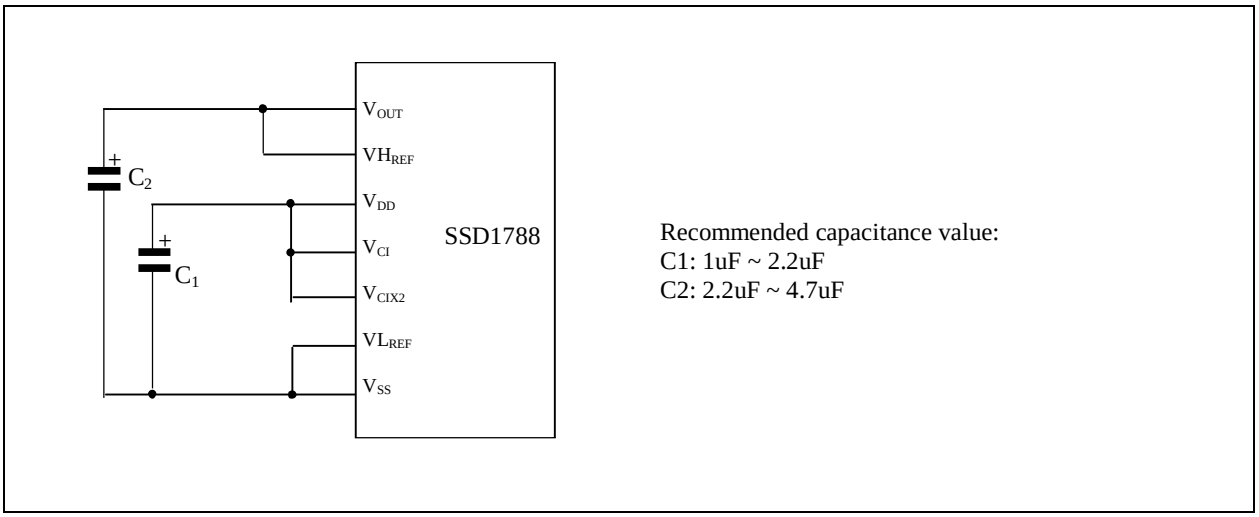


Figure 5 - SSD1788 Hardware Configurations

7.6 Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 6). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

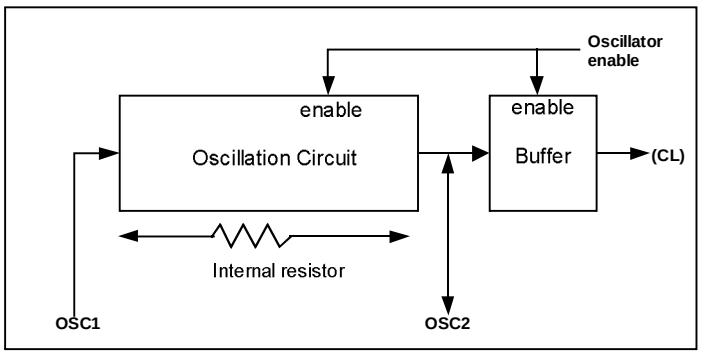


Figure 6 - Oscillator structural block diagram

7.7 Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

7.8 HV Buffer Cell (Level Shifter)

This block is embedded in the Segment/Common Driver Circuits. HV Buffer Cell works as a level shifter, which translates the low voltage output signal to the required driving voltage. The output is shifted out with reference to the internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector, which is synchronized with the internal M signal.

7.9 Level Selector

This block is embedded in the Segment/Common Driver circuits. Level Selector is a control of the display synchronization. Display voltage levels can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

8 COMMAND TABLE

Table 5 - Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	15	0 X_7 Y_7	0 X_6 Y_6	0 X_5 Y_5	1 X_4 Y_4	0 X_3 Y_3	1 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Column Address	Set the start column address by $X_7X_6X_5X_4X_3X_2X_1X_0$ Set the end column address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ Column address = 00000000b (POR) In 8-levels gray scale mode, column address is in a range of 0~97. In 16-level gray scale mode, column address is in a range of 0~48.
0 1 1	75	0 X_7 Y_7	1 X_6 Y_6	1 X_5 Y_5	1 X_4 Y_4	0 X_3 Y_3	1 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Page Address	Set the start page address by $X_7X_6X_5X_4X_3X_2X_1X_0$ Set the end page address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$. Page address = 00000000b (POR)
0 1	BB	1 *	0 *	1 *	1 *	1 *	0 X_2	1 X_1	1 X_0	Set COM Output Scan Direction	X_2 X_1 X_0 ROW0…ROW33 ROW34…ROW67 0 0 0 COM0 ->COM33 COM34 ->COM67 (POR) 0 0 1 COM0 ->COM33 COM67 <-COM34 0 1 0 COM33<-COM0 COM34 ->COM67 0 1 1 COM33<-COM0 COM67 <-COM34
0 1 1 1	BC	1 * * *	0 * * *	1 * * *	1 * * *	1 * * *	1 P_{12} P_{22} P_{32}	0 P_{11} P_{21} P_{31}	0 P_{10} P_{20} P_{30}	Set Data Output Scan Direction	a) Normal or Reverse page/column/scan directions P_{10} = 0: set page address to normal display (POR) P_{10} = 1: set page address to inverse display P_{11} = 0: set column address to normal rotation (POR) P_{11} = 1: set column address to inverse rotation P_{12} = 0: set scan direction to column scan (POR) P_{12} = 1: set scan direction to page scan Please refer to the Figure 7 & Figure 8 on page 35 & 36 respectively for detail description of column/page scan direction modes b) RGB color arrangement P_{22}, P_{21}, P_{20}: The control bits are used for setting the (RGB) color arrangement of segment output. , 000 is the POR value. Please refer to the Figure 10 on page 37 for detail mapping of the segment output. c) Gray-scale selection P_{32} P_{31} P_{30} Gray-scale modes 0 0 1 8-levels gray scale mode (POR) 0 1 0 16-levels gray scale mode (Type A) Please refer to the Table 9 on page 37 to Table 10on page 37 for detail description of different gray-scale selection modes.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	CE	1	1	0	0	1	1	1	0	Set Color Look Up Table (Gray-scale selection: P_{32} P_{32} P_{30} = 001)	N DB3 DB2 DB1DB0 color position 1 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate red tone 000 2 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate red tone 001 ⋮ ⋮ 8 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate red tone 111 9 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate green tone 000 ⋮ ⋮ 16 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate green tone 111 17 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate blue tone 00 ⋮ ⋮ 20 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate blue tone 11
1		*	*	*	*	X_{31}	X_{21}	X_{11}	X_{01}		
1		*	*	*	*	X_{32}	X_{22}	X_{12}	X_{02}		
					⋮						
1		*	*	*	*	X_{38}	X_{28}	X_{18}	X_{08}		
1		*	*	*	*	X_{39}	X_{29}	X_{19}	X_{09}		
					⋮						
1		*	*	*	*	X_{316}	X_{216}	X_{116}	X_{016}		
1		*	*	*	*	X_{317}	X_{217}	X_{117}	X_{017}		
					⋮						
1		*	*	*	*	X_{320}	X_{220}	X_{120}	X_{020}		
0	CA	1	1	0	0	1	0	1	0	Set Display Control	Driver duty selection Select driver duty from 1/8 to 1/68. As Y_4 Y_3 Y_2 Y_1Y_0 is increased from 00001b to 10000b, the number of display lines, N is increased at the same rating. To specify the Y_4 Y_3 Y_2 Y_1Y_0. $Y_4 \sim Y_0 = \frac{N}{4} - 1$ A dummy byte should be sent before the command byte Y_4 to Y_0. After the command byte is sent, an additional dummy byte should be sent to the device in order to finish the whole command.
1		0	0	0	0	0	0	0	0		
1		*	*	*	Y_4	Y_3	Y_2	Y_1	Y_0		
1		0	0	0	0	0	0	0	0		
0	AA	1	0	1	0	1	0	1	0	Set Area Scroll	a) Top Block Address $X_4X_3X_2X_1X_0$ is used to specify the block address (1 block = 4 lines) at the top of the scrolling area. Top block address = 00000b (POR) b) Bottom Block Address $Y_4Y_3Y_2Y_1Y_0$ is used to specify the block address (1 block = 4 lines) at the bottom of the scrolling area. Bottom block address = 00000b (POR) c) Number of specified Blocks The number of specified blocks = Number of (Top fixed area + Scroll area) blocks –1. If bottom scroll or whole screen scroll mode is chosen, the number of specified blocks is set to Z_4~Z_0 Number of specified blocks = 00000b (POR) d) Area Scroll Mode There are four types of area scroll. P_{41} P_{40} Types of Area Scroll 0 0 Center Screen Scroll 0 1 Top Screen Scroll 1 0 Bottom Screen Scroll 1 1 Whole Screen Scroll Type of area scroll = Whole Screen Scroll (POR)
1		*	*	*	X_4	X_3	X_2	X_1	X_0		
1		*	*	*	Y_4	Y_3	Y_2	Y_1	Y_0		
1		*	*	*	Z_4	Z_3	Z_2	Z_1	Z_0		
1		*	*	*	*	*	*	P_{41}	P_{40}		
0	AB	1	0	1	0	1	0	1	1	Set Scroll Start	$X_4X_3X_2X_1X_0$ specify the start block address (1 block = 4 lines) of area scrolling. Start block address = 00000b (POR)
1		*	*	*	X_4	X_3	X_2	X_1	X_0		

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	20	0 *	0 *	1 *	0 *	0 X_3	0 X_2	0 X_1	0 X_0	Set Power Control Register	X_0=0: turns off the reference voltage generator (POR) X_0=1: turns on the reference voltage generator X_1=0: turns off the internal regulator and voltage follower (POR) X_1=1: turns on the internal regulator and voltage follower Select booster level X_3 X_2 Boost level 0 0 3X 0 1 4X 1 0 5X 1 1 6X (POR)
0 1 1	81	1 * *	0 * *	0 X_5 *	0 X_4 *	0 X_3 *	0 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Contrast Level & Internal Regulator Resistor Ratio	a) Select contrast level from 64 contrast steps Contrast increases (V2 decreases) as $X_5X_4X_3X_2X_1X_0$ is increased from 000000b to 111111b. $X_5X_4X_3X_2X_1X_0$ = 000000b (POR) b) The internal regulator gain (1+R2/R1) VOUT increases as $Y_2Y_1Y_0$ is increased from 000b to 111b. The factor, 1+R2/R1, is given by: $Y_2Y_1Y_0$ = 000: 2.84 (POR) $Y_2Y_1Y_0$ = 001: 3.71 $Y_2Y_1Y_0$ = 010: 4.57 $Y_2Y_1Y_0$ = 011: 5.44 $Y_2Y_1Y_0$ = 100: 6.30 $Y_2Y_1Y_0$ = 101: 7.16 $Y_2Y_1Y_0$ = 110: 8.03 $Y_2Y_1Y_0$ = 111: 8.89
0	D6 - D7	1	1	0	1	0	1	1	X_0	Increment / Decrement of the contrast set	X_0=0: The contrast set of voltage regulator is incremented by 1 X_0=1: The contrast set of voltage regulator is decremented by 1
0	A6 - A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	X_0=0: normal display (POR) X_0=1: inverse display
0 1 1	A8	1 * *	0 X_6 Y_6	1 X_5 Y_5	0 X_4 Y_4	1 X_3 Y_3	0 X_2 Y_2	0 X_1 Y_1	0 X_0 Y_0	Enter partial Display	$X_6X_5X_4X_3X_2X_1X_0$: Start COM Address = 000000b (POR) $Y_6Y_5Y_4Y_3Y_2Y_1Y_0$: End COM Address = 000000b (POR)
0	A9	1	0	1	0	1	0	0	1	Exit partial Display	Exit the “partial display mode” by executing the command 10101001b (POR)
0	AE - AF	1	0	1	0	1	1	1	X_0	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
0	94 - 95	1	0	0	1	0	1	0	X_0	Enter/Exit sleep mode	X_0=0: exit the sleep mode. X_0=1: enter sleep mode. (POR)
0	D1 - D3	1	1	0	1	0	0	X_1	X_0	Enable/disable internal oscillator	X_1 X_0 Internal oscillator status 0 1 ON 1 0 OFF (POR)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	82	1 *	0 *	0 *	0 *	0 *	0 *	1 X_1	0 X_0	Set Temperature compensation coefficient	Average temperature gradients X_1 X_0 Average Temperature Gradient [%/oC] 0 0 -0.10 0 1 -0.15 1 0 -0.20(POR) 1 1 -0.25
0	25	0	0	1	0	0	1	0	1	NOP	Command result in No Operation The command should be issued after the execution of the Status Read command
0 1	5C	0 Y_{71}	1 Y_{61}	0 Y_{51}	1 Y_{41}	1 Y_{31}	1 Y_{21}	0 Y_{11}	0 Y_{01}	Write display data	Enter the “write display data mode ” by executing the command 01011100b. The following byte is used to specify the data byte to be written to the GDDRAM directly. The bit should be stated at logic “1” during the display data is written to the GDDRAM.

Graphic command table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	83	1	0	0	0	0	0	1	1	Draw Line	Enter the "Draw line mode" by executing the command 10000011. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The remaining two bytes are used to specify the color. *Remarks: A ≤97; B ≤67; C ≤97; D ≤67*
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		
0	92	1	0	0	1	0	0	1	0	Fill Enable/Disable	Enter the "Fill Enable/Disable mode" by executing the command 10010010. A_0=0: Filled color option is disabled (POR) A_0=1: Filled color option is enabled
1		*	*	*	*	*	*	*	A_0		
0	84	1	0	0	0	0	1	0	0	Draw rectangle	Enter the "Draw rectangle mode" by executing the command 10000100. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The next two bytes are used to specify the color. The last two bytes are used to specify the fill color. *Remarks: A ≤C; B ≤D; C ≤97; D ≤67*
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		
0	8A	1	0	0	0	1	0	1	0	Copy	Enter the "Copy mode" by executing the command. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The remaining two bytes (E_0 to E_7, F_0 to F_7) are used to specify the new location of X coordinates and Y coordinates. *Remarks: A ≤C; B ≤D; C ≤97; D ≤67*
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	8C	1	0	0	0	1	1	0	0	Dim Window	Enter the "Dim Window mode" by executing the command 10001100. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The selected window area will be dimmed by 75% white. *Remarks: A ≤C; B ≤D; C ≤97; D ≤67*
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	8E	1	0	0	0	1	1	1	0	Clear Window	Enter the "Clear Window mode" by executing the command 10001110. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. All pixels contrast will be set to 0. *Remarks: A ≤C; B ≤D; C ≤97; D ≤67*
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		

Remarks: After executed the graphic command, waiting time is required for update GDDRAM content. (When V_{DD}=1.8~2.6V, waiting time = 250ns/pixel; When V_{DD}=2.6~3.6V, waiting time = 125ns/pixel)

Extended command table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	FB	1 *	1 *	1 *	1 *	1 0	0 B_2	1 B_1	1 B_0	Set biasing ratio	Allow user to set bias from 1/ 4 to 1/8 $B_2B_1B_0$ Bias ratio 0 0 0 1/4 bias 0 0 1 1/5 bias 0 1 0 1/6 bias 0 1 1 1/7 bias (POR) 1 0 0 1/8 bias 1 0 1 Reserved 1 1 X Reserved
0 1 1	F2	1 0 0	1 0 0	1 0 C_0	1 0 N_4	0 F_3 N_3	0 F_2 N_2	1 F_1 N_1	0 F_0 N_0	Set Frame frequency and N-line Inversion	This command uses to change the frame frequency; set the N-line inversion and N-line inversion mode $F_3F_2F_1F_0$ 1 1 1 1 : 111Hz 1 1 1 0 : 103.5Hz 1 1 0 1 : 98Hz 1 1 0 0 : 93Hz 1 0 1 1 : 89 Hz 1 0 1 0 : 85 Hz 1 0 0 1 : 81.5 Hz 1 0 0 0 : 78 Hz (POR) 0 1 1 1 : 76.5 Hz 0 1 1 0 : 73.5 Hz 0 1 0 1 : 71 Hz 0 1 0 0 : 68 Hz 0 0 1 1 : 66.5 Hz 0 0 1 0 : 64.5 Hz 0 0 0 1 : 62.5 Hz 0 0 0 0 : 60.5 Hz C_0 = 0 : The counter reset per N-line and each frame C_0 = 1 : The counter reset per N-line only The second byte data sets the n-line inversion register from 2 to 32 lines to reduce display crosstalk. Register values from 00001b to 11111b are mapped to 2 lines to 32 lines respectively. Value 00000b disables the N-line inversion. 00110 is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux should NOT be a multiple of the lines of inversion (n).
0 1 1 1	F7	1 0 0 *	1 0 0 *	1 1 1 *	1 0 0 *	0 1 1 0	1 0 1 1	1 0 X_1 0	1 0 X_0 1	Select PWM/FRC	4 bits PWM/FRC or 2 bits PWM + 2 bits FRC selection X_1X_0 0 0 : 4 bits PWM 0 1 : 4 bits FRC 1 0 : 2 bits PWM + 2 bits FRC (POR) 1 1 : Reserved

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	F6	1 0 0	1 0 0	1 0 0	1 1 0	0 X_3 Y_0	1 X_2 0	1 X_1 1	0 X_0 0	OTP setting	This command set the offset value of contrast $X_3X_2X_1X_0$ 0 0 0 0 : original contrast (POR) 0 0 0 1 : original contrast + 1 step 0 0 1 0 : original contrast + 2 steps 0 0 1 1 : original contrast + 3 steps 0 1 0 0 : original contrast + 4 steps 0 1 0 1 : original contrast + 5 steps 0 1 1 0 : original contrast + 6 steps 0 1 1 1 : original contrast + 7 steps 1 0 0 0 : original contrast - 8 steps 1 0 0 1 : original contrast - 7 steps 1 0 1 0 : original contrast - 6 steps 1 0 1 1 : original contrast - 5 steps 1 1 0 0 : original contrast - 4 steps 1 1 0 1 : original contrast - 3 steps 1 1 1 0 : original contrast - 2 steps 1 1 1 1 : original contrast - 1 step Y_0 = 0 : Disable the OTP setting you have set Y_0 = 1 : Enable the OTP setting you have set (POR)
0	F8	1	1	1	1	1	0	0	0	OTP programming	This command start to program LCD driver with OTP offset value. Each bit can be programmed to 1 once. Detail of OTP programming procedure on page 47

Table 6 - Read Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	5D	0 0 Y_{71}	1 0 Y_{61}	0 0 Y_{51}	1 0 Y_{41}	1 0 Y_{31}	1 0 Y_{21}	0 0 Y_{11}	1 0 Y_{01}	Read display data	Enter the "read display data mode " by executing the command 01011100b. The next byte is a dummy data. The GDDRAM data will be read form the second byte. The GDDRAM column address pointer will be increased by one automatically after each data read (8-levels gray scale mode) OR after each 3-bytes data read. (16-levels gray scale mode). *Remarks: R/$\overline{W}$ = 1 when D7 to D0 is read*
0 0	5D	0 D_7	1 D_6	0 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0	Status Register Read	D_7D_6 = 00: Center Screen Scroll Mode D_7D_6 = 01: Top Screen Scroll Mode D_7D_6 = 10: Bottom Screen Scroll Mode D_7D_6 = 11: Whole Screen Scroll Mode D_4 = 0: Scan Direction is column direction D_4 = 1: Scan Direction is page direction D_3 = 0: Display is OFF D_3 = 1: Display is ON D_2 = 0: Sleep Mode is disabled D_2 = 1: Sleep Mode is enabled D_1 = 0: Display is Inverse D_1 = 1: Display is Normal D_0 = 0: Partial display is disabled D_0 = 1: Partial display is enabled *Remarks: R/$\overline{W}$ = 1 when D7 to D0 is read*

Note: Command patterns other than that given in Command Table are prohibited. Otherwise, unexpected result will occur.
Remarks: "" denote DON'T CARE bit*

8.1 Data Read / Write

To read data from the GDDRAM, 5Dhex command should be executed then input High to R/$\overline{W}$ ($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode. Low to E($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read in 8-levels gray scale mode OR after each 3-bytes data read in 16-levels gray scale mode. Also, a dummy read is required before the first data is read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/$\overline{W}$ ($\overline{WR}$) pin and High to D/$\overline{C}$ pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write in 8-levels gray scale mode OR each 3-bytes data write in 16-levels scale mode. The address will be reset to 0 in next data read/write operation is executed when it is 97.

9 COMMAND DESCRIPTIONS

9.1 Set Column Address (15 Hex)

This command specifies the 8-bit column address of the display data RAM. The start and the end column address are specified by this command. The driver supports up to 98 columns. As the addresses are incremented from the start column to the end column in the column direction scan, the page address is automatically incremented by 1. The column address is then returned to the start column. The column address will be increased by each data access after it is preset by the MCU. Start column < End column must be maintained.

RGB Alignment using 8-levels gray scale mode

LCD Read Direction			Column																					COMMON OUTPUTS
	P11:0		0			1			2			3				96			97					
	P11:1		97			96			95			94				1			0					
	Color		R	G	B	R	G	B	R	G	B	R	G	B		R	G	B	R	G	B			
	Data / Page		D7 D6 D5	D4 D3 D2	D1 D0	D7 D6 D5	D4 D3 D2	D1 D0	D7 D6 D5	D4 D3 D2	D1 D0	D7 D6 D5	D4 D3 D2	D1 D0		D7 D6 D5	D4 D3 D2	D1 D0	D7 D6 D5	D4 D3 D2	D1 D0			
BLOCK	P10:0	P10:1																						
0	0	67																						COM0
	1	66																						COM1
	2	65																						COM2
	3	64																						COM3
1	4	63																						COM4
	5	62																						COM5
	6	61																						COM6
	7	60																						COM7
:	:	:													:									:
:	:	:													:									:
:	:	:													:									:
:	:	:													:									:
:	:	:													:									:
:	:	:													:									:
:	:	:													:									:
:	:	:													:									:
:	:	:													:									:
14	56	11																						COM56
	57	10																						COM57
	58	9																						COM58
	59	8																						COM59
15	60	7																						COM60
	61	6																						COM61
	62	5																						COM62
	63	4																						COM63
16	64	3																						COM64
	65	2																						COM65
	66	1																						COM66
	67	0																						COM67

SEGMENT OUTPUTS	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7	COL8	COL9	COL10	COL11		COL288	COL289	COL290	COL291	COL292	COL293

Table 7 - RAM arrangements of 8-levels gray scale mode

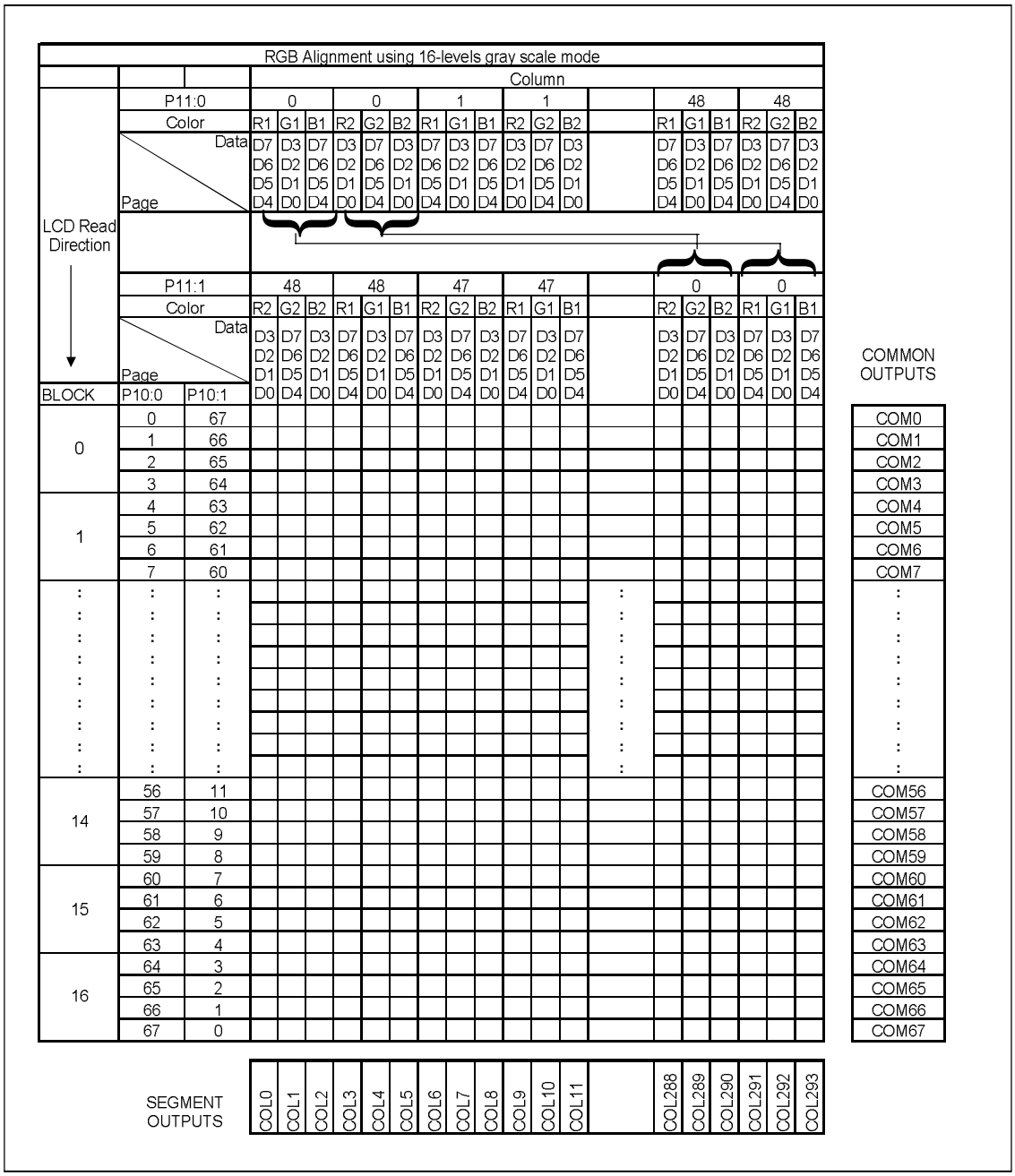


Table 8 - RAM arrangements of 16-levels gray scale mode

9.2 Set Page Address (75 Hex)

This command enters the page address from 0 to 67 to the RAM page register for read/write operations. The driver supports up to 68 lines. All in all, there are 68 pages. As the addresses are incremented from the start page to the end page in the page direction scan, the column address is incremented by 1. The page address is then returned to the start page. Start page < End page must be maintained.

9.3 Set COM Output Scan Direction (BB Hex)

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. Please refer to the Table 5 on Page 24 for detail mapping. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

9.4 Set Data Output Scan Direction (BC Hex)

This command sets the DDRAM such that the MPU operates the display data in the internal RAM.

A. Normal or Inverse page/column/scan directions
The Data Scan direction can be set to either normal or inverse display page and column address scan direction. The column and the page direction are illustrated in the Figure 7 and Figure 8 on page 35 & 36, and Figure 9 on page 36 for example of Normal or Reverse page/column/ scan directions.

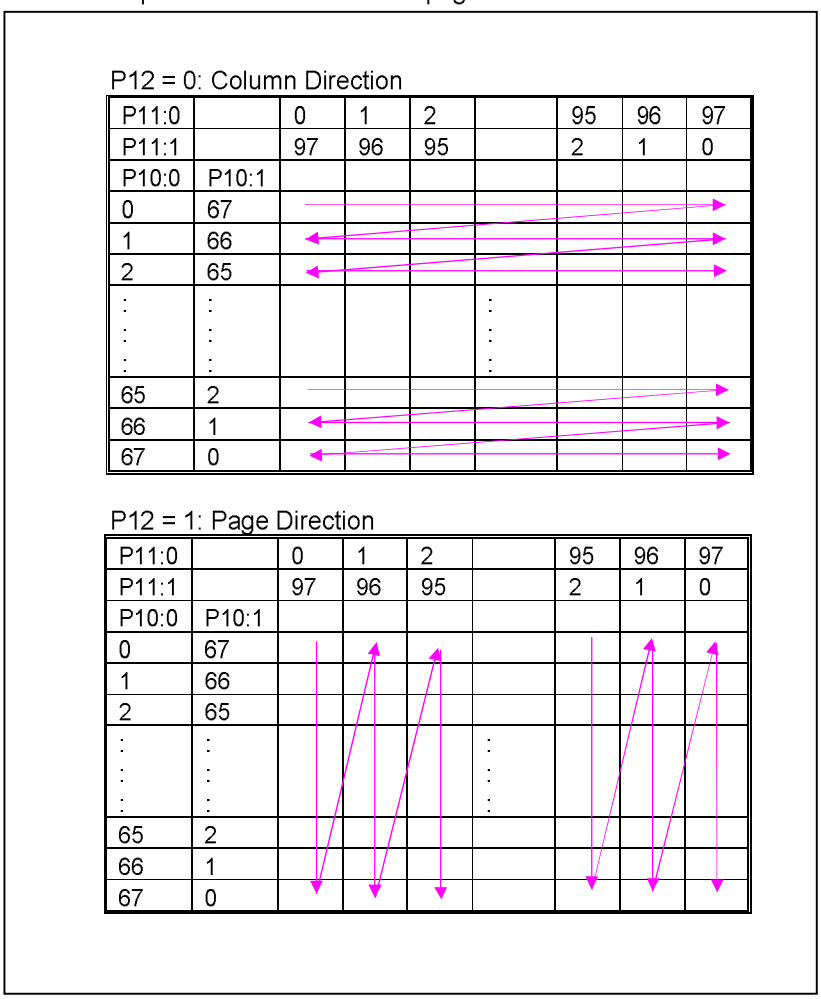


Figure 7 - column and page scan direction of 8-level gray scale mode

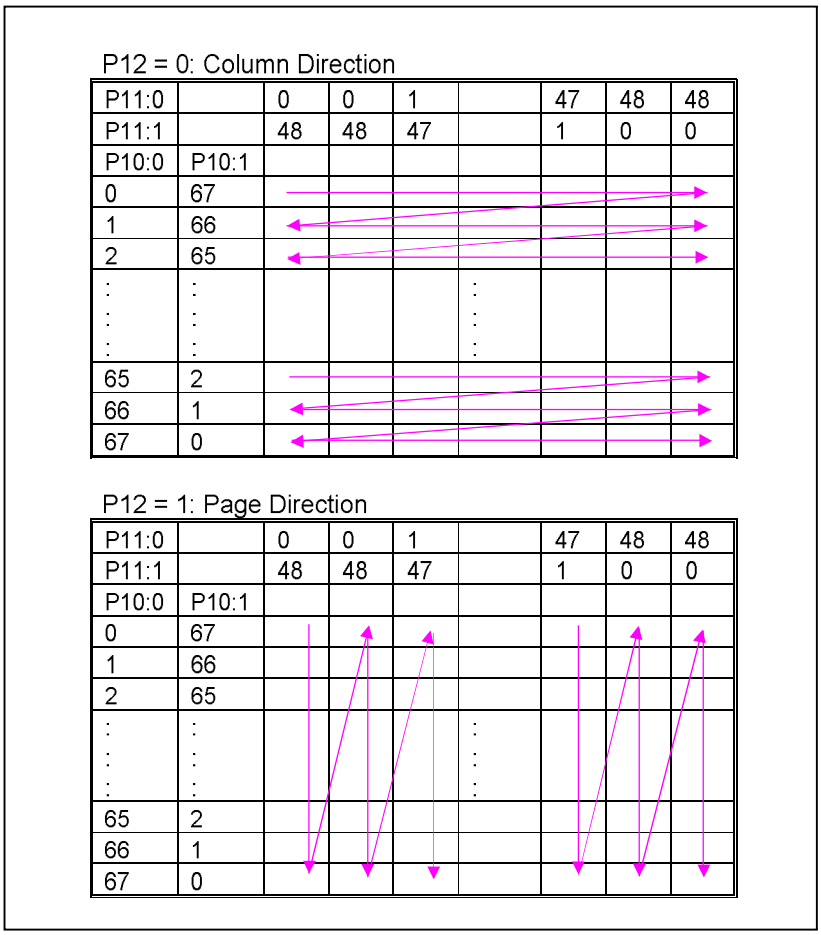


Figure 8 - column and page scan direction of 16-level gray scale mode

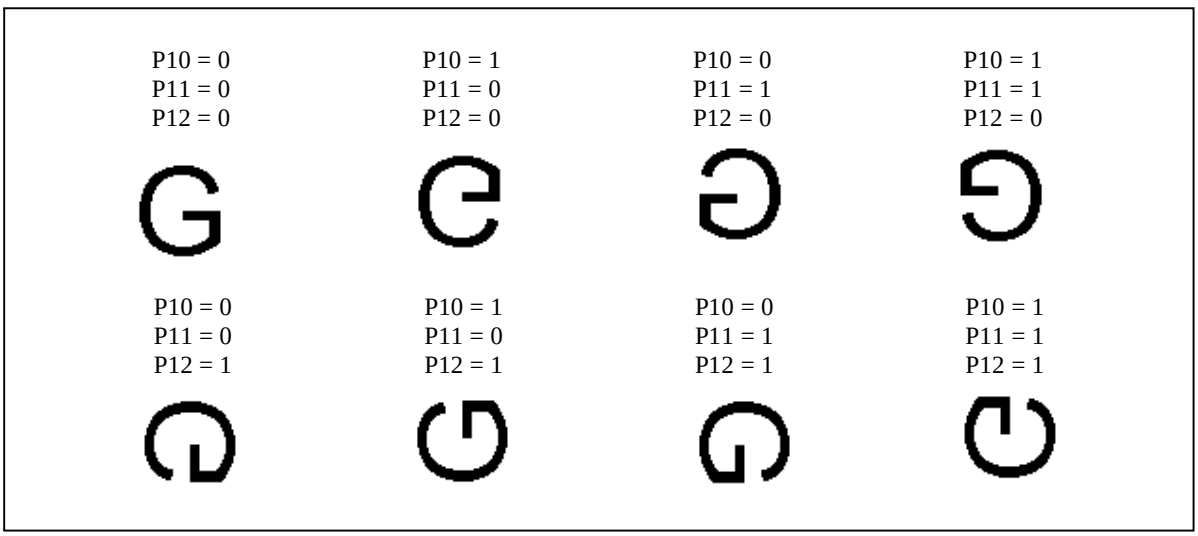


Figure 9 – Example of Normal or Reverse page/column/ scan directions

The parameters following the command set data output scan direction specifies the RGB arrangement and the selection of various gray-scale modes. Please find the information of the RGB arrangement and the gray scale mode in the following section.

B. RGB arrangement mode

The RGB arrangement mode can be selected according to the following table. Three selection bits will give eight combinations of the RGB arrangements. Each combination set will specify the Red, Green and Blue segment output arrangement in odd and even page.

P22, P21, P20	LINE	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7	…	COL293
000	Even page	R	G	B	R	G	B	R	G	…	B
	Odd page	R	G	B	R	G	B	R	G		B
001	1	B	G	R	B	G	R	B	G	…	R
	2	B	G	R	B	G	R	B	G		R
010	1	R	G	B	B	G	R	R	G	…	R
	2	R	G	B	B	G	R	R	G		R
011	1	B	G	R	R	G	B	B	G	…	B
	2	B	G	R	R	G	B	B	G		B
100	1	R	G	B	R	G	B	R	G	…	B
	2	B	G	R	B	G	R	B	G		R
101	1	B	G	R	B	G	R	B	G	…	R
	2	R	G	B	R	G	B	R	G		B
110	1	R	G	B	B	G	R	R	G	…	R
	2	B	G	R	R	G	B	B	G		B
111	1	B	G	R	R	G	B	B	G	…	B
	2	R	G	B	B	G	R	R	G		R

Table 9 - RGB Arrangement modes

C. Gray scale mode

The gray scale mode can be selected according to the following table. Two types of gray scale mode such that the device can display between 256 colors or 4096 colors.

P32	P31	P30	Numbers of Gary-scale
0	0	1	8 gray-scale mode
0	1	0	16 gray-scale mode

Table 10 - Gray scale selection mode

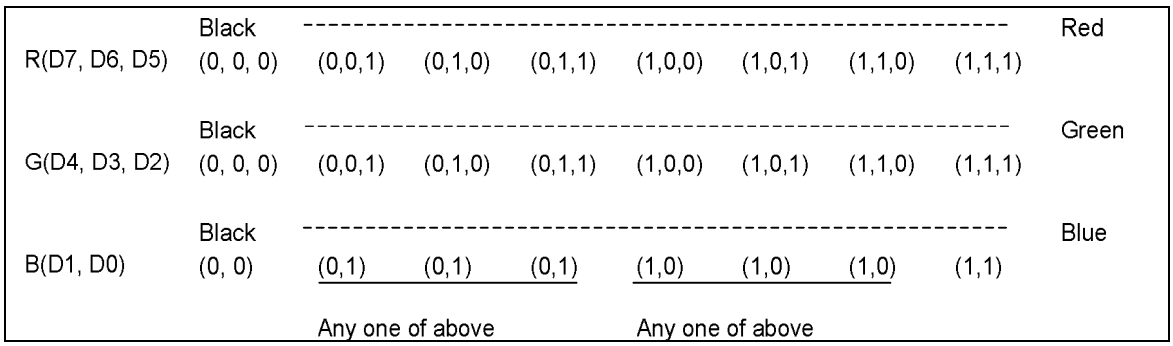


Figure 10 - Examples: 8 gray-scale display arrangement

Description of different gray-scale display

8-gray-scale display:
Table 7 on page 33 shows the arrangement of the display data. The data D7, D6, D5, D4, D3, D2, D1, D0 (RRRGGGBB) is converted into 4-bits data (RRRRGGGGBBBB). The 4-bits data is then stored into the GDDRAM.

16-gray-scale display:
Table 8 on page 34 shows the arrangement of the display data. The data D7, D6, D5, D4, D3, D2, D1, D0 is encoded and write into the GDDRAM in three operation cycles.

D7, D6, D5, D4, D3, D2, D1, D0: R1, R1, R1, R1, G1, G1, G1, G1 (1^{ST} write)

D7, D6, D5, D4, D3, D2, D1, D0: B1, B1, B1, B1, R2, R2, R2, R2 (2^{ND} write)

D7, D6, D5, D4, D3, D2, D1, D0: G2, G2, G2, G2, B2, B2, B2, B2 (3^{RD} write)

9.5 Set Color Look Up Table (CE Hex)

This command transforms the display data (R: 3 bits, G: 3 bits, B: 2 bits) into 4-bit data. The 4 bit data will then be stored into the GDDRAM by choosing colors to represent red, green and blue from 4096 colors. When the GDDRAM output the data, the red, green and blue data are converted back to 8 bit data (R: 3 bits, G: 3 bits, B: 2 bits). The Color Look-up Table must be set when using 8-levels gray scale mode.

9.6 Set Display Control (CA Hex)

This command is used to select the duty ratio of the IC. All available driving duty can be selected using this command. The driving duty can be changed from 1/8 to 1/68.

9.7 Set Area Scroll (AA Hex)

This command specifies the portion of screen for scrolling. The command sets the starting block address, finishing block address, number of specific blocks and the area scroll mode of the area scrolling. Please be noted that the starting block address should be smaller than the finishing block address.

The block address increment direction is started at 0^{th} block such that the GDDRAM address corresponds to the top of the fixed area. Similarly, the block address decrement direction is started at the 16^{th} block such that the GDDRAM address corresponds to the bottom fixed area. The remaining block address excluding the top and the bottom fixed areas are assigned to the scroll plus the background areas.
The set area scroll function is divided into four parts.

Part I -Specify the top block address of the scroll + the background areas. Specify the 0^{th} block for the top screen scroll or the whole screen scroll. The scroll start block address is also set at this top block address until the scroll start set command is executed.

Part II – Specify the bottom address of the scroll + background areas. Specify the 16^{th} block for the bottom or the whole screen scroll.

Part III – Specify number of scrolled blocks = number of (Top fixed area + scroll area) blocks –1. When the bottom scroll or whole screen scroll is chosen, the resulted value is identical to the value stated in part II.

Part IV
Specify the area scroll type. Altogether there are four types of area scroll. Please refer to Table 11 for detail.

P41	P40	Types of Area Scroll
0	0	Center Screen Scroll
0	1	Top Screen Scroll
1	0	Bottom Screen Scroll
1	1	Whole Screen Scroll

Table 11 - Area scrolling selection modes

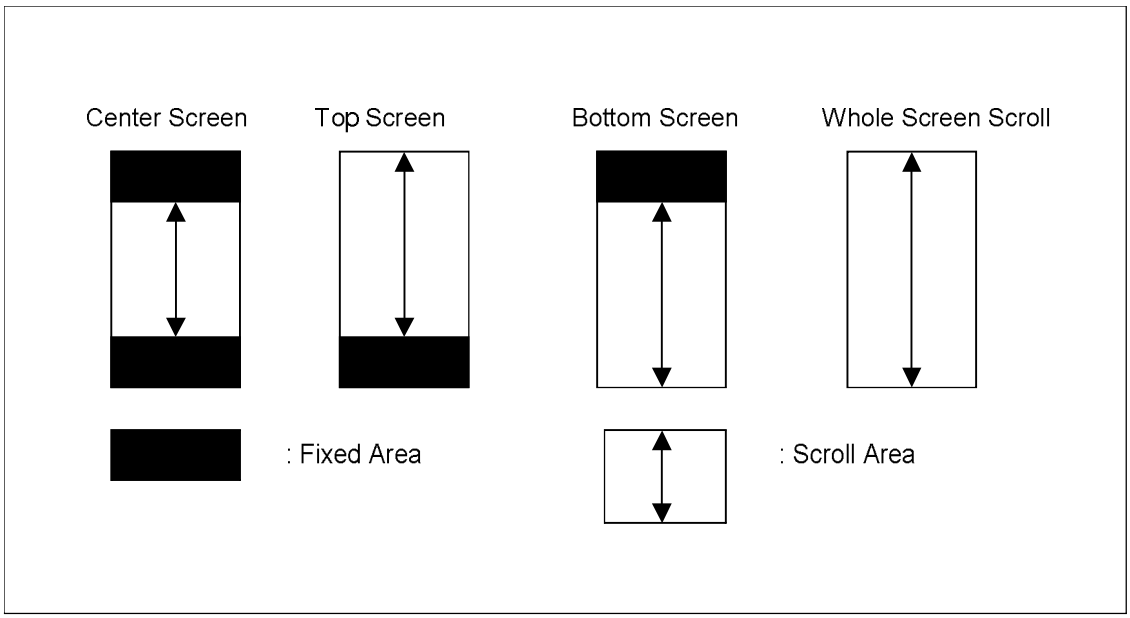


Figure 11 - Area scrolling selection modes

The area scroll function is executed by prompt in the set area scroll command following by changing the start block address by the set scroll start command. Figure 11 illustrates the operation model of the scrolling function.

Example: In the Center screen scroll of 1/48 duty (display range: 48 lines = 12 blocks)

Description	Command	Data
- Set Area Scroll	AAH	
- 8 lines (block 0 & block 1) are specified for the top fixed area		
- The Top Block Address = Number of the top fixed area		
= 8 / 4		02H
- 8 lines (block 15 & block 16) are specified for the bottom fixed area		
- 20 lines (block 10 to block 14) are specified the background areas		
- The Specified Bottom Block Address		
= Bottom Block Address + Number of Background area		
= 9 + (20 / 4) = 14 (0E Hex)		0EH
- 32 lines (block 2 to block 9) are specified the scroll area		
- Number of Specified Block		
= Top fixed area + Scroll Area – 1		
= (8 / 4) + (32 / 4) - 1 = 9 (09 Hex)		09H
- Set area scroll mode – Center screen mode		00H
- Set Scroll start (Scroll range form 02H ~ 0EH)	ABH	
		02H

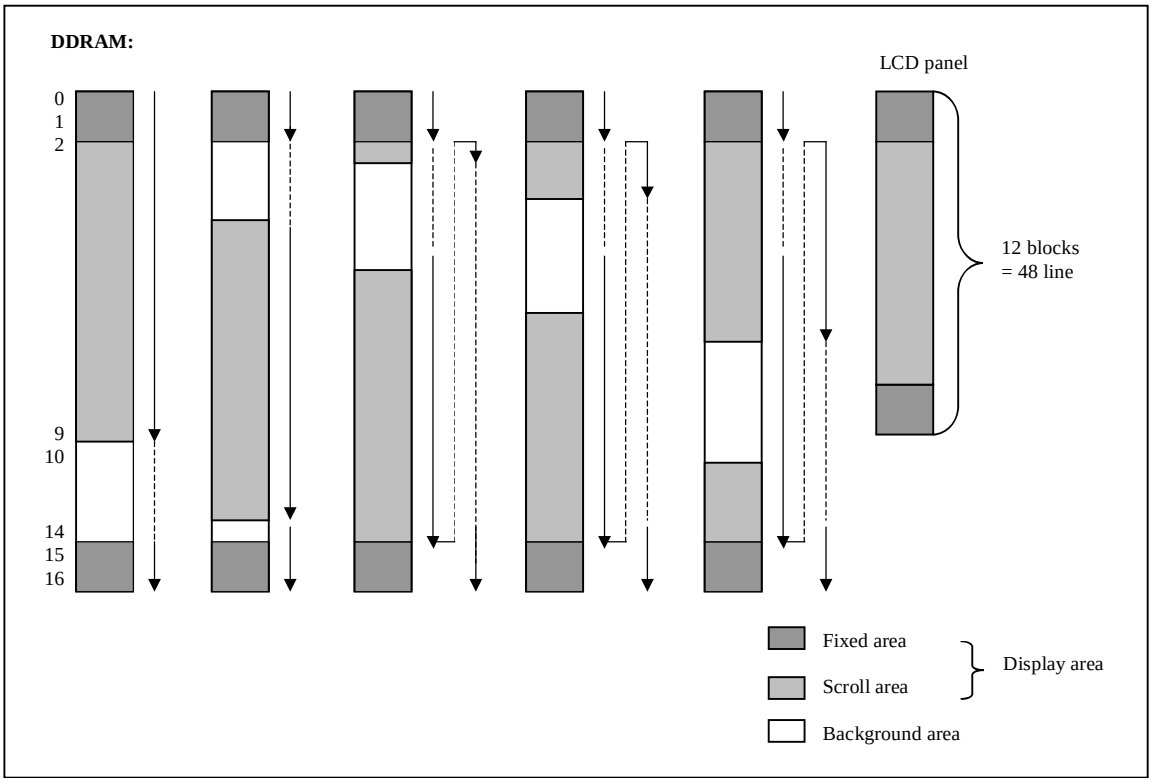
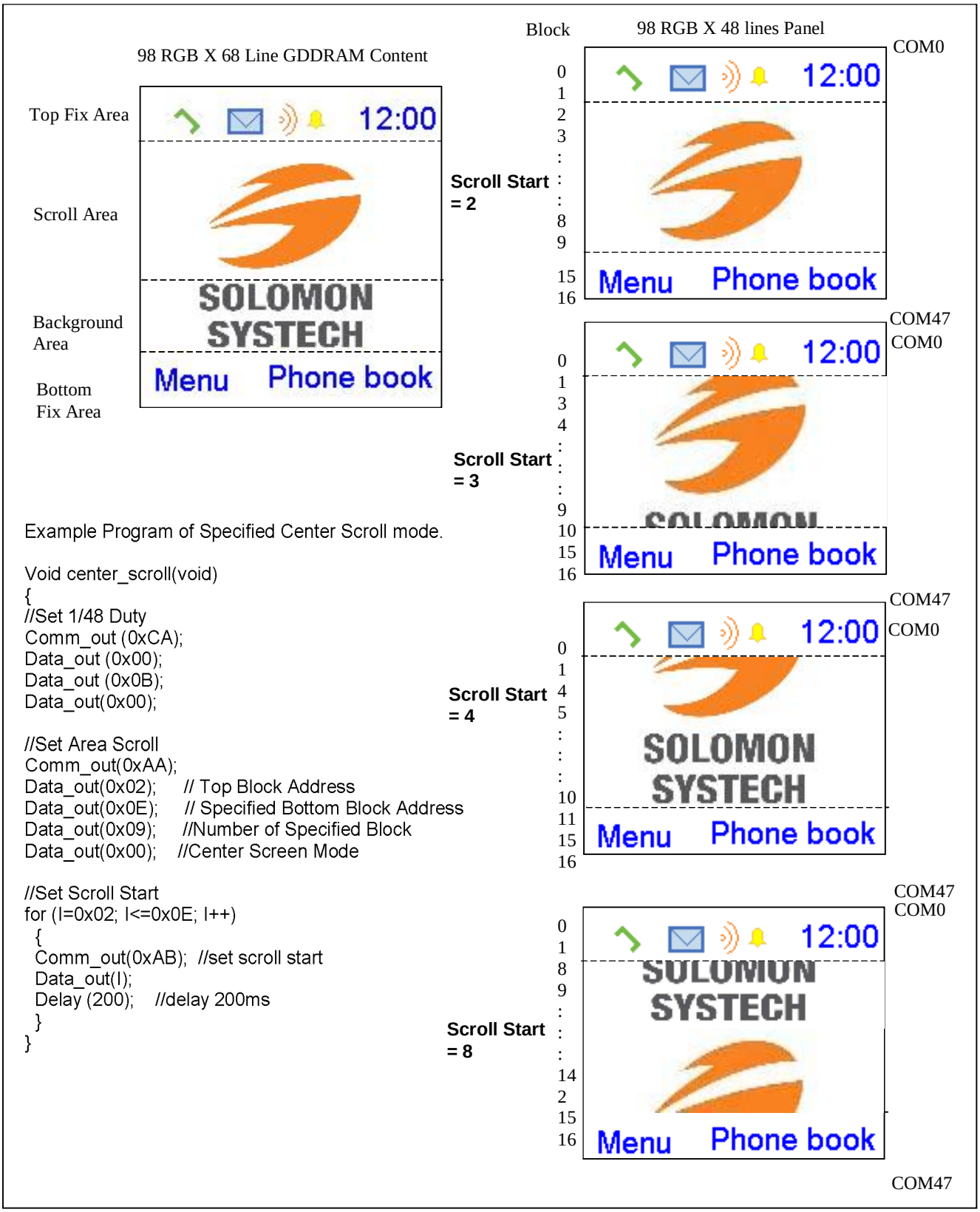


Figure 12 - GDDRAM updates for area scrolling



Example Program of Specified Center Scroll mode.

```
Void center_scroll(void)
{
//Set 1/48 Duty
Comm_out (0xCA);
Data_out (0x00);
Data_out (0x0B);
Data_out(0x00);

//Set Area Scroll
Comm_out(0xAA);
Data_out(0x02);     // Top Block Address
Data_out(0x0E);     // Specified Bottom Block Address
Data_out(0x09);     //Number of Specified Block
Data_out(0x00);    //Center Screen Mode

//Set Scroll Start
for (I=0x02; I<=0x0E; I++)
  {
  Comm_out(0xAB);  //set scroll start
  Data_out(I);
  Delay (200);    //delay 200ms
  }
}
```

Figure 13 – Example of Specified Center Scroll Mode

9.8 Set Scroll Start (AB Hex)

This command specifies the starting block address of the area scrolling and then executes the area scroll by changing the start block address dynamically. Start block < End block must be maintained. Please be noted that the set scroll start command should be executed after the set area scroll command.

9.9 Set Power Control Register (20 Hex)

This command turns on/off the various power circuits associated with the chip. There are three power sub-circuits (reference voltage generator, internal regulator and voltage follower) could be turned on/off by this command. In addition, the configuration of the internal primary booster (3X/4X/5X/6X) can be selected by this command.

9.10 Set Contrast Level & Internal Regulator Ratio (81 Hex)

This command adjusts the contrast of the LCD panel by changing the LCD driving voltage, V_{OUT}, provided by the On-Chip power circuits. V_{OUT} is set with 64 steps (6-bit) in the contrast control register by a set of compound commands. Please refer to the Figure 14 for the contrast control process flow diagram.

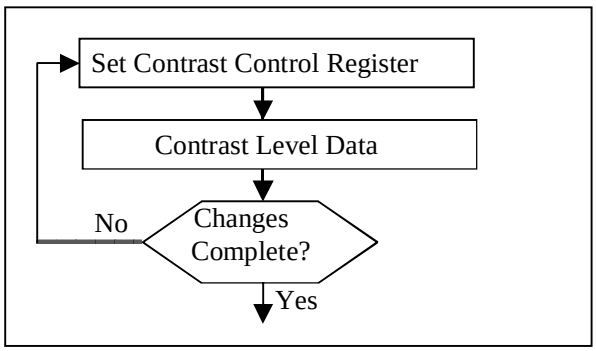


Figure 14 - Contrast Control Flow Set Segment Re-map

This command also sets the feedback gain of the internal regulator. There are altogether 8 internal regulator gains, which are used for the adjustment of V_{OUT} level. This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network. The Contrast Control Voltage Range curves is referred to the following formula:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) * V_{con}$$

$$V_{con} = \left(1 - \frac{63 - \alpha}{210}\right) * V_{ref}$$

$$, where\ Vref = 1.7V$$

Remarks: TC = -0.20%/°C

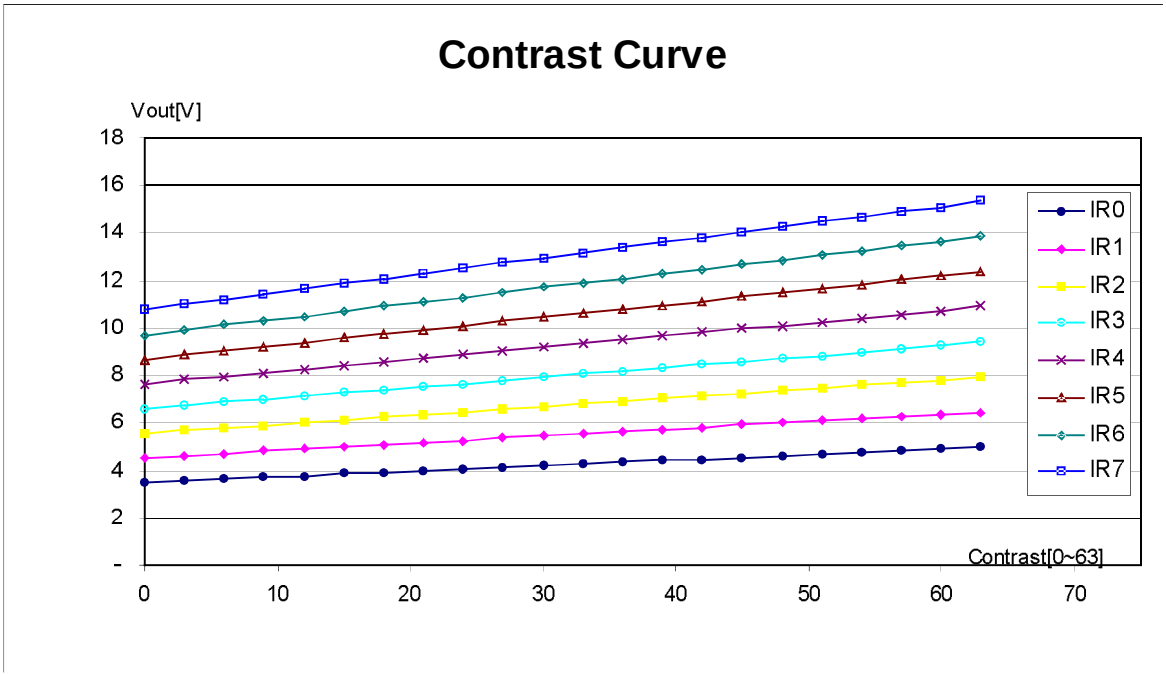


Figure 15 - Contrast Control Voltage Range Curve (VDD=2.7V; VCI=3V; Booster level = 6X; TC = -0.20%/°C)

Note: The Maximum operation voltage of V_{OUT} is 13.5V with panel load.

9.11 Set Increment/Decrement of the contrast set (D6/D7 Hex)

This command can increase the contrast step by +1 and decrease the contrast set by –1. It is the most convenient way to change the contrast of the display by programming.

9.12 Set Normal/Inverse Display (A6/A7 Hex)

For a normally white display panel, after the execution of Normal Display command, image data 000(RGB) indicates black pixel and image data FFF (RGB) indicate white pixel. For a normally black display panel, after the execution of Inverse Display command, image data 000(RGB) indicates Black pixel and image data FFF (RGB) indicate white pixel.

Example:

For a normal White display panel (Set Normal Display: A6 Hex):

RAM Content			Color
R	G	B	
F	F	F	White
0	0	0	Black
F	0	0	Red
0	F	0	Green
0	0	F	Blue

For a normal Black display panel (Set Normal Display: A7 Hex):

RAM Content			Color
R	G	B	
F	F	F	White
0	0	0	Black
F	0	0	Red
0	F	0	Green
0	0	F	Blue

9.13 Enter Partial Display (A8 Hex)

This command and the following parameters specify the display area of the partial display mode. The following figure shows the display and non-display area when the partial display mode is executed.

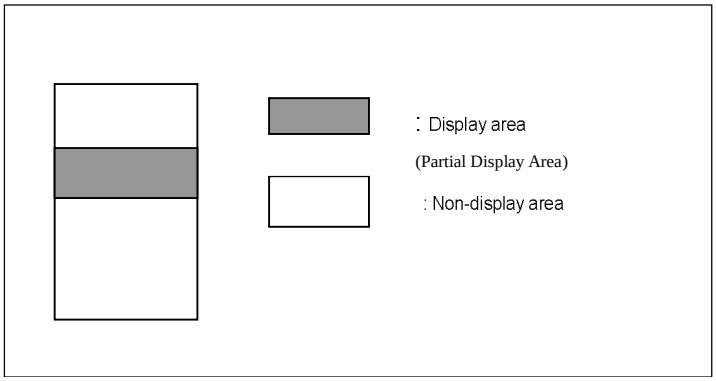


Figure 16 - Partial display mode

9.14 Exit Partial Display (A9 Hex)

This command exits the partial display mode.

9.15 Set Display On/Off (AE/AF Hex)

This command is used to turn the display on or off. When display off is issued with entire display is on, power save mode will be entered.

9.16 Enter/Exit sleep mode (94/95 Hex)

This command enter/exit the sleep mode.

9.17 Enable/Disable the internal oscillator (D1/D2 Hex)

This command enables or disables the internal oscillator. The internal oscillator is turned off after hardware or software reset.

9.18 Set Temperature compensation coefficient (82 Hex)

This command sets the average temperature gradients. Four sets of average temperature gradients can be selected. Please refer to the command table for detail description of the average temperature gradients. The default value of the temperature gradient is –0.2 %/^{0}C

9.19 NOP (25 Hex)

A command causing the chip takes No Operation.

9.20 Write display data mode (5C Hex)

This command is used to execute the write display data mode. The display data byte is directly written to the GDDRAM. Please be noted that the D/$\overline{C}$ signal should be set to high during the display data is written to the GDDRAM.

9.21 Read display data mode (5D Hex)

This command is used to execute the read display data mode. The display data byte is directly read from the GDDRAM. Please be noted that the D/$\overline{C}$ signal should be set to high during the display data is read from to the GDDRAM.

Graphic Command

9.22 Draw Line (83Hex)

Given the starting point (X1, Y1) and the ending point (X2, Y2), a line will be drawn with the color specified.

The following example illustrates the line drawing procedure.

1. Enter the "draw line mode" by execute the command 83H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 01H
5. Set the finishing Y-coordinates, Y2. E.g., 01H
6. Set the color to RGB = (0,1,0) e.g., 0FH following by 00H

Result: A color line will be drawn between coordinates (0,0) and (1,1)

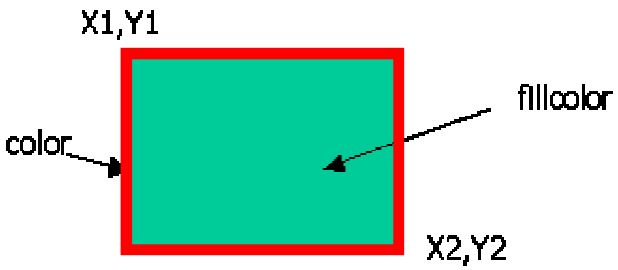
Remarks: X1 ≤97; Y1 ≤67; X2 ≤97; Y2 ≤67

9.23 Fill Enable/Disable (92 Hex)

This command allows the fill color option to be enabled or disabled. This command is applicable to the Draw Rectangle feature. When the selection bit is "0", the fill color option is disabled. When the selection bit is "1", the fill color option is enabled.

9.24 Draw rectangle (84 Hex)

Given the starting point (X1, Y1) and the ending point (X2, Y2), specify the width and height of a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.



The following example illustrates the rectangle drawing procedure.

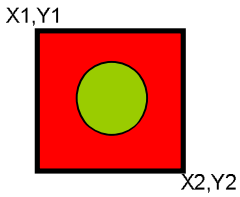
1. Enter the "draw rectangle mode" by execute the command 8AH
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 02H
5. Set the finishing Y-coordinates, Y2. E.g., 02H
6. Set the color to RGB = (1,0,0) e.g., F0H following by 00H
7. Set the filled color to RGB = (0,1,0) e.g., 0FH following by 00H

Result: A filled color square will be drawn with the coordinates of the top left hand corner at (0,0) and the coordinates of the bottom right hand corner at (2,2)

Remarks: X1 ≤X2; Y1 ≤Y2; X2 ≤97; Y2 ≤67

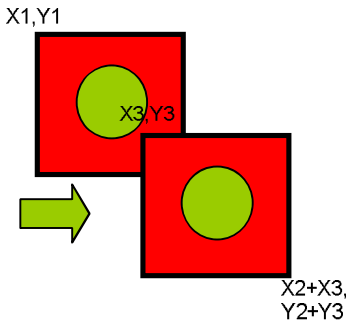
9.25 Copy (8A Hex)

Copy the rectangular region defined by the starting point (X1, Y1) and the ending point (X2, Y2) to location (X3, Y3). There are two possible results with the command copy executed depending on the setting of the start point coordinates and end point coordinates.
The following example illustrates the copy procedure.

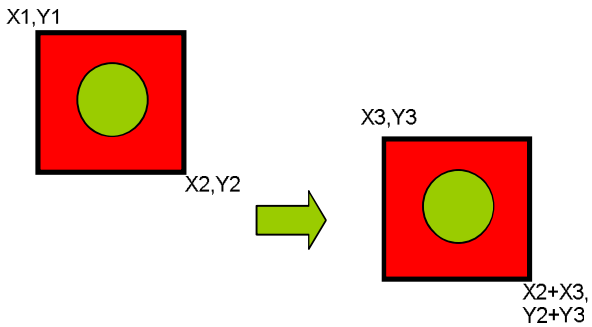


Case 1 – The overlap region will superimpose.

1. Enter the "copy mode" by execute the command 84H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 02H
5. Set the finishing Y-coordinates, Y2. E.g., 02H
6. Set the New X-coordinates, X3. E.g., 01H
7. Set the New Y-coordinates, Y3. E.g., 01H



Case 2 – The original content remains unchanged



1. Enter the "copy mode" by execute the command 84H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 01H
5. Set the finishing Y-coordinates, Y2. E.g., 01H
6. Set the New X-coordinates, X3. E.g., 09H
7. Set the New Y-coordinates, Y3. E.g., 09H

Remarks: X1 ≤ X2; Y1 ≤ Y2; X2 ≤ 97; Y2 ≤ 67

9.26 Dim Window (8C Hex)

This command will dim the window area specify by starting point (X1, Y1) and the ending point (X2, Y2). After the execution of this command, the selected window area will be dimmed by 75% white. Additional execution of this command over the same window area will not change the data content.
Remarks: X1 ≤ X2; Y1 ≤ Y2; X2 ≤ 97; Y2 ≤ 67

9.27 Clear Window (8E Hex)

This command sets the window area specify by starting point (X1, Y1) and the ending point (X2, Y2) to clear the window display. The contrast of the window will be set to zero.
Remarks: X1 ≤ X2; Y1 ≤ Y2; X2 ≤ 97; Y2 ≤ 67

Extended Command

9.28 Set biasing ratio (FB Hex)

This command selects a suitable bias ratio (1/4 to 1/8) required for driving the particular LCD panel in use.

9.29 Set Frame Frequency (F2 Hex)

This command specifies the frame frequency so as to minimize the flickering due to the ac main frequency. The frequency is set to 78Hz after POR.

9.30 Set N-line inversion (F2 Hex)

Number of line inversion is set by this command for reducing crosstalk noise. 2 to 32-line inversion operations could be selected. At POR, this operation is set to 0110b (7 lines). It should be noted that the total number of mux should NOT be a multiple of the inversion number (n). Or else, some lines will not change their polarity during frame change.

9.31 Set N-line inversion Mode (F2 Hex)

This command specifies the N-line inversion mode. At POR, The polarity will toggle per N-line and each frame, otherwise, the polarity toggle per N-line only.

9.32 Select PWM/FRC (F7 Hex)

This command set the Pulse Width Modulation, Frame Rate Control or mix of FWM & FRC.

9.33 OTP setting and programming (F6/F8 Hex)

OTP (One Time Programming) is a method to adjust V_{OUT}. In order to eliminate the variations of LCD module in term of contrast level, OTP can be used to achieve the best contrast of every LCD modules.

OTP setting and programming should include two major steps. Find the OTP offset and OTP programming as following,

Step 1. Find OTP offset

(1) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(2) Send original initialization routines
(3) Set and display any test patterns
(4) Adjust the contrast value (C:0x81, D:0x00~0x3F, D: 0x00 ~ 0x07) until there is the best visual contrast
(5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x24
OTP offset value = 0x24 - 0x20 = +4
OTP setting command should be (C: 0xF6, D: 0x14, D: 0x0A)

Example 2:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x1B
OTP setting = 0x1B - 0x20 = -5
OTP setting command should be (C:0xF6, D: 0x1B, D: 0x0A)

Step 2. OTP programming

(6) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(7) Enable Oscillator (C: 0xD1) and Exit Sleep Mode (C: 0x94)
(8) Connect an external V_{OUT} by closing SW1 (see diagram below)
(9) Send OTP setting commands that we find in step 1 (C: 0xF6, D: 0x10~0x1F, D: 0x0A)
(10) Send OTP programming command (C: 0xF8)
(11) Wait at least 2 seconds
(12) Disconnect the external Vout by opening SW1
(13) Discharge the capacitor C by closing the switch SW2 and wait for 1 second
(14) Hardware Reset
(15) Verify the result by repeating step 1. (2) – (3)

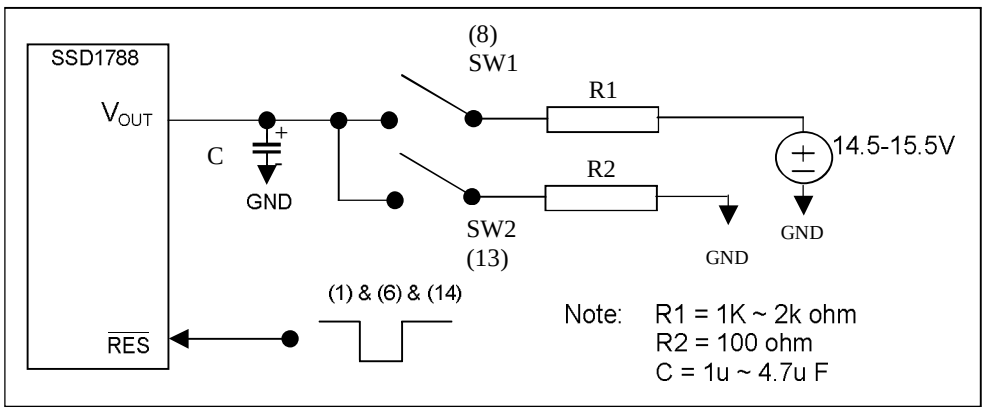


Figure 17 – OTP programming circuitry

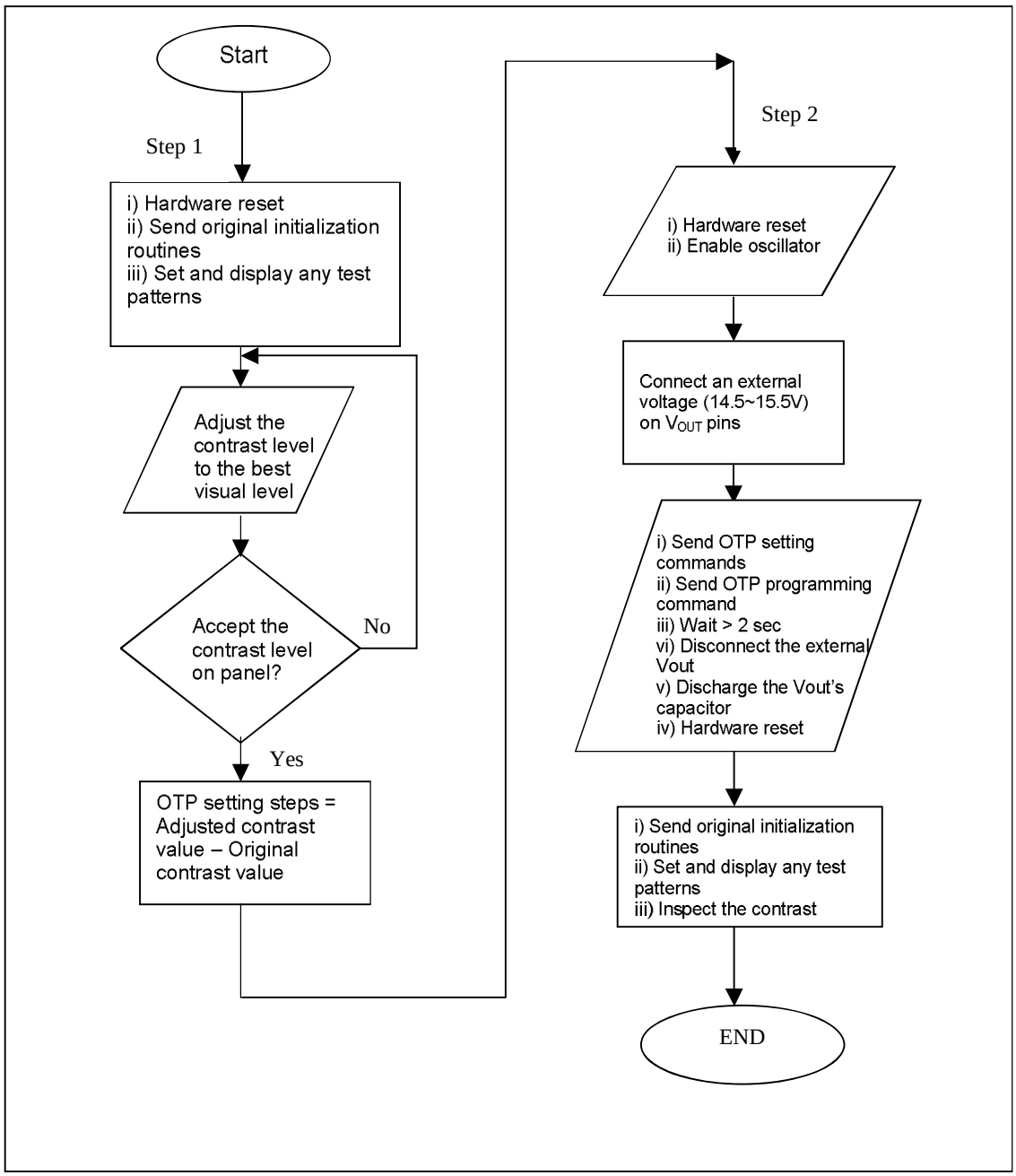


Figure 18 – Flow chart of OTP programming Procedure

OTP Example program

Find the OTP offset:

1. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
2. COMMAND(0XD1); \\Enable oscillator;
   COMMAND(0X94); \\ exit sleep mode;
3. COMMAND(0X0B); \\ turn on the reference voltage generator, internal regulator and voltage follower; Select booster level.
4. COMMAND(0XCA) \\ Set Duty ratio
   DATA(0X10) \\ 68Mux ([68 / 4] –1 = 16(decimal) / 10(Hex))
   COMMAND(0XF7) \\ Set PWM/FRC
   DATA(0X28) \\ pure PWM
   DATA(0X2C)
   DATA(0X05)
   COMMAND(0XFB) \\ Set Biasing ratio
   DATA(0X3) \\ 1/7
5. COMMAND(0X81) \\ Set target gain and contrast.
   DATA(0X14) \\ contrast = 20
   DATA(0X05) \\ IR5 => gain = 7.16
6. \\ Set target display contents
   COMMAND(0X15) \\ set column address
   DATA(0x00) \\ set start column address at 0
   DATA(0X61) \\ set end column address at 97
   COMMAND(0X75) \\ set page address
   DATA(0X00) \\ set start page address at 0
   DATA(0X43) \\ set end page address at 67
   COMMAND(0X5C) \\ write target content to GDDRAM
   DATA(…)
   COMMAND(0xAF) \\ display on
7. OTP offset calculation… target OTP offset value is +3

OTP programming:

8. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
9. COMMAND(0XAB) \\ Enable Oscillator
10. COMMAND(0x94) \\ Exit Sleep Mode
11. Connect a external V_{OUT} (14.5V~15.5V)
12. COMMAND(0XF6) \\ Set OTP offset value to +3 (0011)
    DATA(0X13) \\ 0001 $X_3X_2X_1X_0$, where $X_3X_2X_1X_0$ is the OTP offset value
    DATA(0x0A) \\ Enable the OTP setting
13. COMMAND(0XF8) \\ Send the OTP programming command.
14. Wait at least 2 seconds for programming wait time.
15. Disconnect an external Vout
16. Discharge the Vout's capacitor
17. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin

Verify the result:

18. After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel.

Read Status Command

9.34 Status register read

This command will output the status of the device. The following parameters can be monitored by the status read register.

1. Various area scroll mode
2. Column scan direction
3. Page scan direction
4. Display ON/OFF
5. Sleep mode ON/OFF
6. Display Normal/Inverse
7. Partial display mode ON/OFF

10 MAXIMUM RATINGS

Table 12 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{OUT}		-0.3 to 15	V
V_{CI}	Input Voltage	VSS-0.3 to 4.0	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
Ron	Input Resistance	1000	ohm

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} and Vout be constrained to the range $V_{SS} < V_{DD} \leq V_{CI} < V_{OUT}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Table 13 - DC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.6V, T_A = -40 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	System power supply pins of the logic block Range	Recommend Operating Voltage Possible Operating Voltage	2.4	2.7	3.6	V
V_{DDIO}	System power supply pins of logic block Range	Recommend Operating Voltage Possible Operating Voltage	1.2	-	V_{DD}	V
V_{CI}	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	V_{DD}	-	3.6	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 5X DC-DC , Write accessing, Tcyc =5MHz, Typ. Osc. Freq., Display On, no panel attached.	-	400	1000	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.775V, V_{OUT} = 10.3V, Voltage Generator On, 5X DC-DC Converter Enabled, R/W(WR) Halt, Typ. Osc. Freq., Display On, no panel attached.	-	300	450	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.775V, LCD Driving Waveform Off, Oscillator Off, R/W(WR) halt.	-	2	5	µA
V_{OUT}	LCD Driving Voltage Generator Output (V_{out} Pin) V_{OUT} Converter Efficiency	Display On, Voltage Generator Enabled, DC-DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled. 6X boost, no panel loading	5 93	- 99	13.5 -	V %
V_{REF}	Internal Reference Voltage (T = 25°C) Reference Voltage (T = 25°C) Reference Voltage (T = -20°C) Reference Voltage (T = 70°C)	TC0 = -0.10%/°C TC1 = -0.15%/°C TC2 = -0.20%/°C (POR) TC3 = -0.25%/°C TC2 TC2 TC2	1.64 1.64 1.65 1.65 1.65 1.79 1.50	1.69 1.69 1.70 1.70 1.70 1.85 1.55	1.74 1.74 1.75 1.75 1.75 1.91 1.60	V V V V V V V
V_{OH1}	Logic High Output Voltage	Iout=-100 A	0.9* V_{DDIO}	-	V_{DDIO}	V
V_{OL1}	Logic Low Output Voltage	Iout=100 A	0	-	0.1*V_{DDIO}	V
V_{IH1}	Logic High Input voltage		0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*V_{DDIO}	V
I_{OH}	Logic High Output Current Source	Vout = V_{DD}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
ΔV_{OUT}	Variation of V_{OUT} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-2	0	2	%

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
TC0	Average Temperature Gradient Flat Temperature Coefficient	Voltage Regulator Enabled	0	-0.10	-0.12	%/°C
TC1	Temperature Coefficient 1		-0.12	-0.15	-0.17	%/°C
TC2	Temperature Coefficient 2 (POR)		-0.17	-0.20	-0.22	%/°C
TC3	Temperature Coefficient 3		-0.22	-0.25	-0.27	%/°C

The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref}at50°C - V_{ref}at0°C}{50°C - 0°C} x \frac{1}{V_{ref}at25°C} x100\%$$

12 AC CHARACTERISTICS

Table 14 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.7V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Fosc	Oscillation Frequency of Display Timing Generator for: 68 MUX Mode	Internal Oscillator Enabled (default), VDD = 2.7V	465.12	477.36	489.6	kHz
F_{FRM}	Frame Frequency for: 68 MUX Mode	b. 98 RGB x 68 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., Fext, feeding to CL pin.	76	78	80	Hz

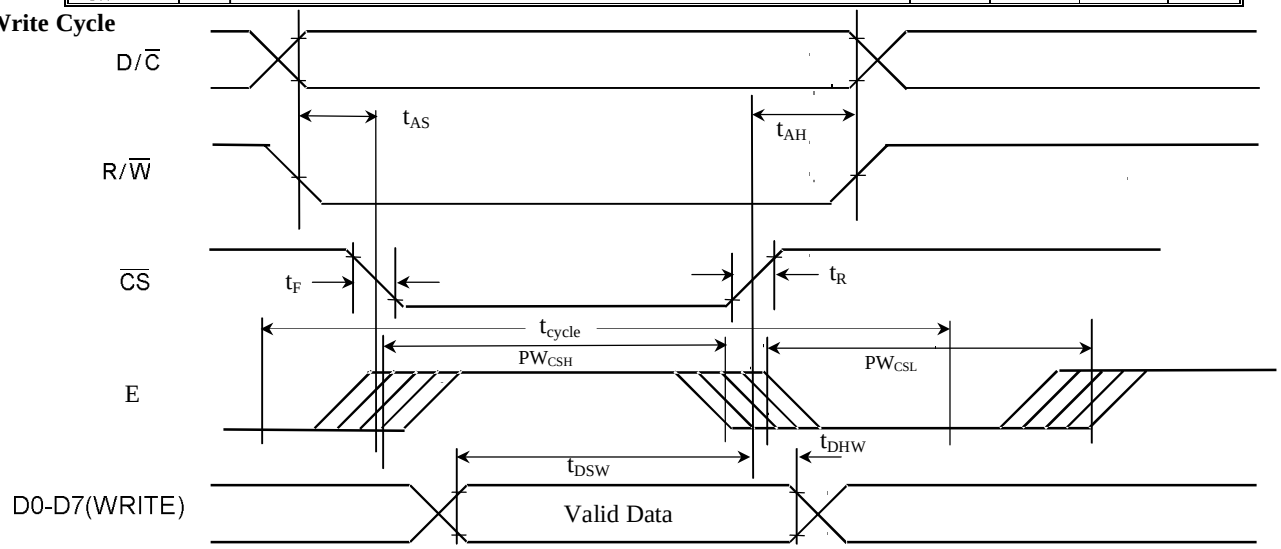
Remarks: Fext stands for the frequency value of external clock feeding to the CL pin
Fosc stands for the frequency value of internal oscillator

Table 15 – Parallel 6800-series Interface Timing Characteristics

(T_A = -40 to 85°C, V_{DD} = 2.6V to 3.6V, V_{DDIO} = 1.2V to V_{DD})

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	130	-	-	ns
PW_{CSL}	Control Pulse Low Width	65	-	-	ns
PW_{CSH}	Control Pulse High Width	65	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	200	ns
t_{OH}	Output Hold time	20	-	60	ns

Write Cycle



The PW_{CSH} timing reference is 50% of the rising / falling edge of E or $\overline{CS}$ pin.

The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of E or $\overline{CS}$ pin.

Read Cycle

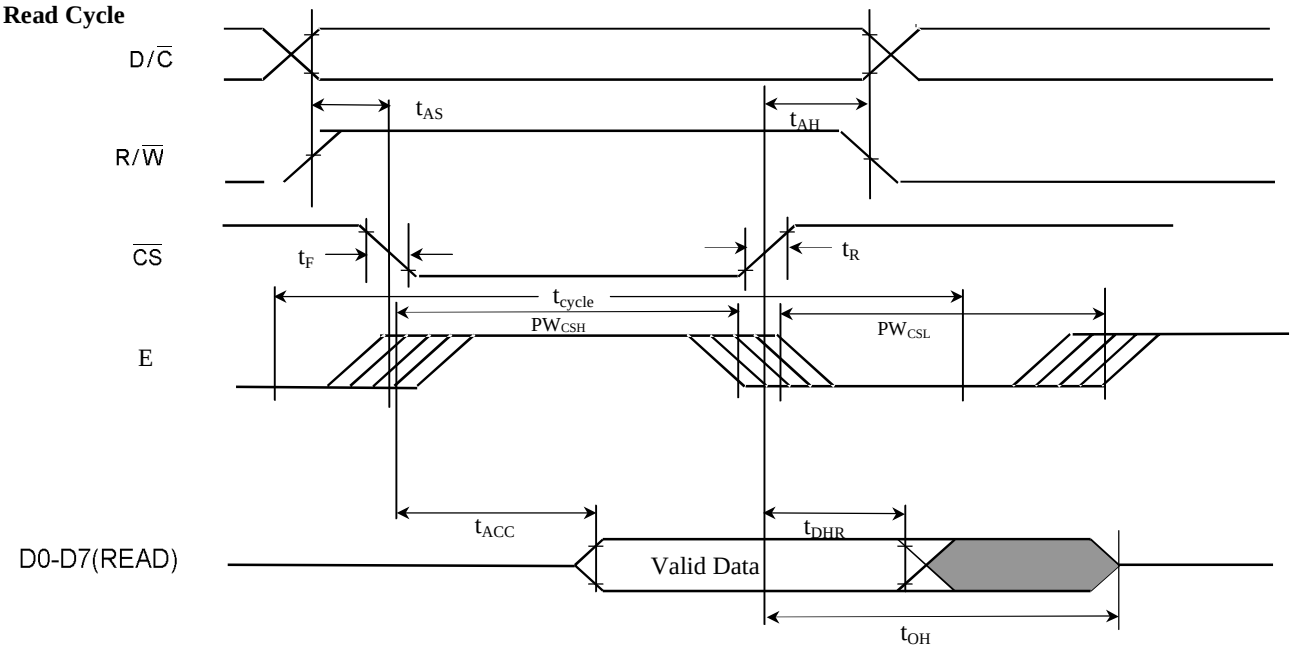


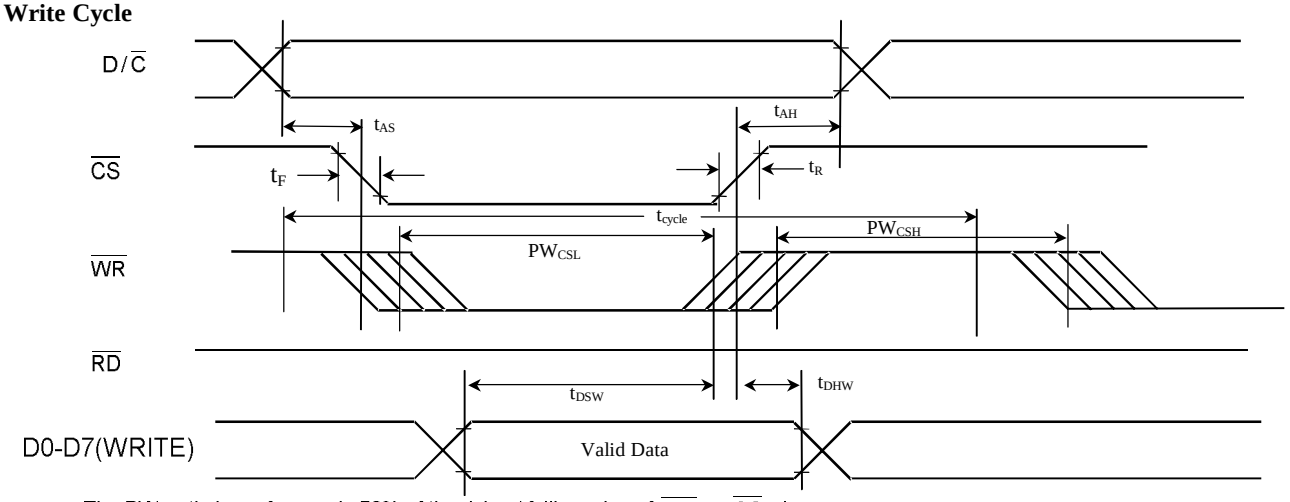
Figure 19 – Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

Table 16 – Parallel 8080-series Interface Timing Characteristics

(T_A = -40 to 85°C, V_{DD} = 2.6V to 3.6V, V_{DDIO} = 1.2V to V_{DD})

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	130	-	-	ns
PW_{CSL}	Control Pulse Low Width	65	-	-	ns
PW_{CSH}	Control Pulse High Width	65	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns

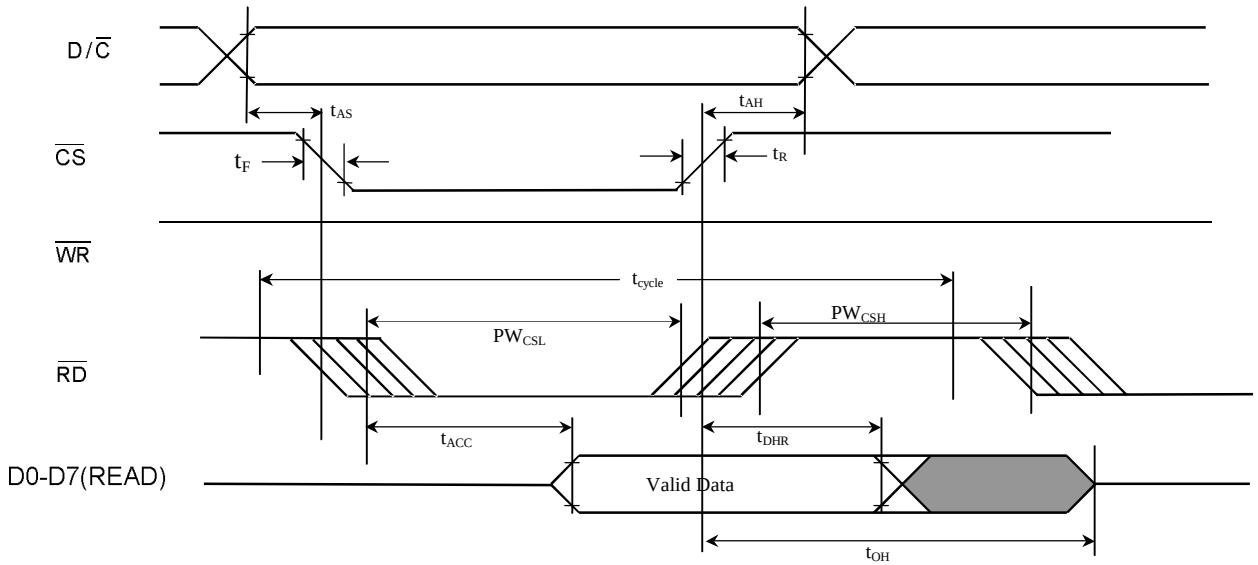
Write Cycle



The PW_{CSL} timing reference is 50% of the rising / falling edge of $\overline{WR}$ or $\overline{CS}$ pin.

The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of $\overline{WR}$ or $\overline{CS}$ pin.

Read Cycle



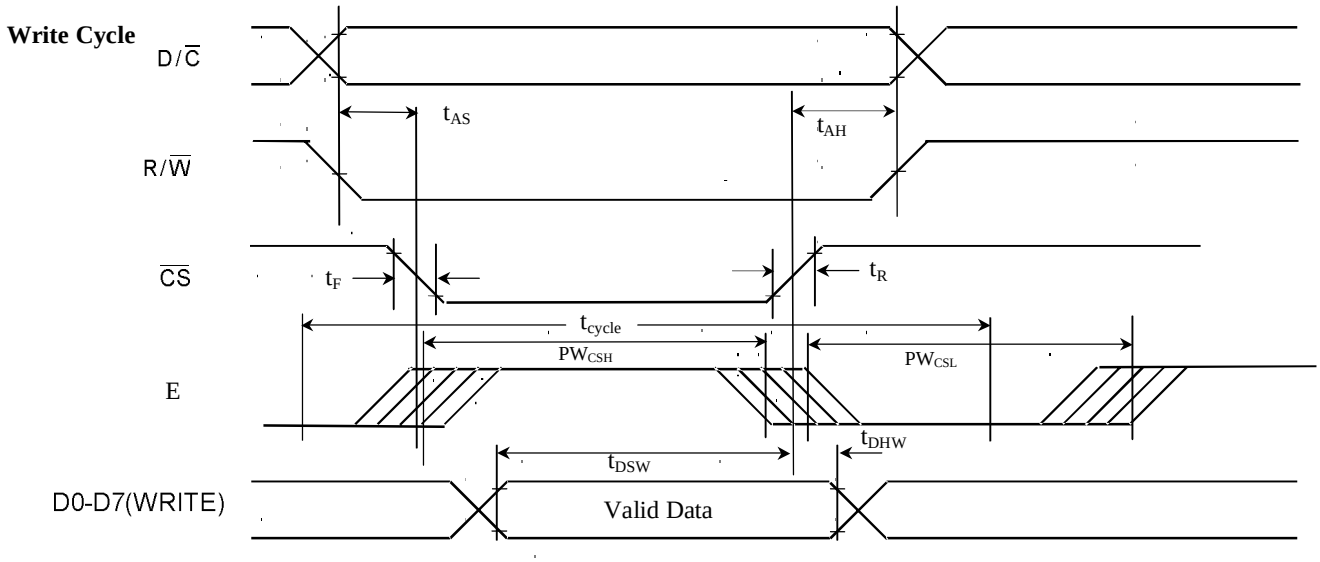
The PW_{CSL} timing reference is 50% of the rising / falling edge of $\overline{RD}$ or $\overline{CS}$ pin.

The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of $\overline{RD}$ or $\overline{CS}$ pin.

Figure 20 – Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

Table 17 – Parallel 6800-series Interface Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V, V_{DDIO} = 1.2V to V_{DD})

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	250	-	-	ns
PW_{CSL}	Control Pulse Low Width	125	-	-	ns
PW_{CSH}	Control Pulse High Width	125	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns



The PW_{CSH} timing reference is 50% of the rising / falling edge of E or $\overline{CS}$ pin.
The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of E or $\overline{CS}$ pin.

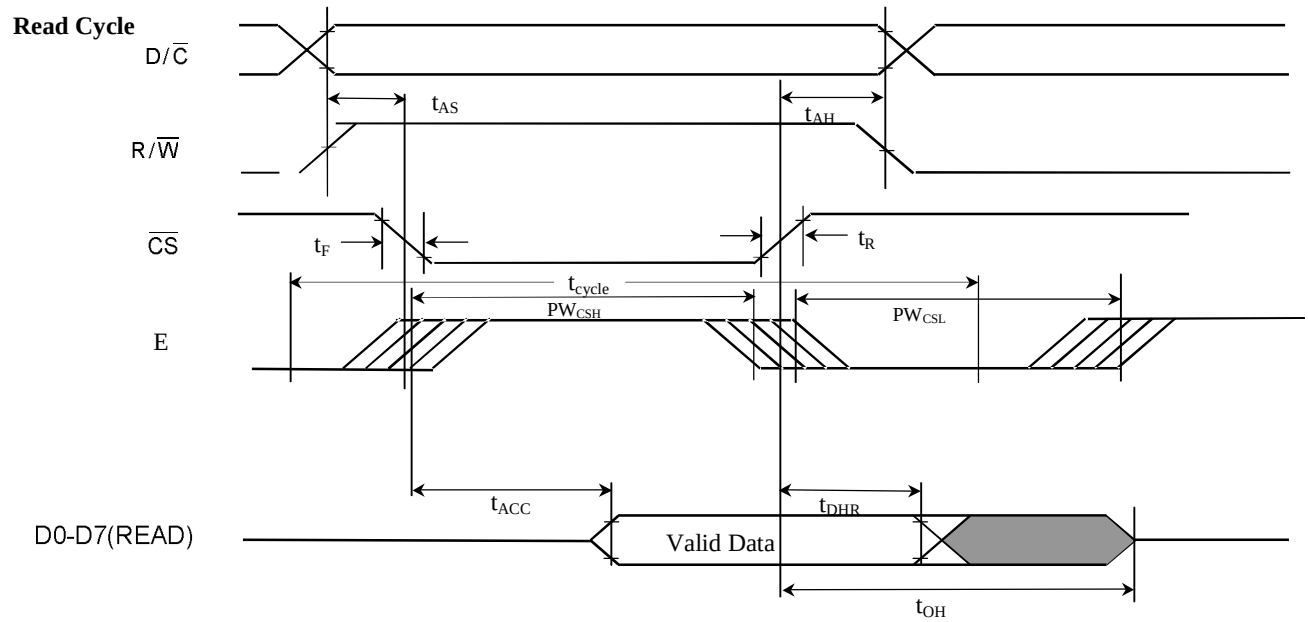
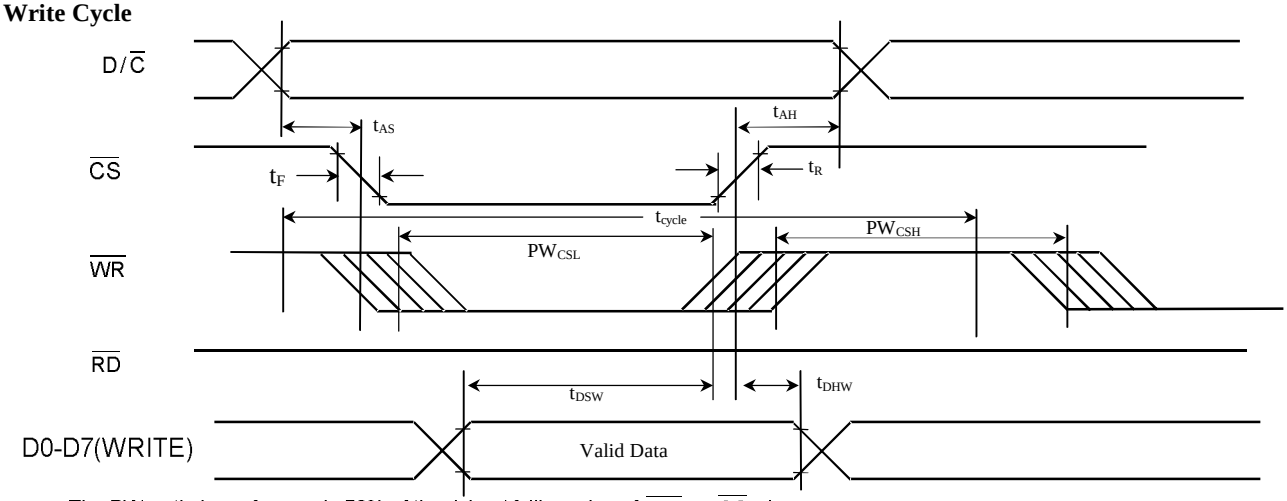


Figure 21 – Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

Table 18 – Parallel 8080-series Interface Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V, V_{DDIO} = 1.2V to V_{DD})

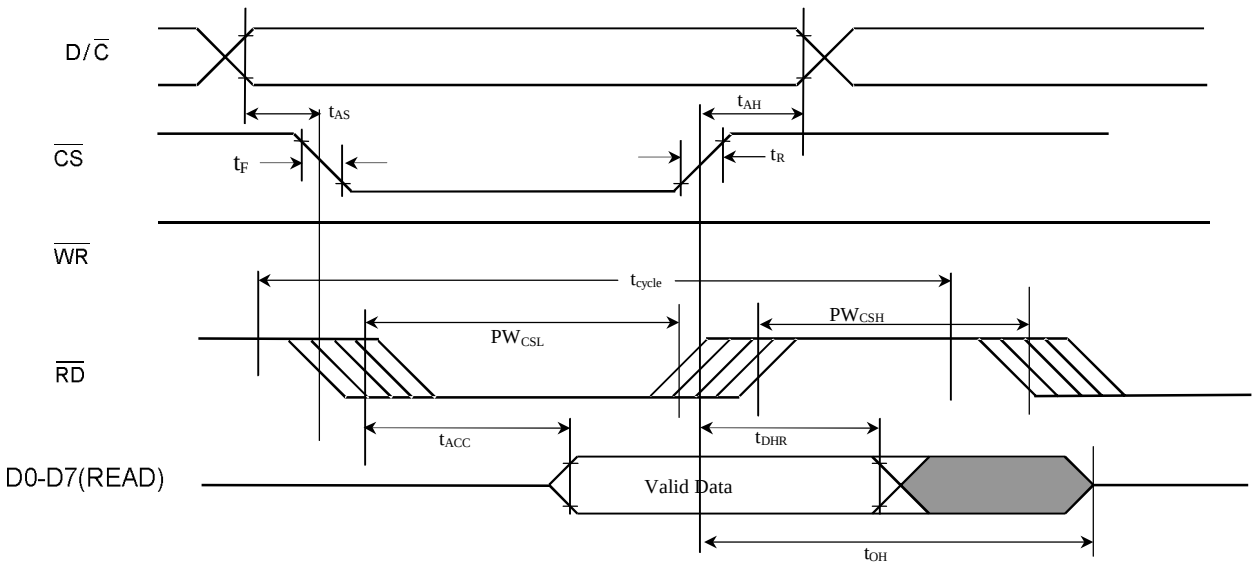
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	250	-	-	ns
PW_{CSL}	Control Pulse Low Width	125	-	-	ns
PW_{CSH}	Control Pulse High Width	125	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns

Write Cycle



The PW_{CSL} timing reference is 50% of the rising / falling edge of $\overline{WR}$ or $\overline{CS}$ pin.
The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of $\overline{WR}$ or $\overline{CS}$ pin.

Read Cycle



The PW_{CSL} timing reference is 50% of the rising / falling edge of $\overline{RD}$ or $\overline{CS}$ pin.
The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of $\overline{RD}$ or $\overline{CS}$ pin.

Figure 22 – Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

Table 19 – 4-Wires Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.6V, V_{DDIO} = 1.2V to V_{DD})

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	20	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

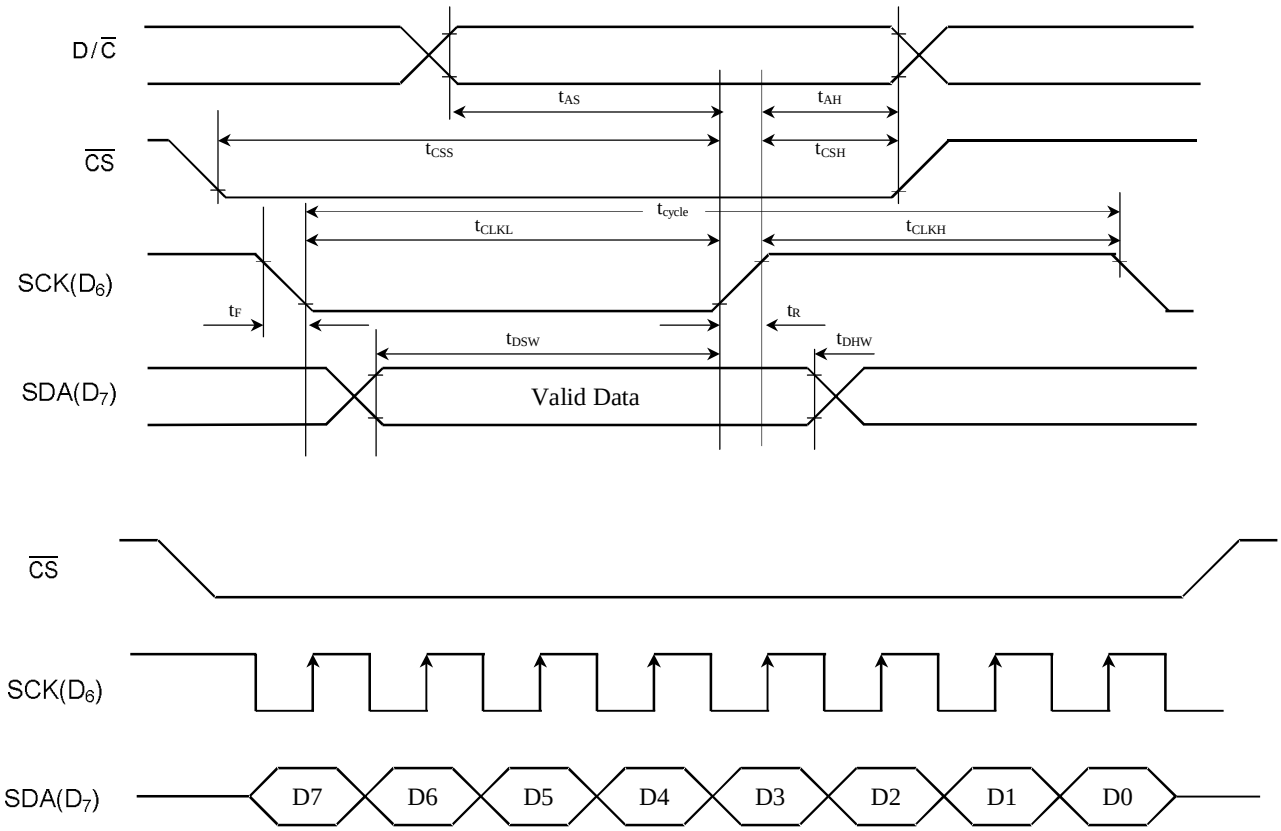


Figure 23 – 4-Wires Serial Timing Characteristics (PS0 = L, PS1 =L)

Table 20 – 3-Wires Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.6V, V_{DDIO} = 1.2V to V_{DD})

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	20	MHz
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	30	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns

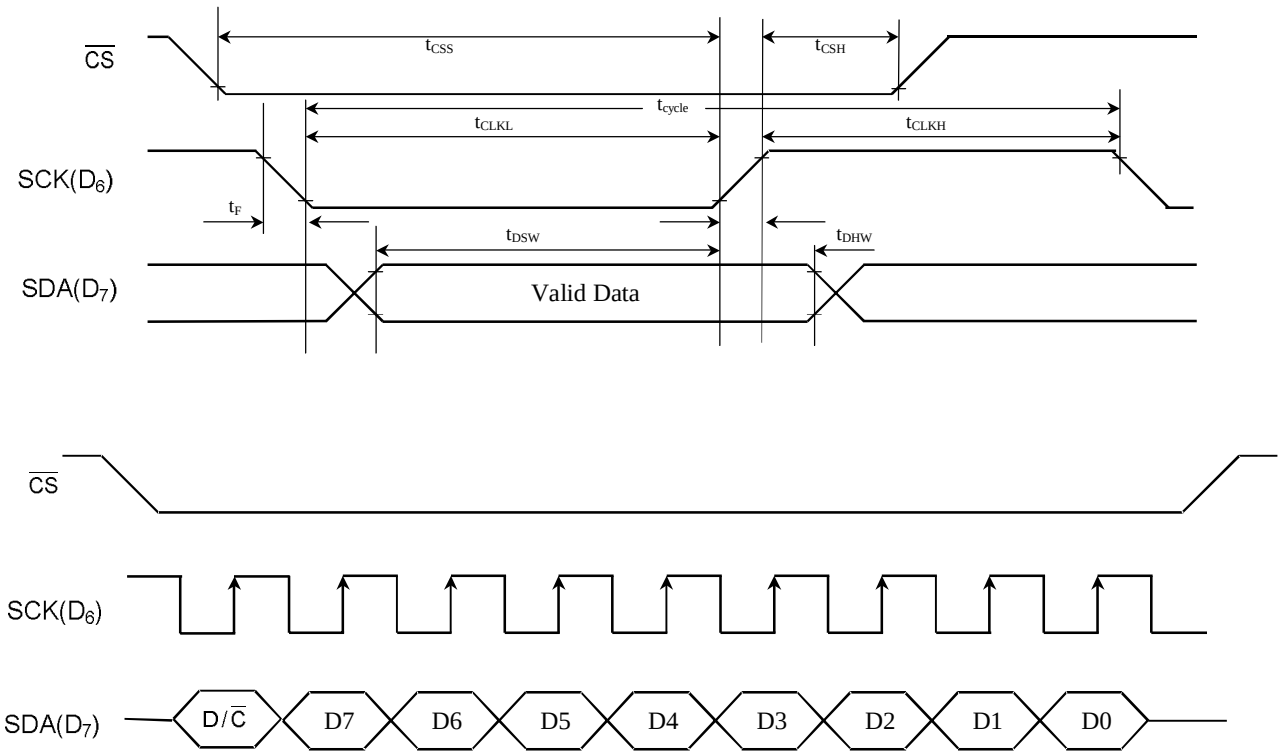


Figure 24 – 3-Wires Serial Timing Characteristics (PS0 = L, PS1 =H)

Table 21 – 4-Wires Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V, V_{DDIO} = 1.2V to V_{DD})

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	60	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	16.6	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

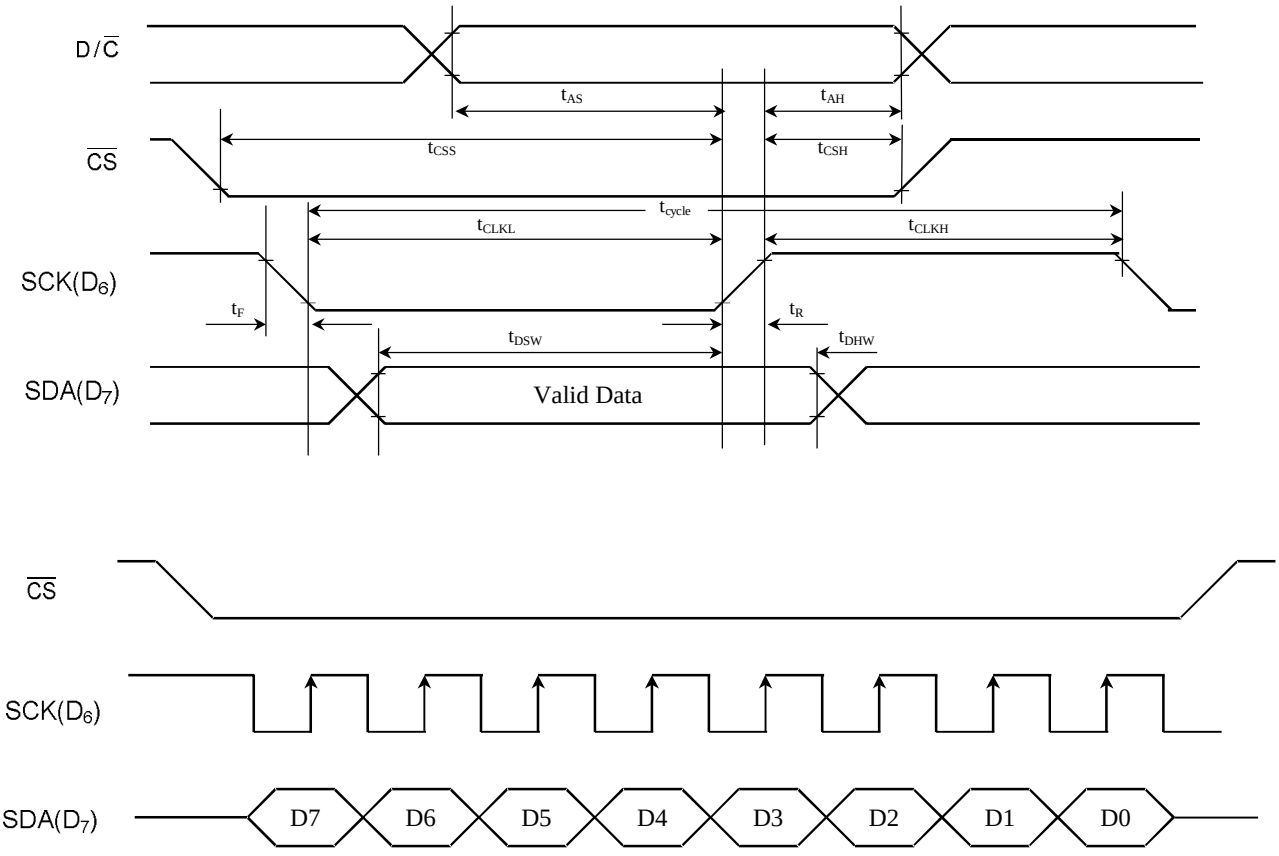


Figure 25 – 4-Wires Serial Timing Characteristics (PS0 = L, PS1 =L)

Table 22 – 3-Wires Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V, V_{DDIO} = 1.2V to V_{DD})

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	60	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	16.6	MHz
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	30	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns

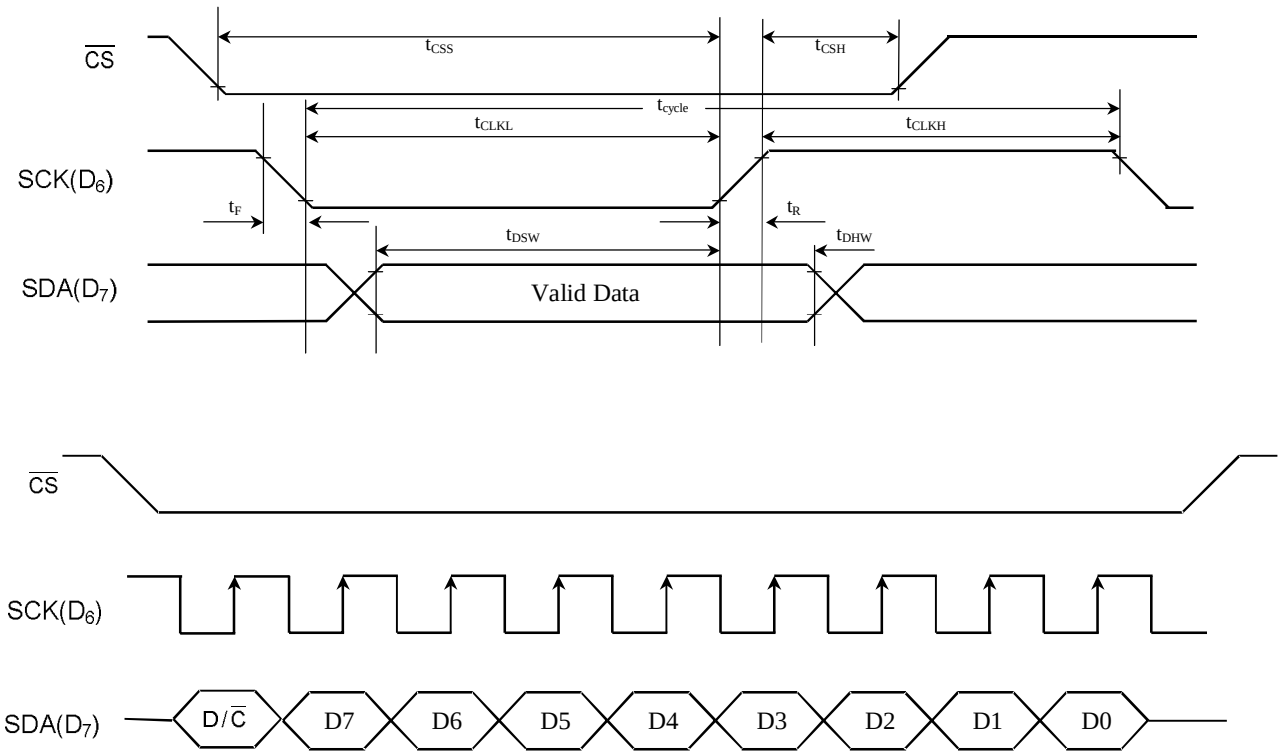


Figure 26 – 3- Wires Serial Timing Characteristics (PS0 = L, PS1 =H)

Table 23 – Power Up/Down Timing Characteristics (TA = -40 to 85°C, VDD = 2.4V to 3.6V, V_{DDIO} = 1.2V to V_{DD})

Symbol	Parameter	Min	Typ	Max	Unit
t_{PR}	Power rise time	-	-	30	us
t_{PD}	Power delay time	-	-	30	us
t_{STABLE}	Chip stable time	-	-	10	us
t_{RES}	Reset pulse	10	-	-	us
t_{READY}	Chip need time after hardware reset	-	-	1	us

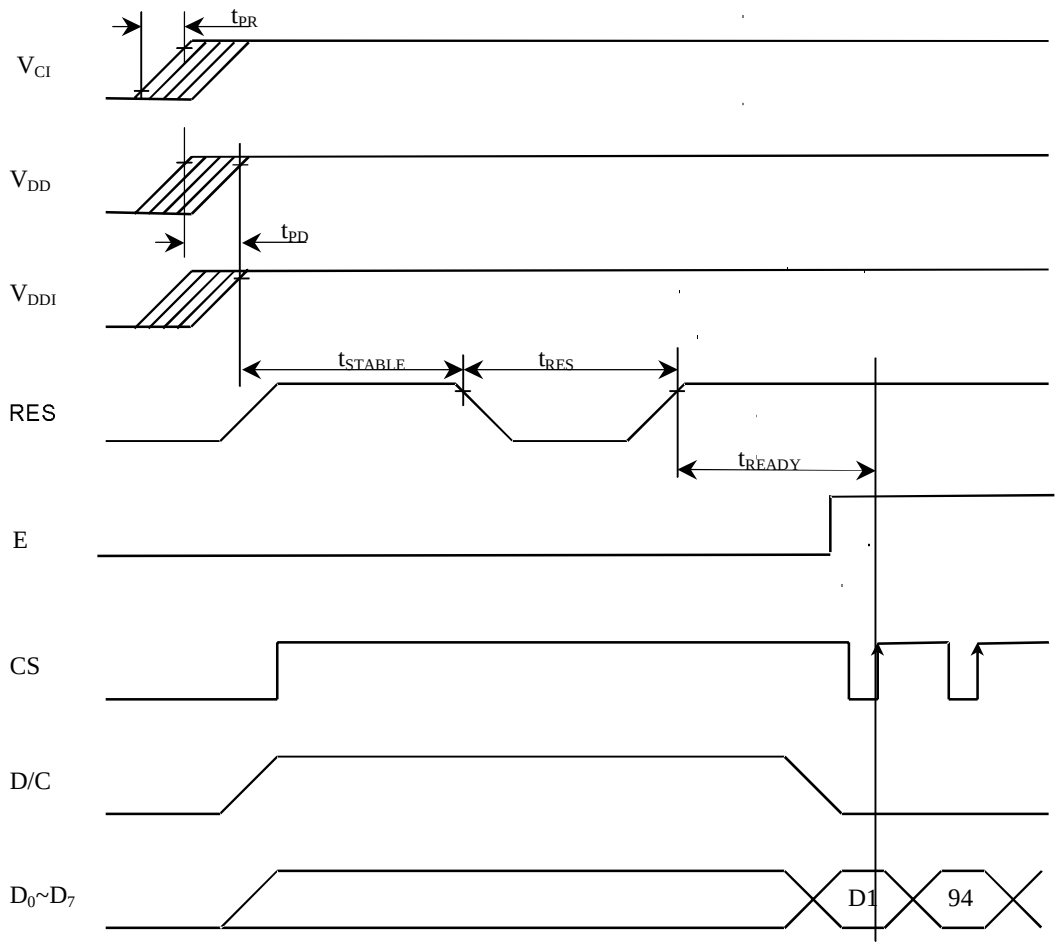


Figure 27 – Power Up

Symbol	Parameter	Min	Typ	Max	Unit
t_{CHARGE}	V_{OUT} Charge up wait time (charge up to 11.7V)	50	-	-	ms
t_{PDOWN}	Power Hold time	50	-	-	ms

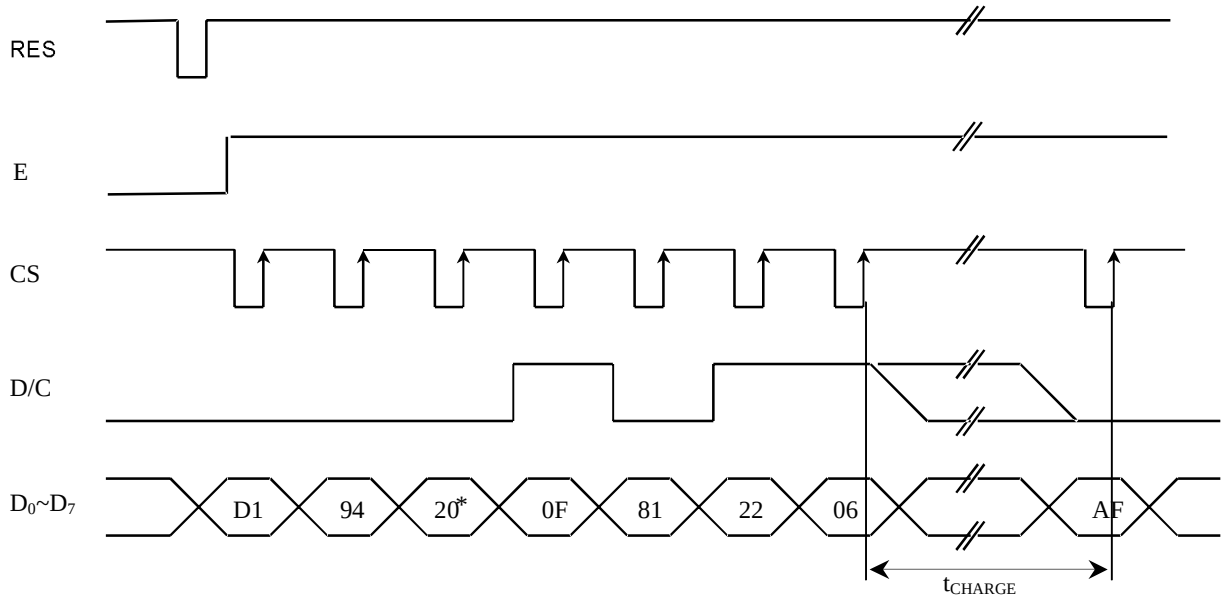
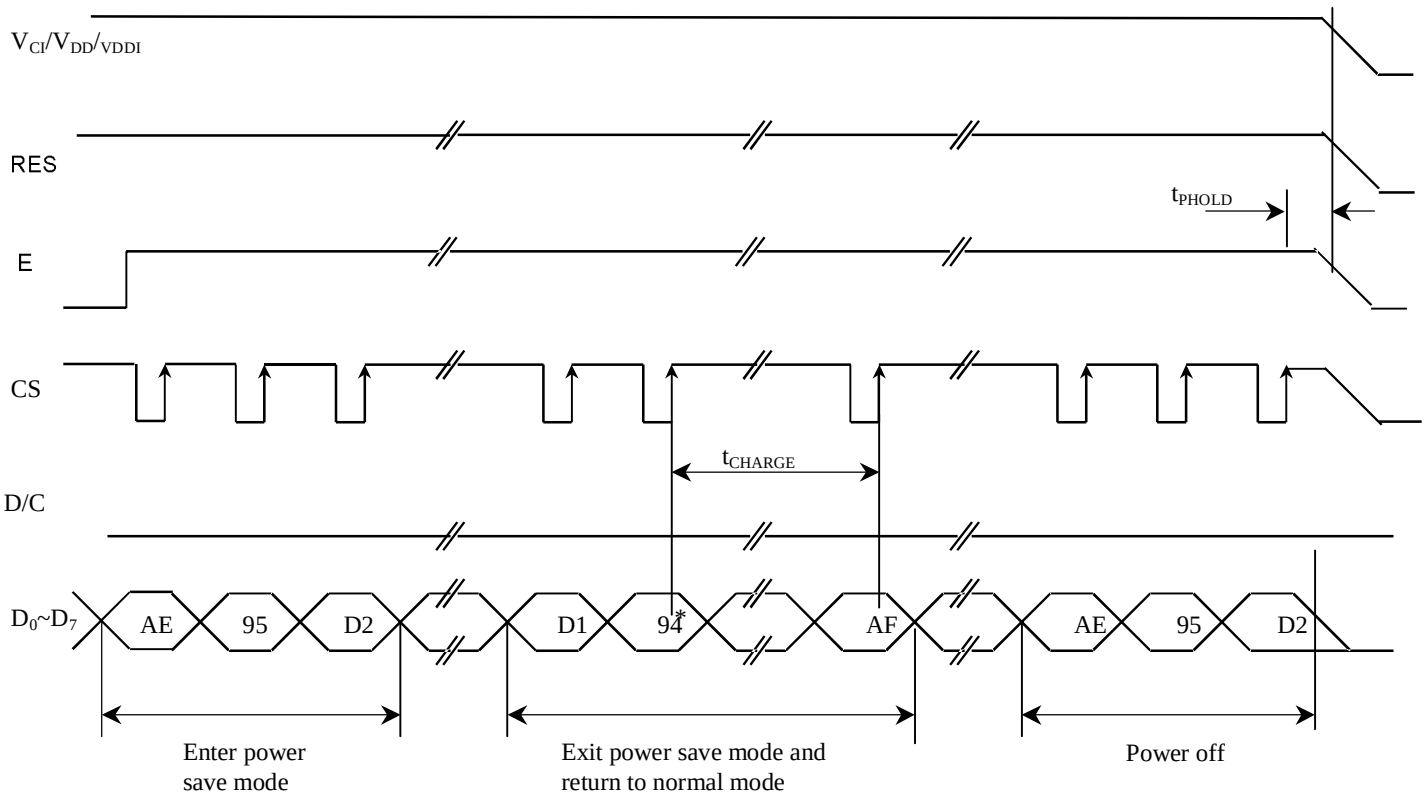


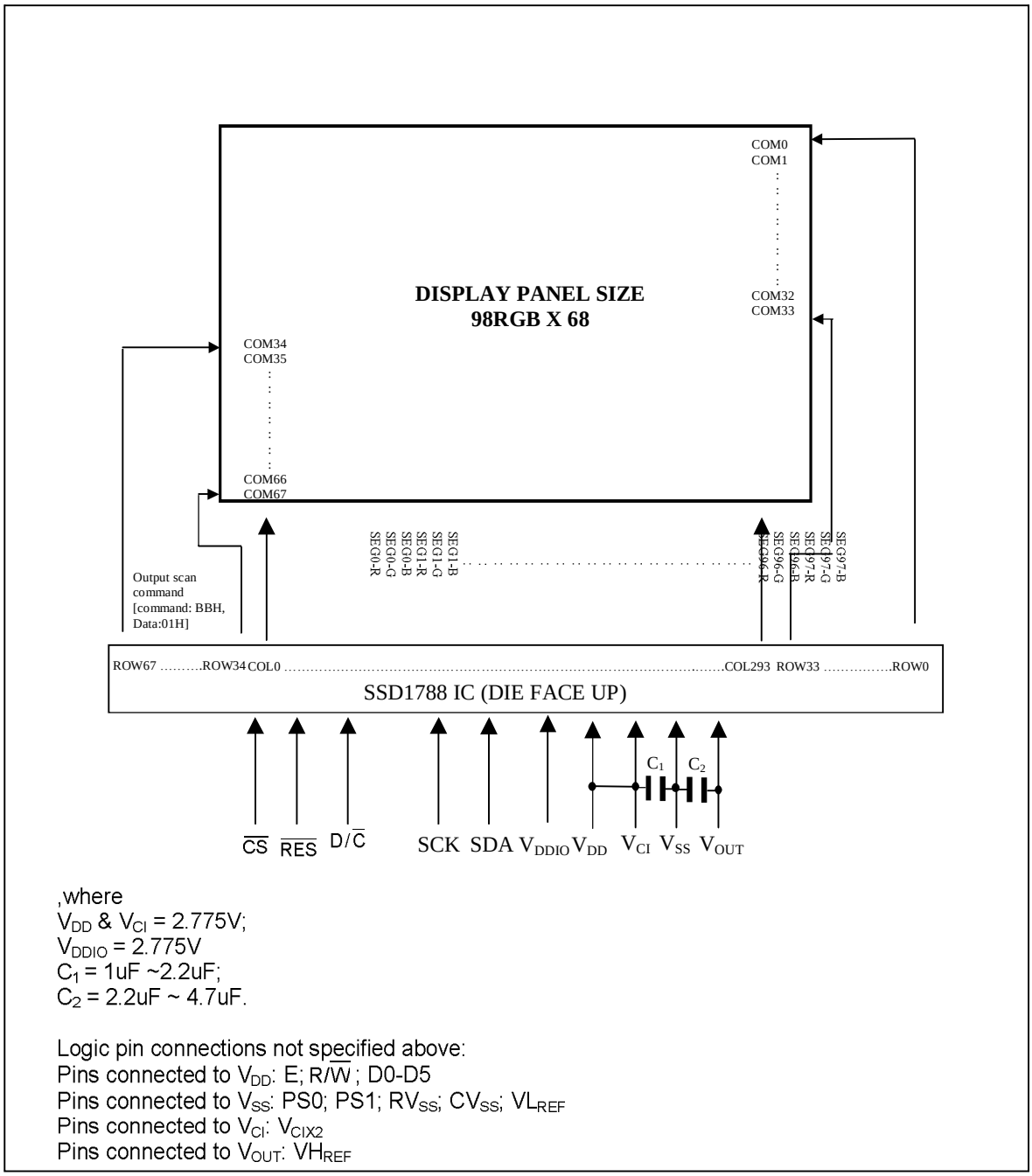
Figure 28 – Initial Code Timing Chart



- *After enable Booster & Regulator circuitry, there has 200ms mask off period that is used to provide a wait time to charge up V_{OUT} capacitor. Within the mask off period, SEG doesn't have output waveform.*

Figure 29 – Power save / power up / power off timing chart

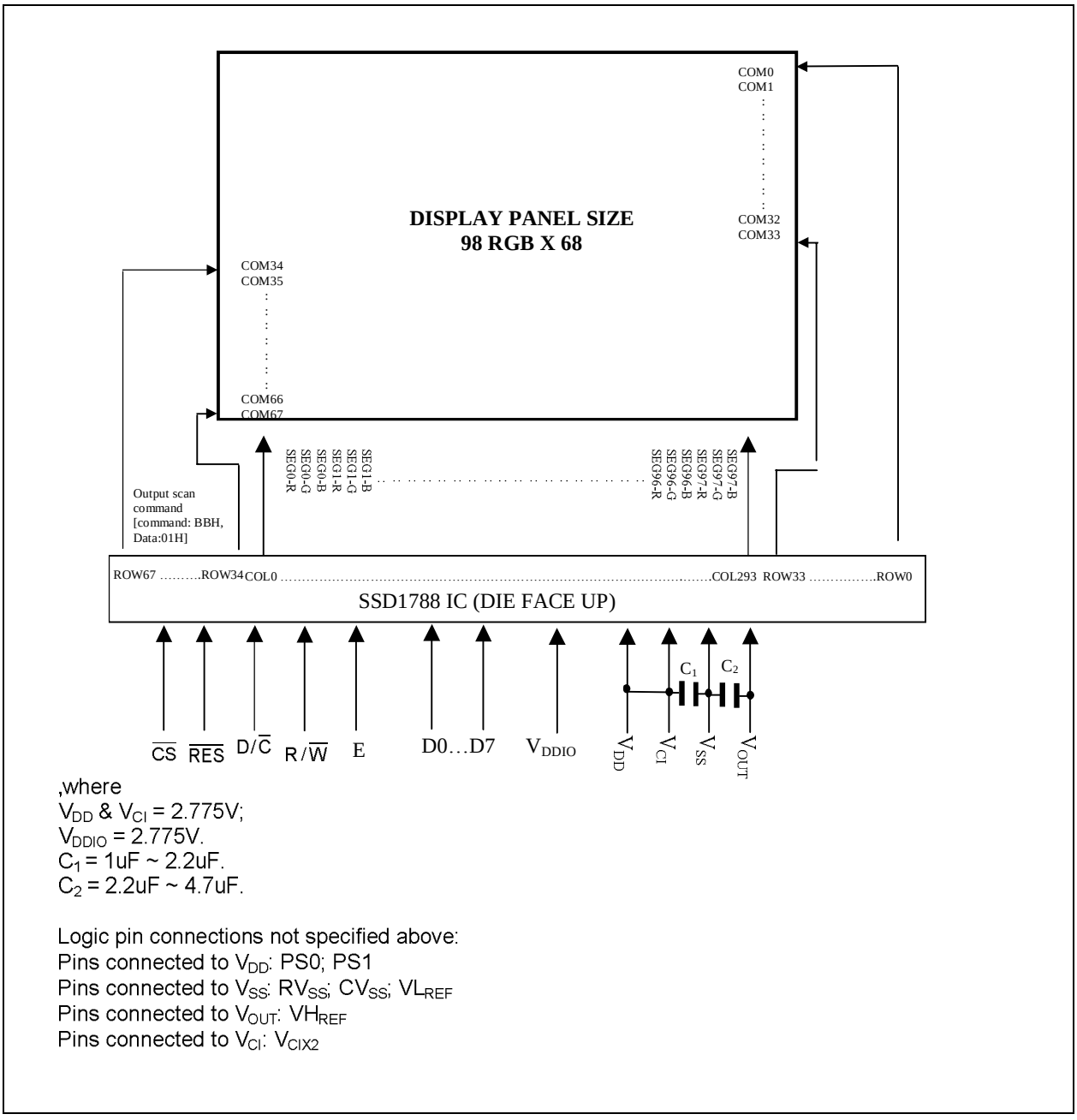
13 APPLICATION EXAMPLES



,where
V_{DD} & V_{CI} = 2.775V;
V_{DDIO} = 2.775V
C_1 = 1uF ~2.2uF;
C_2 = 2.2uF ~ 4.7uF.

Logic pin connections not specified above:
Pins connected to V_{DD}: E; R/$\overline{W}$; D0-D5
Pins connected to V_{SS}: PS0; PS1; RV_{SS}; CV_{SS}; VL_{REF}
Pins connected to V_{CI}: V_{CIX2}
Pins connected to V_{OUT}: VH_{REF}

Figure 30 - Application Examples I (4-wires SPI mode)



,where
V_{DD} & V_{CI} = 2.775V;
V_{DDIO} = 2.775V.
C_1 = 1uF ~ 2.2uF.
C_2 = 2.2uF ~ 4.7uF.

Logic pin connections not specified above:
Pins connected to V_{DD}: PS0; PS1
Pins connected to V_{SS}: RV_{SS}; CV_{SS}; VL_{REF}
Pins connected to V_{OUT}: VH_{REF}
Pins connected to V_{CI}: V_{CIX2}

Figure 31 - Application Examples II (6800 PPI mode)

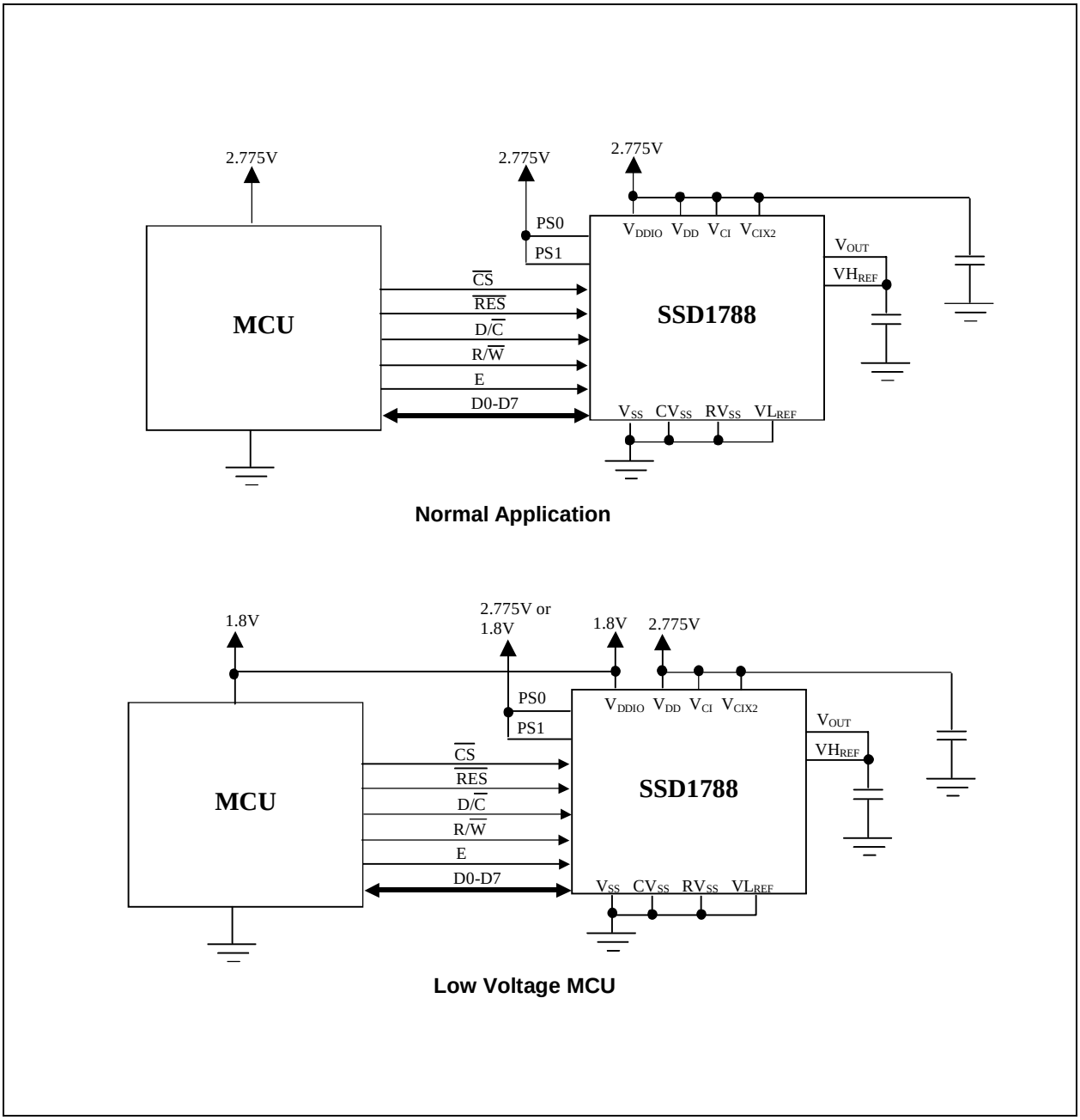
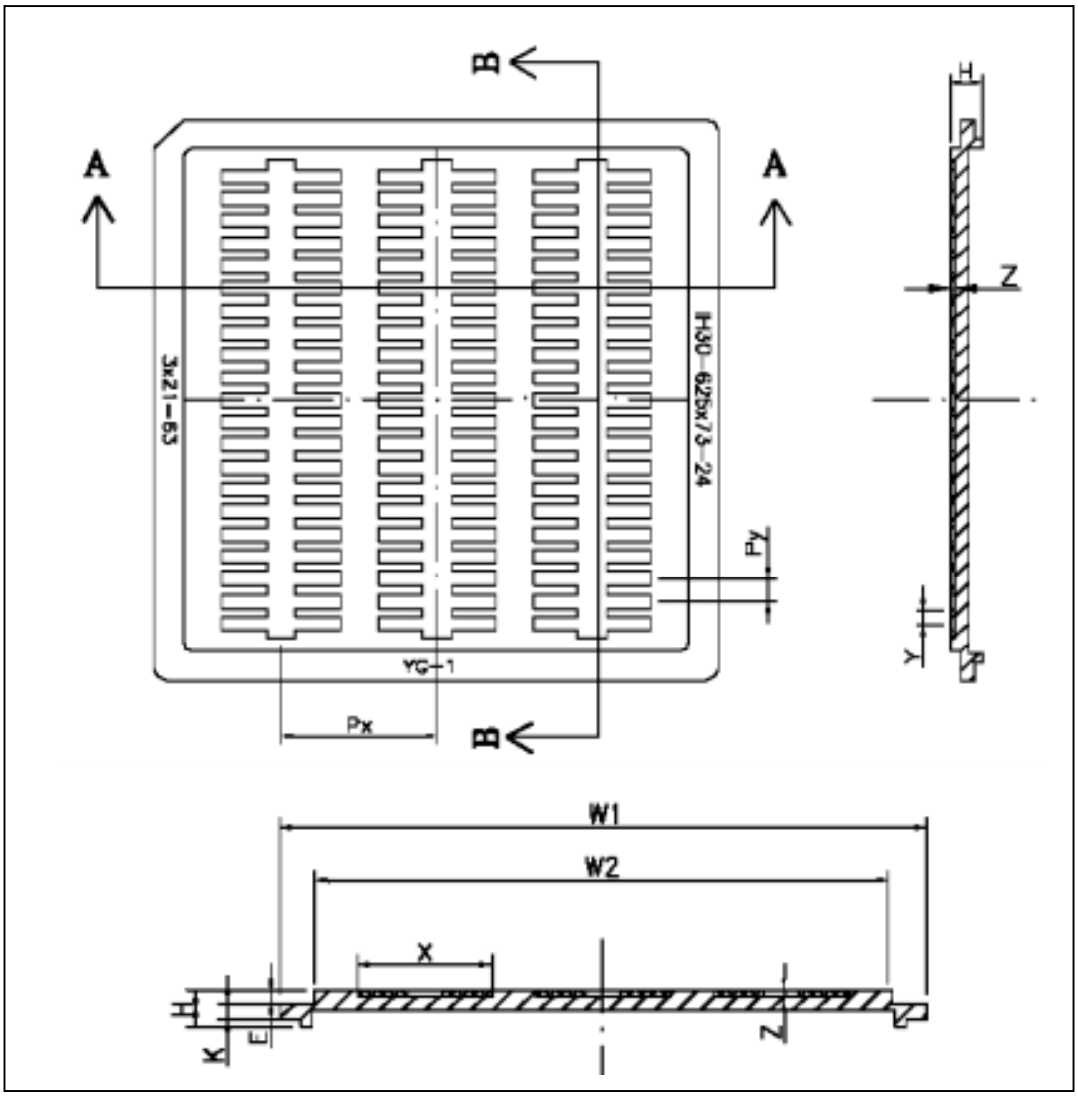


Figure 32 – Applications notes for V_{DD}/V_{DDIO} connection

14 PACKAGE INFORMATION

14.1 DIE TRAY DIMENSIONS



Spec	mm	(mil)
W1	$76.0^{+0.2}_{-0.1}$	(2992)
W2	$68.0^{+0.2}_{-0.1}$	(2677)
H	4.20 ± 0.1	(165)
E	1.60 ± 0.1	(63)
K	1.90 ± 0.1	(75)
Px	20.79 ± 0.1	(826)
Py	3.03 ± 0.1	(119)
X	$15.88^{+0.1}_{-0}$	(625)
Y	$1.85^{+0.1}_{-0}$	(73)
Z	0.62 ± 0.05	(24)
N	63	

http://www.solomon-systech.com