

Micro-Power Inverting DC/DC Controller

FEATURES

- 2.4V to 7V input voltage operation.
- Adjustable output voltage up to -40V.
- Low quiescent current at 80 μ A.
- Pulse frequency modulation maintains high efficiency (87%).
- 70KHz to 160KHz switching frequency.
- Power-saving shutdown mode (0.7 μ A typical).
- High efficiency with low cost external P-channel MOSFET or PNP bipolar transistor.

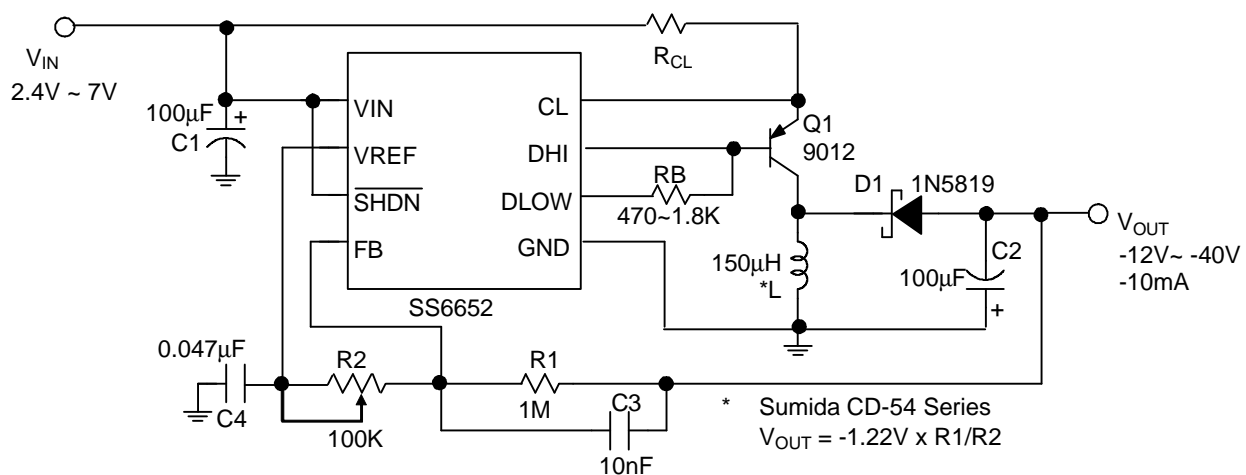
APPLICATIONS

- Negative LCD Contrast Bias for
 1. Notebook & Palmtop Computers.
 2. Pen-Based Data System.
 3. Portable Data Collection Terminals.
 4. Personal Digital Assistants.
- Negative Voltage Supply.

DESCRIPTION

The SS6652 is a high-performance inverting DC/DC controller, designed to drive an external power switch to generate programmable negative voltages, and is particularly suited to LCD bias contrast applications. Efficiency of 87% can be achieved with low cost PNP bipolar transistor drivers. Output voltage can be scaled to -40V or greater by two external resistors. A pulse frequency modulation scheme is employed to maintain high-efficiency conversion over a wide input voltage range. Quiescent current is about 80 μ A and can be reduced to 0.7 μ A in shutdown mode. With switching frequencies in the 70KHz to 160KHz range, the small size switching components are ideal for battery powered portable equipment, like notebook and palmtop computers.

TYPICAL APPLICATION CIRCUIT



Negative LCD Contrast Bias Power Supply

ORDERING INFORMATION

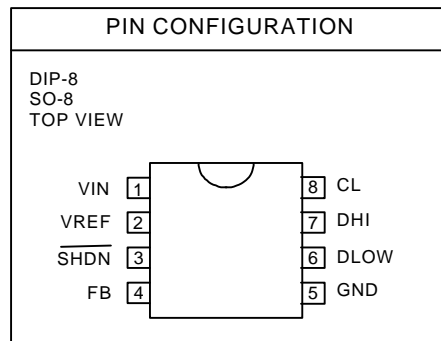
SS6652CXXX

PACKING TYPE
TR: TAPE & REEL
TB: TUBE

PACKAGE TYPE
N: PLASTIC DIP
S: SMALL OUTLINE

EX: SS6652CSTR

→ in SO-8 Package in Tape & Reel Packing
(CN is not available in TR packing type.)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7V
SHDN Voltage	7V
Operation Temperature Range	0°C~70°C
Storage Temperature Range	-65°C~ 150°C

TEST CIRCUIT

Refer to Typical Application Circuit.

ELECTRICAL CHARACTERISTICS (V_{IN}=5V, T_a=25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage		2.4		7	V
Switch Off Current	V _{FB} =-50mV		80	150	μA
V _{REF} Voltage	I _{SOURCE} = 250μA	1.16	1.22	1.28	V
V _{REF} Source Current		250			μA
DLOW "ON Resistance"			5		Ω
DHI "ON Resistance"			7		Ω
CL Threshold			70		mV
Shutdown Threshold		0.8	1.5	2.4	V
Shutdown Mode Current	V _{SHDN} = 0V		0.7	2	μA

■ TYPICAL PERFORMANCE CHARACTERISTICS

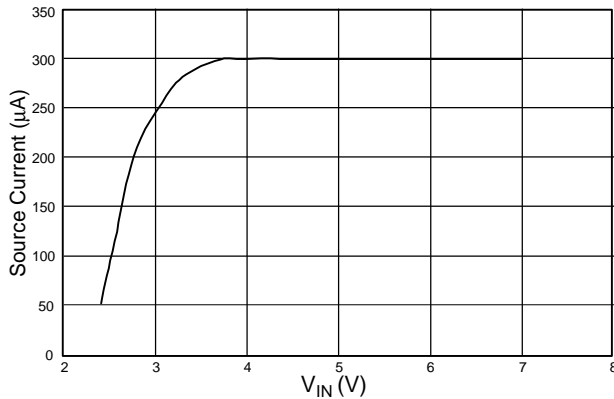


Fig. 1 V_{REF} Source Current vs. V_{IN}

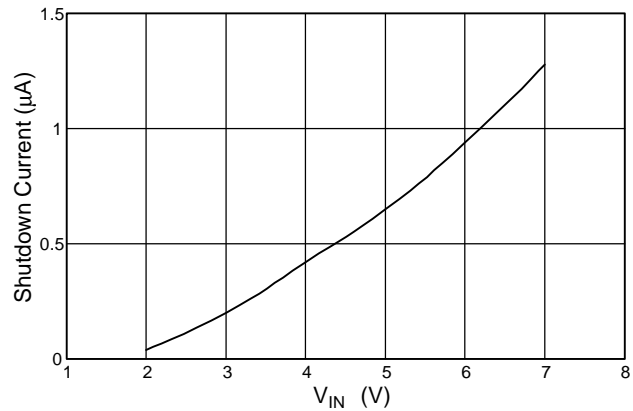


Fig. 2 Shutdown Current vs. V_{IN}

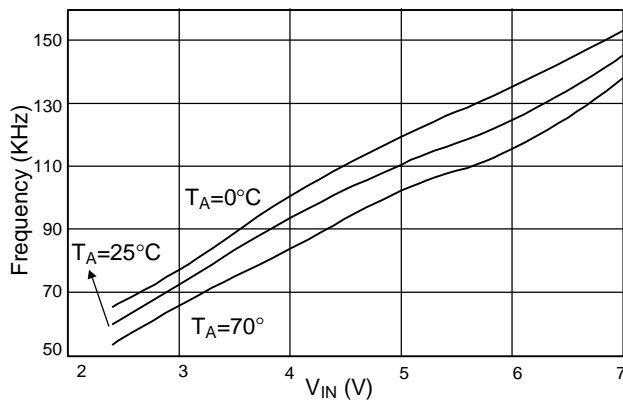


Fig. 3 Frequency vs. V_{IN} Voltage

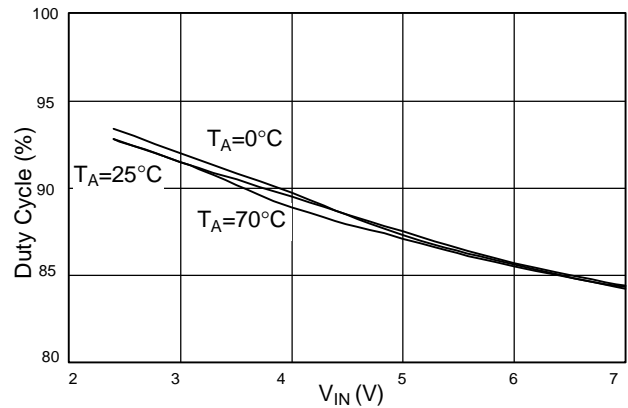
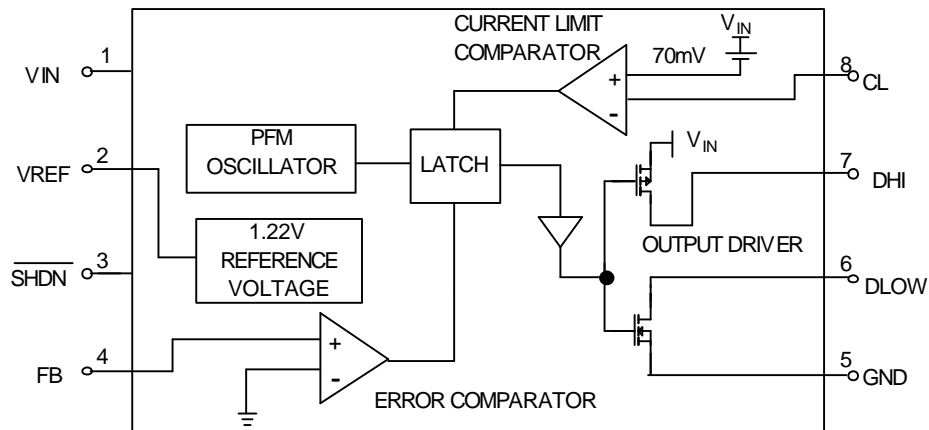


Fig. 4 Duty Cycle vs. V_{IN} Voltage

■ BLOCK DIAGRAM



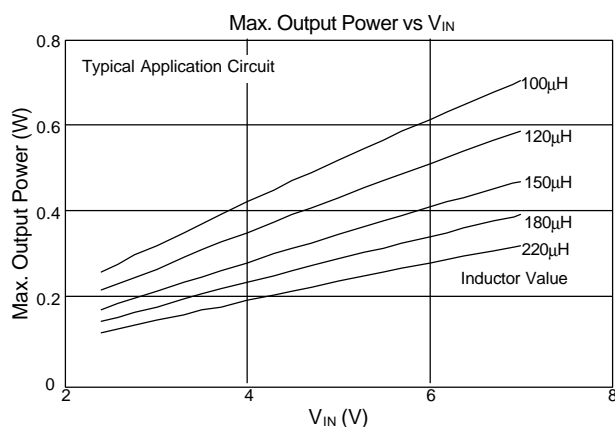
■ PIN DESCRIPTIONS

- PIN 1: VIN - Input supply voltage (2.4V~7V)
- PIN 2: VREF - Reference output (1.22V). Bypass with a 0.047μF capacitor to GND. Sourcing capability is guaranteed to be greater than 250μA.
- PIN 3: $\overline{\text{SHDN}}$ - Logic input to shutdown the chip.
 >1.5V = normal operation,
 GND = shutdown
 In shutdown mode DLOW and DHI pins are at high level.
- PIN 4: FB - Feedback signal input to sense ground. Connecting a resistor R1 to V_{OUT} and a resistor R2 to V_{REF} pin yields the output voltage:

$$V_{\text{OUT}} = - (R1/R2) \times V_{\text{REF}}$$
- PIN 5: GND - Power ground.

- PIN 6: DLOW - Driver sinking output. Connected to DHI when using an external P-channel MOSFET. When using an external PNP bipolar transistor, connect a resistor RB from this pin to DHI. RB value depends on V_{IN}, inductor and PNP bipolar transistor. By adjusting the RB value, efficiency can be optimized.
- PIN 7: DHI - Driver sourcing output. Connect to gate of the external P-channel MOSFET or base of the PNP bipolar transistor.
- PIN 8: CL - Current-limit input. This pin clamps the switch peak current to prevent over-current damage to the external switch.

■ APPLICATION INFORMATION



The typical application circuit generates an adjustable negative voltage for contrast bias of LCD displays. Efficiency and output power can be optimized by using appropriate inductor and switch. The following formulae provide a guideline for determining the optimal component values:

$$L = (11.1 - 0.15 \times V_{\text{IN}}) \times \frac{V_{\text{IN}}}{|I_{\text{OUT}}| \times |V_{\text{OUT}}|}$$

$$\text{PNP} : |V_{\text{CEO}}| > V_{\text{IN}} + |V_{\text{OUT}}|$$

$$|I_{\text{C,MAX}}| \geq 200 \times \frac{|I_{\text{OUT}}|}{V_{\text{IN}}}$$

$$|V_{\text{CE}}| < 0.4\text{V at } I_{\text{C}} = 200 \times \frac{I_{\text{OUT}}}{V_{\text{IN}}}$$

$$\text{and } b = 10$$

$$R_{\text{B}} \cong 3 \times L \times (V_{\text{IN}} - 0.8)$$

where, V_{IN}(V), V_{OUT}(V), I_{OUT}(A), L(μH), R_B(Ω)

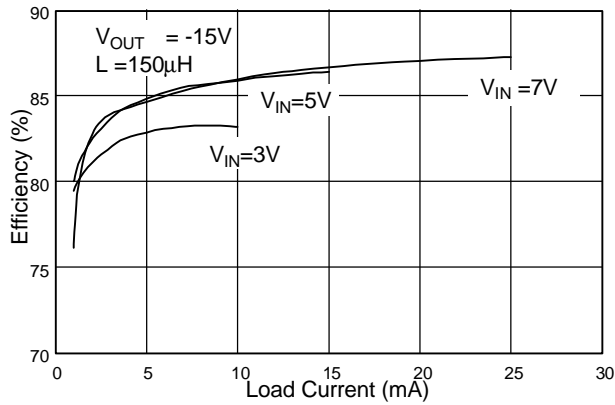
APPLICATION CIRCUIT (Refer to TYPICAL APPLICATION CIRCUIT)


Fig. 5 Efficiency vs. Load Current

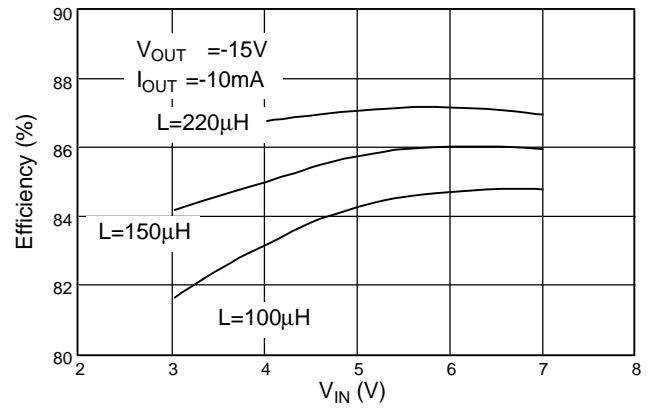
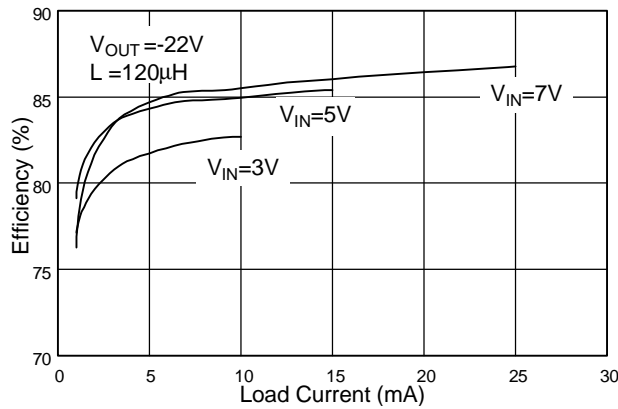

 Fig. 6 Efficiency vs. V_{IN}


Fig. 7 Efficiency vs. Load Current

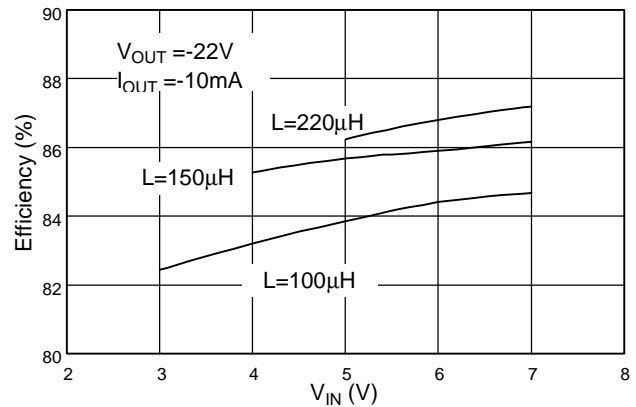
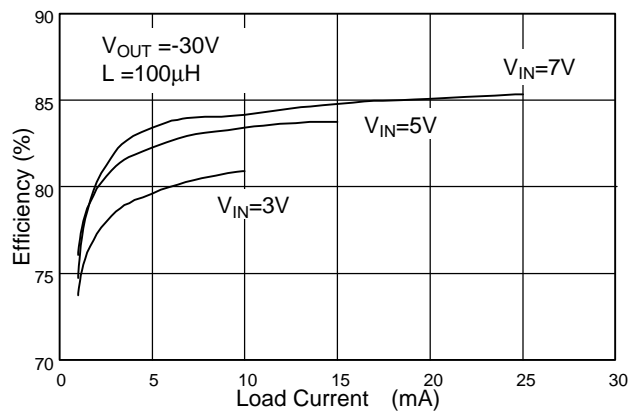
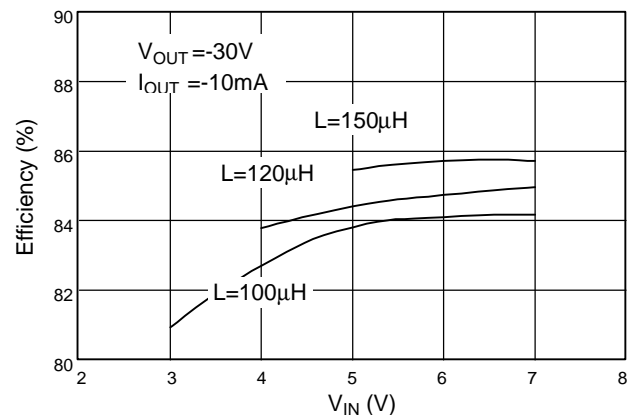
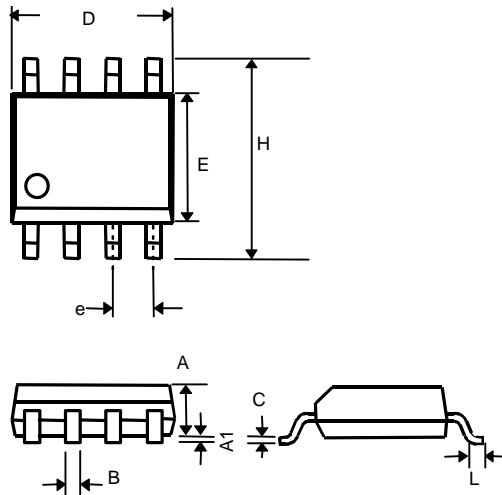

 Fig. 8 Efficiency vs. V_{IN}


Fig. 9 Efficiency vs. Load Current


 Fig. 10 Efficiency vs. V_{IN}

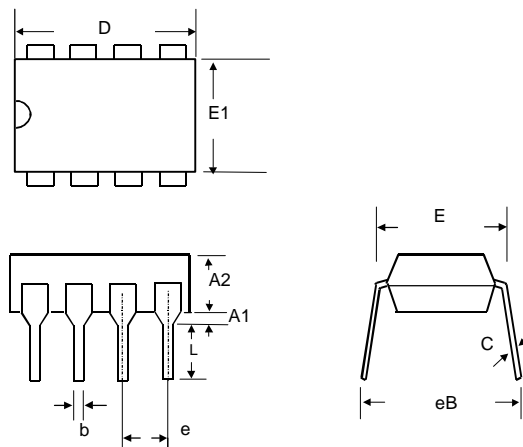
PHYSICAL DIMENSIONS

● 8 LEAD PLASTIC SO (unit: mm)



SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27(TYP)	
H	5.80	6.20
L	0.40	1.27

● 8 LEAD PLASTIC DIP (unit: mm)



SYMBOL	MIN	MAX
A1	0.381	—
A2	2.92	4.96
b	0.35	0.56
C	0.20	0.36
D	9.01	10.16
E	7.62	8.26
E1	6.09	7.12
e	2.54 (TYP)	
eB	—	10.92
L	2.92	3.81

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