

# High-Efficiency, Inverting DC/DC Controller

## FEATURES

- 4V to 20V Input Voltage Operation.
- Adjustable Output Voltage up to -40V.
- Low Quiescent Current at 100µA.
- Pulse Frequency Modulation Maintains High Efficiency (max. 90%).
- 100KHz to 320KHz Switching Frequency.
- Power-Saving Shutdown Mode (8µA Typical).
- High Efficiency with Low Cost External PNP Bipolar Transistor.

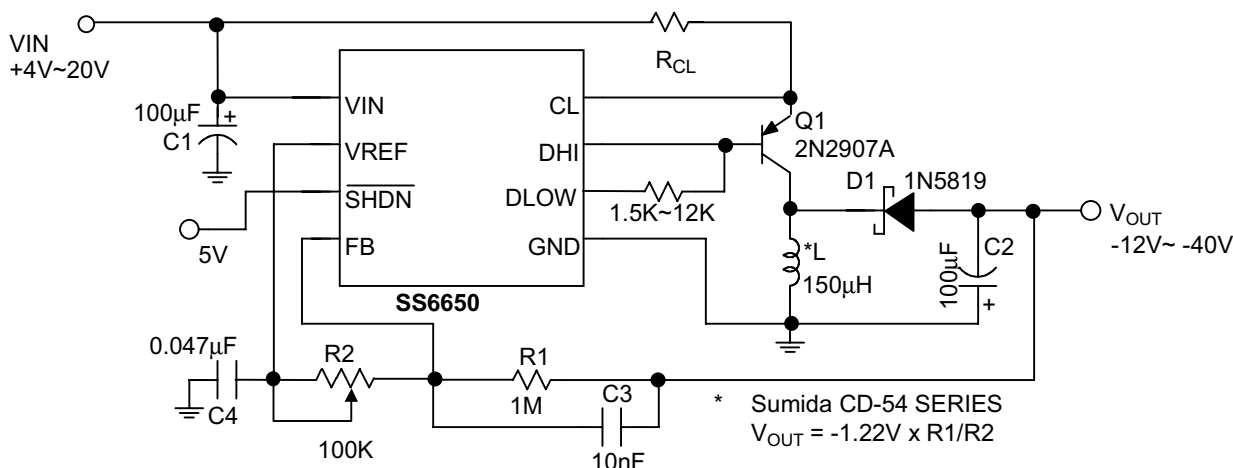
## APPLICATIONS

- Negative LCD Contrast Bias for
  1. Notebook & Palmtop Computers.
  2. Pen-Based Data System.
  3. Portable Data Collection Terminals.
  4. Personal Digital Assistants.
- Negative Voltage Supply.

## DESCRIPTION

The SS6650 is a high performance inverting DC/DC controller, designed to drive an external power switch to generate programmable negative voltages. In the particularly suitable LCD bias contrast application, maximum efficiency of 90% can be achieved with low cost PNP bipolar transistor drivers. 4V to 20V input operation range allows the SS6650 to be powered directly by the battery pack in most battery-operated applications for greater efficiency. Output voltage can be scaled to -40V or greater by two external resistors. A pulse frequency modulation scheme is employed to maintain high efficiency conversion under wide input voltage range. Quiescent current is about 100µA and can be reduced to 8µA in shutdown mode. Switching frequency being around 100KHz to 320KHz range, small size switching components are ideal for battery powered portable equipments, like notebook and palmtop computers.

## TYPICAL APPLICATION CIRCUIT



Negative LCD Contrast Bias Power Supply

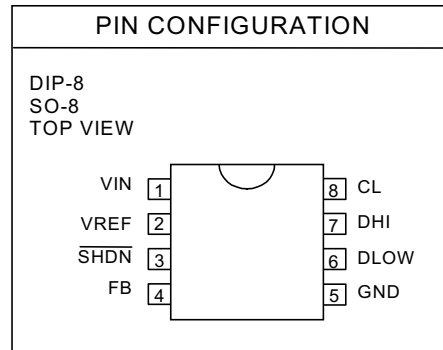
## ORDERING INFORMATION

SS6650CXXX

PACKING TYPE  
 TR: TAPE & REEL  
 TB: TUBE

PACKAGE TYPE  
 N: PLASTIC DIP  
 S: SMALL OUTLINE

Example: SS6650CSTR  
 → in SO-8 Package & Tape & Reel Packing Type  
 (CN is not available in TR packing type.)



## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 20V

$\overline{\text{SHDN}}$  Voltage ..... 15V

Operating Temperature Range ..... 0°C~ 70°C

Storage Temperature Range ..... -65°C~ 150°C

## TEST CIRCUIT

Refer to Typical Application Circuit.

## ELECTRICAL CHARACTERISTICS ( $V_{\text{IN}}=13\text{V}$ , $T_{\text{A}}=25^{\circ}\text{C}$ , unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage		4		20	V
Switch Off Current	$V_{\text{FB}} = -50\text{mV}$		100	200	$\mu\text{A}$
$V_{\text{REF}}$ Voltage	$I_{\text{SOURCE}} = 250\mu\text{A}$	1.16	1.22	1.28	V
$V_{\text{REF}}$ Source Current		250			$\mu\text{A}$
DLOW "ON Resistance"			15		$\Omega$
DHI "ON Resistance"			10		$\Omega$
CL Threshold		50	70	90	mV
Shutdown Threshold		0.8	1.5	2.4	V
Shutdown Mode Current	$V_{\overline{\text{SHDN}}}=0\text{V}$		8	20	$\mu\text{A}$

## ■ TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A=25^\circ\text{C}$ )

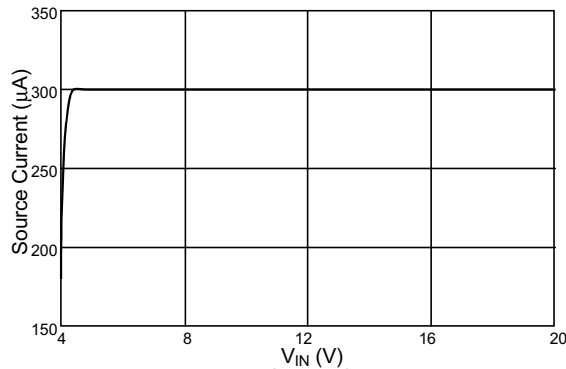


Fig. 1  $V_{REF}$  Source Current vs.  $V_{IN}$

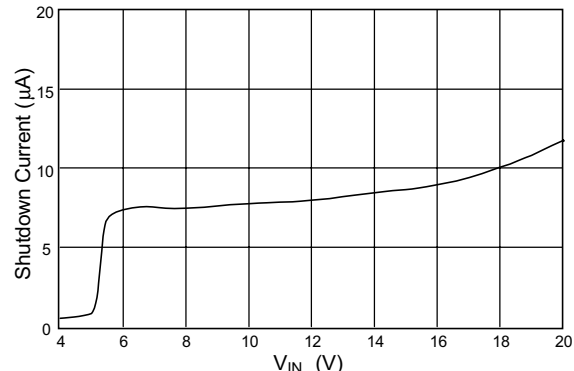


Fig. 2 Shutdown Current vs.  $V_{IN}$

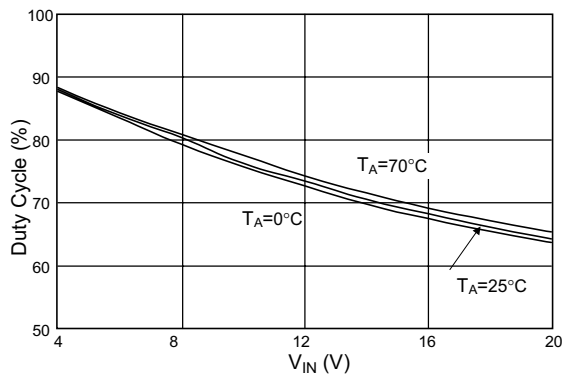


Fig. 3 Duty Cycle vs.  $V_{IN}$  Voltage

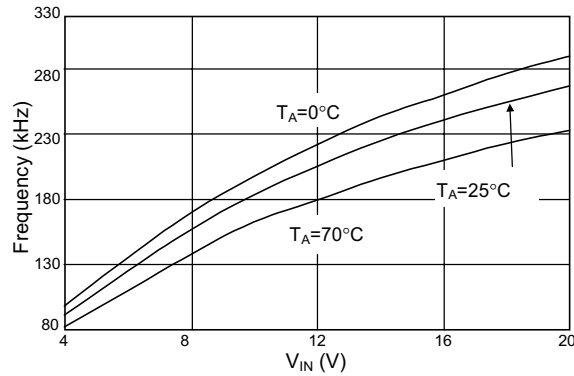
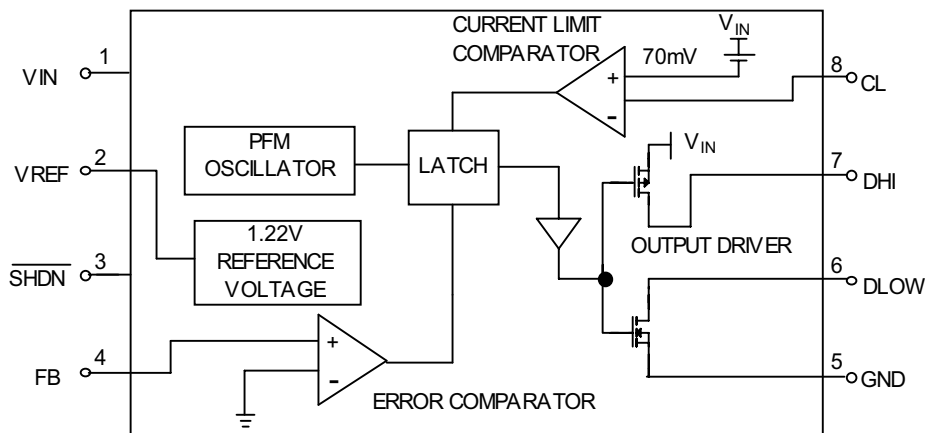


Fig. 4 Frequency vs.  $V_{IN}$  Voltage

## ■ BLOCK DIAGRAM



## PIN DESCRIPTIONS

PIN 1: VIN - Input Supply Voltage (4V~20V)

PIN 2: VREF - Reference Output (1.22V) Bypass with a 0.047μF capacitor to GND. Sourcing capability is guaranteed to be greater than 250μA.

PIN 3:  $\overline{\text{SHDN}}$  - Logic input to shutdown the chip. >1.5V (normal operation), GND (shutdown mode) In shutdown mode DLOW and DHI pins are at high level.

PIN 4: FB - Feedback signal input to sense ground. Connecting a resistor R1 to V<sub>OUT</sub> and a resistor R2 to V<sub>REF</sub> pin yields the output voltage:

$$V_{\text{OUT}} = -(R1/R2) \times V_{\text{REF}}$$

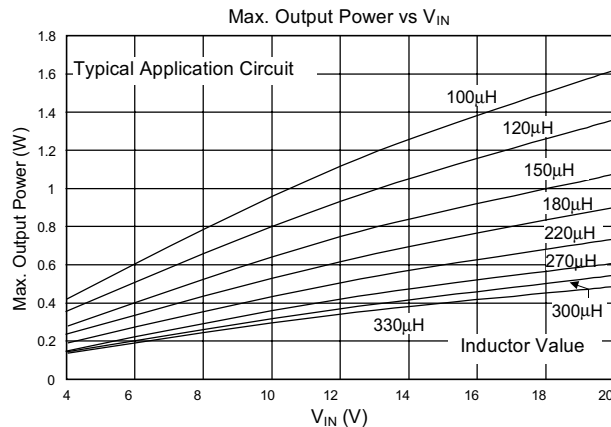
PIN 5: GND - Power ground.

PIN 6: DLOW - Driver sinking output. Connected to DHI when using an external P-channel MOSFET. When using an external PNP bipolar transistor, connect a resistor RB from this pin to DHI. RB value depends on V<sub>IN</sub>, inductor and PNP bipolar transistor. By adjusting the RB value, efficiency can be optimized.

PIN 7: DHI - Driver sourcing output. Connect to gate of the external P-channel MOSFET or base of the PNP bipolar transistor.

PIN 8: CL - Current-limit input. This pin clamps the switch peak current to prevent over-current damage to the external switch.

## APPLICATION INFORMATIONS



The typical application circuit generates an adjustable negative voltage for contrast bias of LCD displays. Efficiency and output power can be optimized by using appropriate inductor and switch. The following formulas provide a guideline for determining the optimal component values:

$$L = (111 - 0.15 \times V_{\text{IN}}) \times \frac{V_{\text{IN}}}{|I_{\text{OUT}}| \times |V_{\text{OUT}}|}$$

$$\text{PNP} : |V_{\text{CE0}}| > V_{\text{IN}} + |V_{\text{OUT}}|$$

$$|I_{\text{C,MAX}}| \geq 200 \times \frac{|I_{\text{OUT}}|}{V_{\text{IN}}}$$

$$|V_{\text{CE}}| < 0.4\text{V} \text{ at } I_{\text{c}} = 200 \times \frac{I_{\text{OUT}}}{V_{\text{IN}}}$$

$$\text{and } \beta = 10$$

$$R_{\text{B}} \cong 3 \times L \times (V_{\text{IN}} - 0.8)$$

where, V<sub>IN</sub>(V), V<sub>OUT</sub>(V), I<sub>OUT</sub>(A), L(μH), R<sub>B</sub>(Ω)

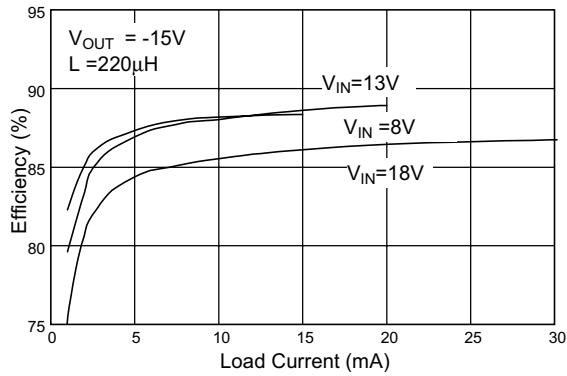
**APPLICATION CIRCUIT (Refer to TYPICAL APPLICATION CIRCUIT)**


Fig. 5 Efficiency vs. Load Current

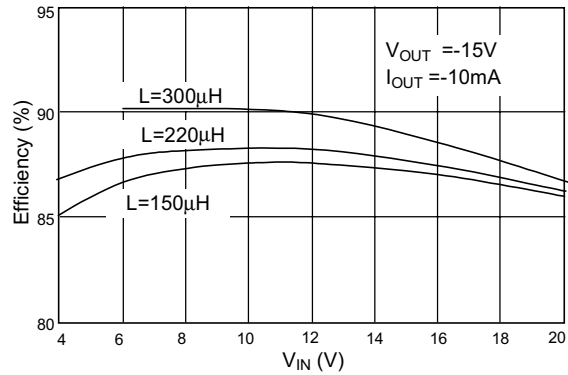
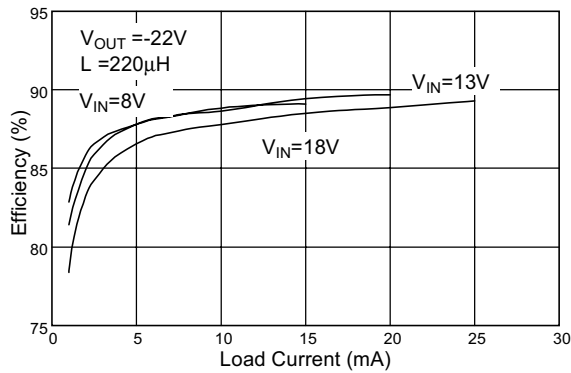

 Fig. 6 Efficiency vs.  $V_{IN}$ 


Fig. 7 Efficiency vs. Load Current

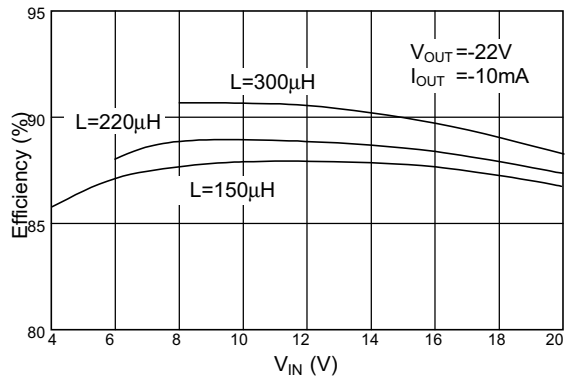
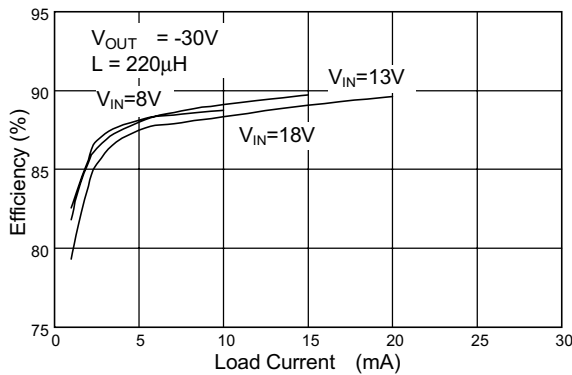
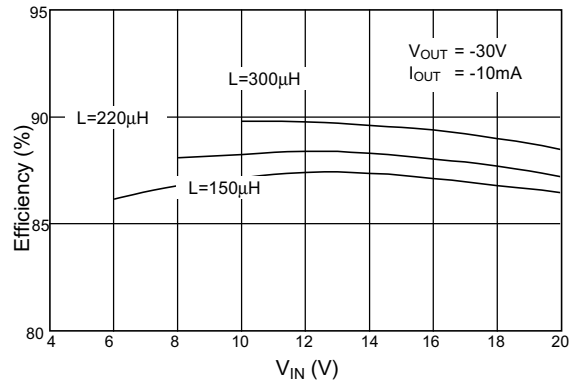
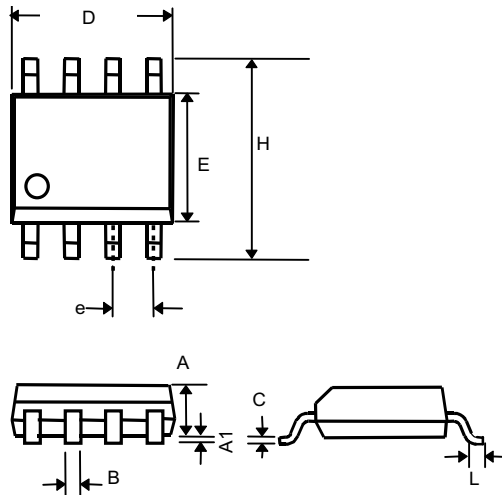

 Fig. 8 Efficiency vs.  $V_{IN}$ 


Fig. 9 Efficiency vs. Load Current


 Fig. 10 Efficiency vs.  $V_{IN}$

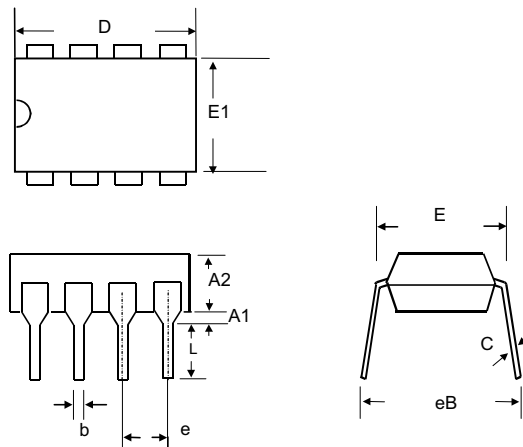
## ■ PHYSICAL DIMENSIONS

### ● 8 LEAD PLASTIC SO (unit: mm)



SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27(TYP)	
H	5.80	6.20
L	0.40	1.27

### ● 8 LEAD PLASTIC DIP (unit: mm)



SYMBOL	MIN	MAX
A1	0.381	—
A2	2.92	4.96
b	0.35	0.56
C	0.20	0.36
D	9.01	10.16
E	7.62	8.26
E1	6.09	7.12
e	2.54 (TYP)	
eB	—	10.92
L	2.92	3.81

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, express or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.