FAIRCHILD
SEMICONDUCTOR®

SPT7936

12-BIT, 28 MSPS SAMPLING A/D CONVERTER

FEATURES

- 3.0-3.6 V Power Supply
- Typical SINAD: 60 dB for (f_{IN} = 10 MHz)
- Low power: (260 mW @3.3 V)
- Sample Rate: 28 MSPS
- Internal Sample/Hold
- Differential Input
- Sleep Mode (Power Down)

APPLICATIONS

- Imaging
- Test Equipment
- Computer Scanners
- Communications
- Set-Top Boxes

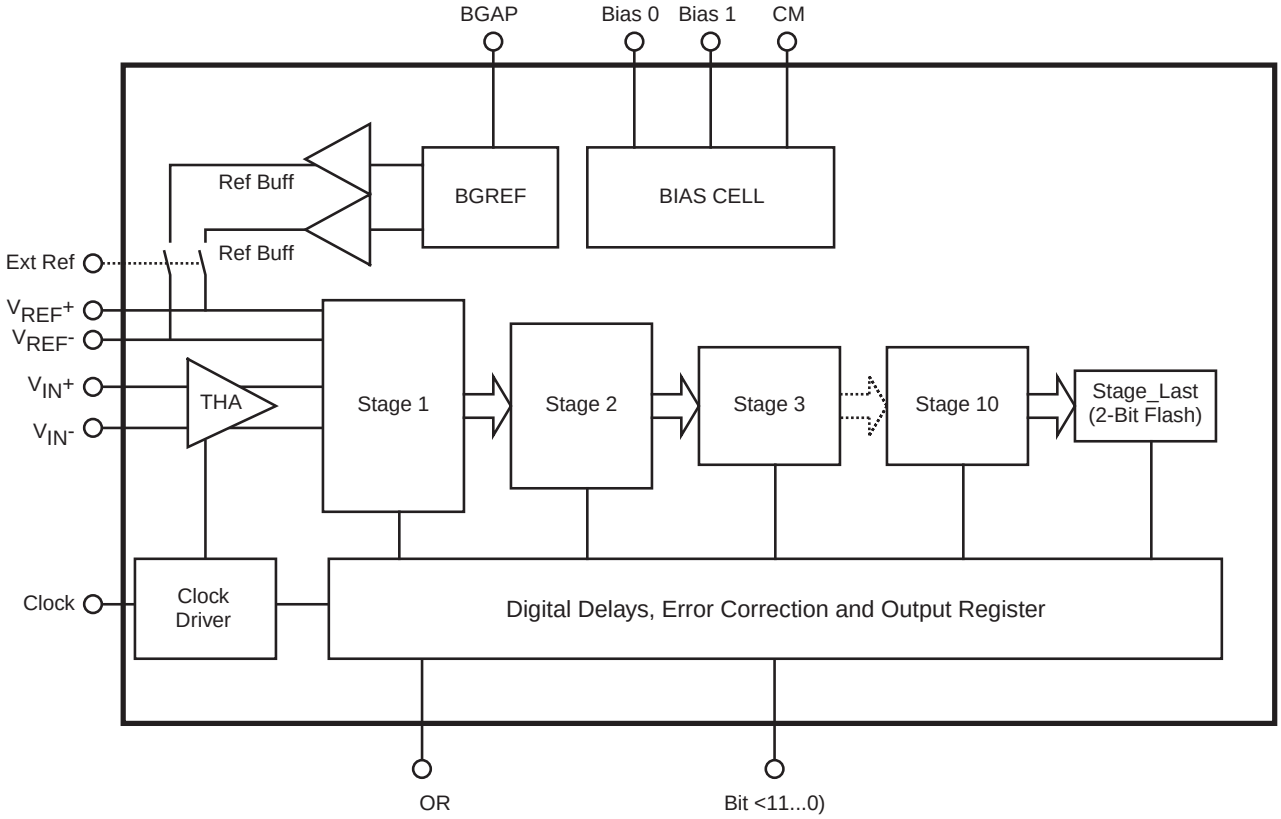
GENERAL DESCRIPTION

The SPT7936 is a compact, high-speed, low power 12-bit monolithic analog-to-digital converter, implemented in a 0.5 µm CMOS process. The converter includes sample and hold. The full scale range can be set between ±0.6 V and ±1.2 V using external references. It operates from a single 3.0-3.6 V supply-compatible with modern digital systems. Most converters in this performance range demand at least a +5 V supply. Its low distortion and high dynamic range offers the performance needed for demanding imaging, multimedia, telecommunications and instrumentation applications.

The SPT7936 has a pipelined architecture - resulting in low input capacitance. Digital error correction of the 11 most significant bits ensures good linearity for input frequencies approaching Nyquist.

The device is available in a 44L TQFP package over the commercial temperature range of 0 to +70 °C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{DD_1} ..... - 0.3 V to +6 V
V_{DD_2} ..... - 0.3 V to +6 V

Temperatures

Operating Temperature ..... 0 to +70 °C
Storage Temperature.. ..... - 65 to +125 °C

Input Voltages

Analog In ..... - 0.3 V to V_{DD} + 0.3 V
Digital In ..... - 0.3 V to V_{DD} + 0.3 V
REF_P ..... - 0.3 V to V_{DD} + 0.3 V
REF_N ..... - 0.3 V to V_{DD} + 0.3 V
CLOCK..... - 0.3 V to V_{DD} + 0.3 V

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$-T_{MAX}, $V_{DD_1} = V_{DD_2} = 3.3$ V, Sampling Rate = 28 MSPS, Differential input signal, 50% duty cycle clock with 2.5 ns rise and fall times, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7936 MIN	SPT7936 TYP	SPT7936 MAX	UNITS
DC Accuracy						
Differential Nonlinearity (DNL)		VI		±0.5	±1.0	LSB
Integral Nonlinearity		VI		±1.3	±3.0	LSB
Common Mode Rejection Ratio (CMRR)		V		54		dB
No Missing Codes				Guaranteed		
Analog Input						
Input Voltage Range (differential) VFSR		IV	0.6	±1	±1.2	V
Common Mode Input Voltage VCMI		IV	1.2	1.5	1.6	V
Input Capacitance C_{IN}		V		2		pF
(From Each Input to Ground)						
Midscale Offset V_{OS}	$V_{IN}+ = V_{IN}- = V_{CM}$	V		±2		%
Gain Error		V		-0.2		%
Input Bandwidth	Large Signal	V		150		MHz
Reference Voltages						
Internal Reference Voltage on Pin 10 (V_{REFNI})		VI	0.95	1.0	1.05	V
Internal Reference Voltage on Pin 11 (V_{REFPI})		VI	1.95	2.0	2.05	V
Internal Reference Voltage Drift		IV			100	ppm/°C
Negative Input Voltage (V_{REF}-)		VI	0.9	1.0	1.3	V
Positive Input Voltage (V_{REF}+)		VI	1.9	2.0	2.3	V
Reference Input Voltage Range (V_{REF}+ — V_{REF}-)		IV	0.6	1.0	1.2	V
Common Mode Output Voltage (V_{CM})		VI	1.45	1.50	1.55	V
Bandgap Output Voltage (V_{BGAP})		VI	2.365	2.415	2.465	V
Dynamic Performance						
Effective Number of Bits	f_{IN} = 5.0 MHz	V		10.0		Bits
	f_{IN} = 10.0 MHz	VI	9.2	9.7		Bits
Signal to Noise and Distortion Ratio (SINAD)	f_{IN} = 5.0 MHz	V		62		dB
	f_{IN} = 10.0 MHz	VI	57	60		dB
Signal to Noise Ratio (SNR)	f_{IN} = 5.0 MHz	V		64		dB
Without Harmonics	f_{IN} = 10.0 MHz	VI	59	63		dB
Total Harmonic Distortion (THD)	f_{IN} = 5.0 MHz	V		–66		dB
	f_{IN} = 10.0 MHz	VI		–64	–61	dB

ELECTRICAL SPECIFICATIONS

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PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7936 MIN	SPT7936 TYP	SPT7936 MAX	UNITS
Dynamic Performance						
Spurious Free Dynamic Range (SFDR)	f_{IN} = 5.0 MHz	V		67		dB
	f_{IN} = 10.0 MHz	VI	62	64		dB
Differential Phase (DP)		V		0.08		degrees
Differential Gain (DG)		V		0.27		%
Digital Inputs						
Logic 0 Voltage (V_{IL})		VI			20% V_{DD}	
Logic 1 Voltage (V_{IH})		VI	80% V_{DD}			
Logic 0 Current (IIL)	(V_I=V_{SS})	VI			±1	µA
Logic 1 Current (I_{IH})	(V_I=V_{DD})	VI			±1	µA
Input Capacitance (C_{IND})		V		1.8		pF
Digital Outputs						
Logic 0 Voltage (V_{OL})	(I = +2 mA)	VI		0.2	0.4	V
Logic 1 Voltage (V_{OH})	(I = -2 mA)	VI	85% V_{DD}	90% V_{DD}		V
Output Hold Time (t_H)		V		5		ns
Output Delay Time (t_D)		V		8		ns
Switching Performance						
Maximum Conversion Rate (f_S)		VI	28			MSPS
Minimum Conversion Rate		IV	1			MSPS
Pipeline Delay (See Timing Diagram)		IV		8.0		Clocks
Aperture Jitter σ_{AP}		V		10		ps
Aperture Delay t_{AP}		V		2		ns
Power Supply						
Supply Voltage V_{DD}		IV	3.0	3.3	3.6	V
Supply Current I_{DD}						
ext ref		VI		75	87	mA
int ref		VI		79	91	mA
Power Dissipation P_D						
ext ref		VI		248	288	mW
int ref		VI		260	300	mW
Sleep Mode Current						
ext ref		VI		8	9	mA
int ref		VI		11	12	mA
Sleep Mode Power Dissipation						
ext ref		VI		25	29	mW
int ref		VI		36	40	mW
Power Supply Rejection Ratio (PSRR)		V		52		dB

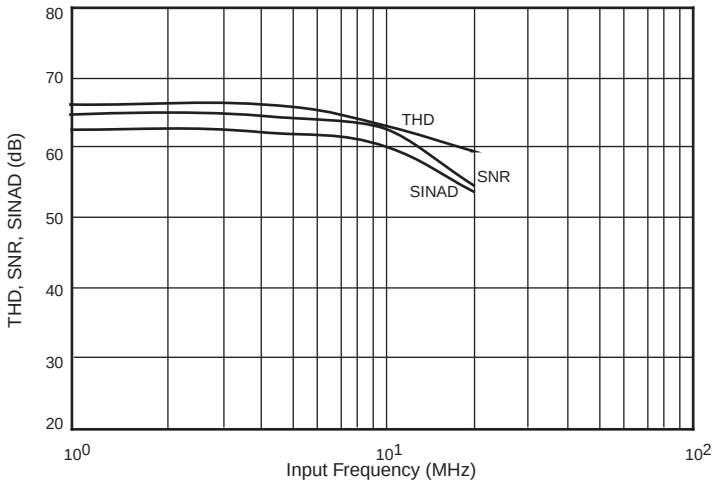
TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

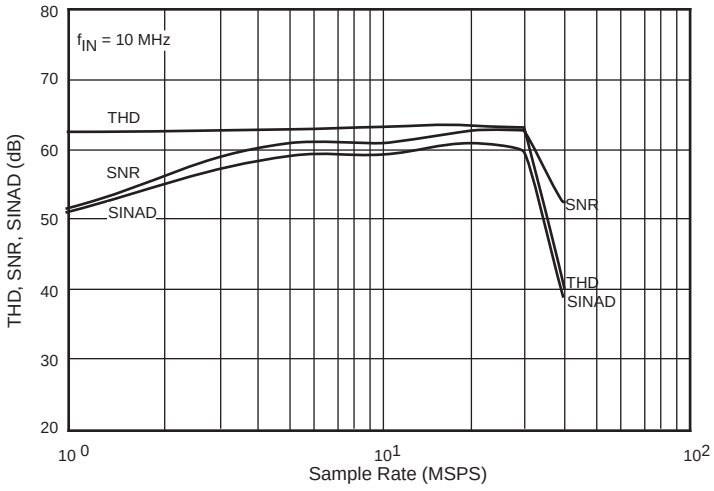
TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

THD, SNR, SINAD vs Input Frequency

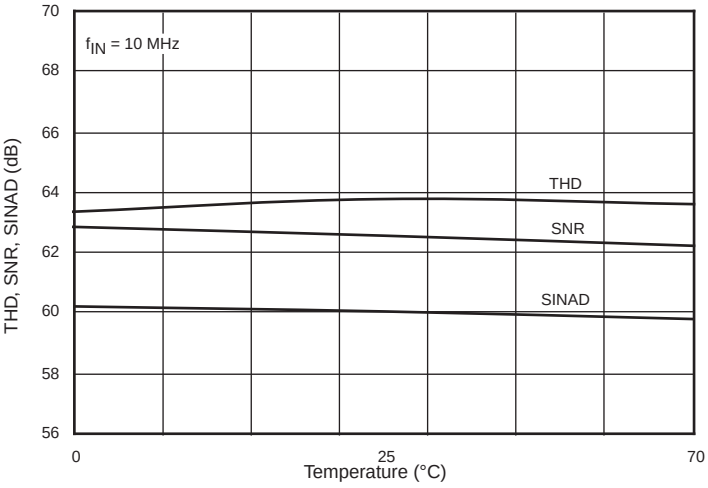


THD, SNR, SINAD vs Sample Rate

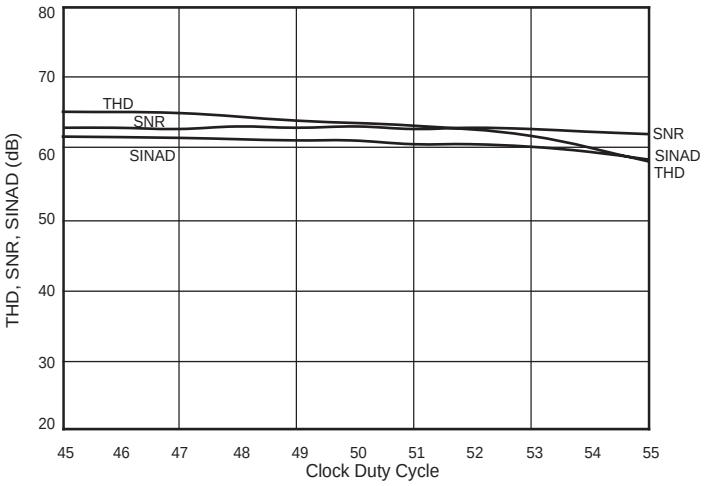


Note: Bias1 and Bias2 currents optimized for each sample rate.

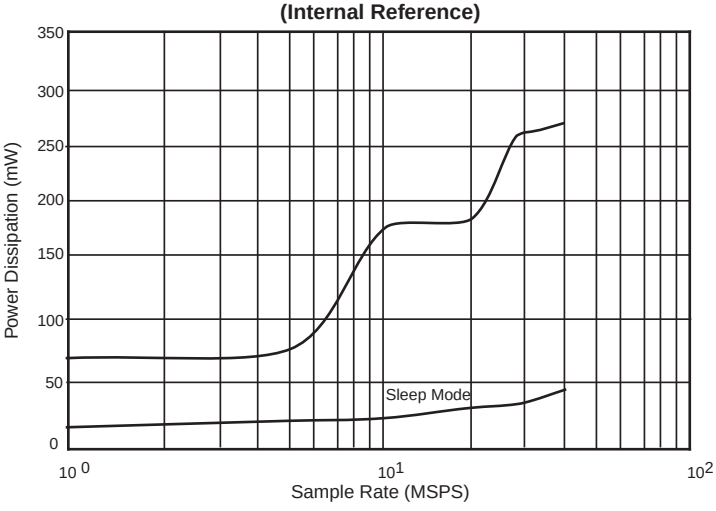
THD, SNR, SINAD vs Temperature



THD, SNR, SINAD vs Clock Duty Cycle

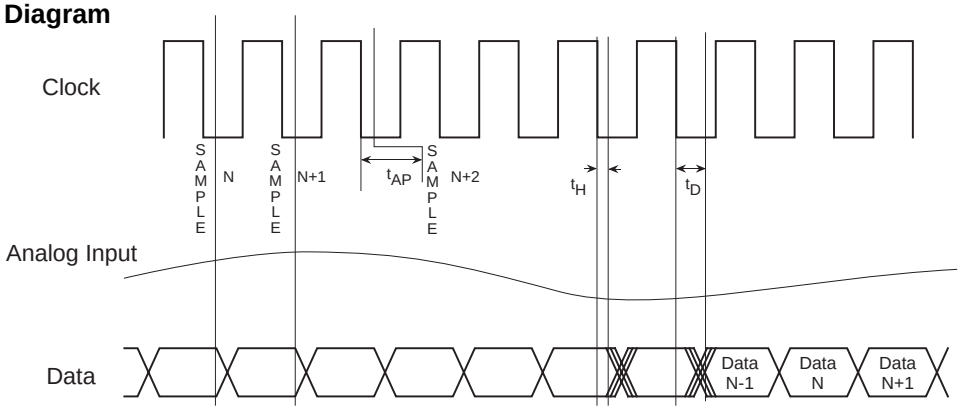


Power Dissipation vs Sample Rate (Internal Reference)



Note: Bias1 and Bias2 optimized for each sample rate.

Figure 1 - Timing Diagram



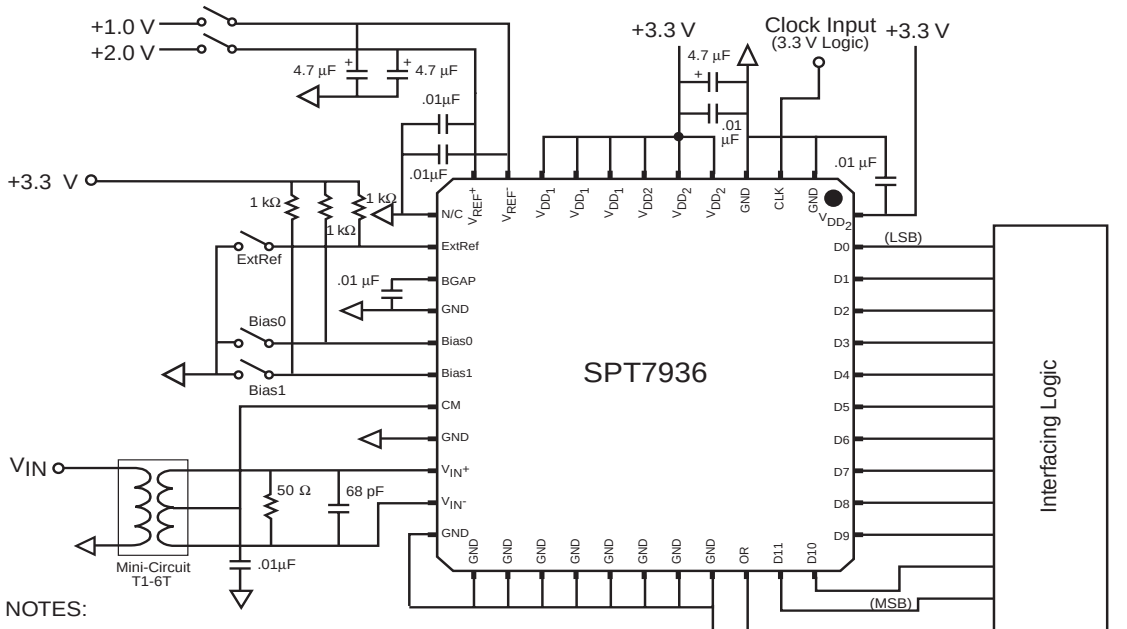
GENERAL DESCRIPTION

The SPT7936 is a low power, 12-bit, 28 MSPS ADC. It has a pipelined architecture and incorporates digital error correction of the 11 most significant bits. This error correction ensures good linearity performance for input frequencies up to Nyquist. The inputs are fully differential, making the device insensitive to system-level noise. This device can also be used in a single-ended mode. (See analog input section.) With the power dissipation roughly proportional to the sampling rate, this device is ideal for very low power applications in the range of 1 to 28 MSPS.

TYPICAL INTERFACE CIRCUIT

The SPT7936 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7936 in normal circuit operation. The following sections provide a description of the functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 2 - Typical Interface Circuit



NOTES:

1) Place the ferrite bead (*) as close to the device as possible.
2) Place 0.01 microfarad capacitors as close to the device as possible.
3) All capacitors are surface-mount unless otherwise specified.
4) All input pins (references, analog input, clock input) must be protected. (See absolute maximum rating.)
5) Set Bias1 and Bias0 for maximum sample rate.

Bias1	Bias0	
0	0	Sleep mode
0	1	Max. 5 MHz sampling
1	0	Max. 20 MHz sampling
1	1	Max. 28 MHz sampling

6) Use internal or external reference. Do not connect external voltage reference when using internal references.
7) All V_{DD_1} and V_{DD_2} must be connected together. Do not leave any pin unconnected.
8) All GND must be connected together. Do not leave any pin unconnected.

ANALOG INPUT

The SPT7936 has a differential input that should have a common mode voltage of +1.5 V. The input voltage range is determined by the reference voltages which may be generated internally or applied externally.

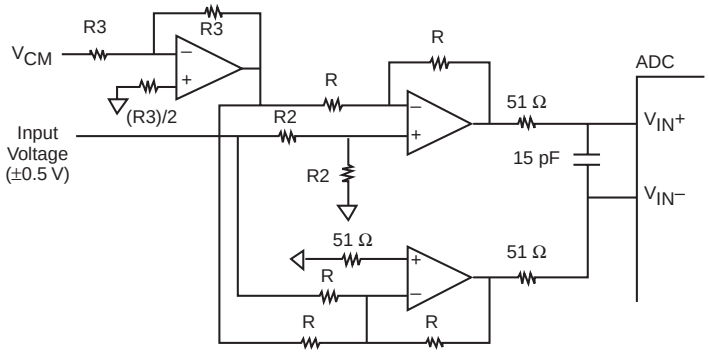
The input of the SPT7936 can be configured in various ways depending on if a single-ended or differential, AC- or DC-coupled input is desired.

The AC coupled input is most conveniently implemented using a transformer with a center tapped secondary winding. The center tap is connected to the V_{CM} pin as shown in figure 2. To obtain low distortion, it is important that the selected transformer does not exhibit core saturation at the full-scale voltage. Excellent results are obtained with the Mini Circuits T1-6T or T1-1T. Proper termination of the input is important for input signal purity. A small capacitor across the inputs attenuates kickback noise from the internal sample and hold.

Figure 3 illustrates a solution (based on operational amplifiers) that can be used if a a DC coupled single-ended input is desired. The selection criteria of the buffer op-amps is as follows:

- Open loop gain >75 dB
- Gain bandwidth product >50 MHz
- Total harmonic distortion ≤-75 dB
- Signal to Noise ratio >75 dB

Figure 3 - DC-Coupled Single-Ended-to-Differential Conversion (Power Supplies are Not Shown)



POWER SUPPLIES AND GROUNDING

The SPT7936 is operated from a single power supply in the range of 3.0 to 3.6 volts. Nominal operation is suggested to be 3.3 volts. All power supply pins should be bypassed as close to the package as possible. The analog and digital grounds should be connected together with a ferrite bead as shown in the typical interface circuit and as close to the ADC as possible.

REFERENCES

The SPT7936 can use either an internal or external voltage reference. When the digital input EXTREF is high, the external reference is used. When EXTREF is low, the internal reference is used.

INTERNAL REFERENCE

The internal references are set at +1.0 V and +2.0 V. When the internal reference is used, the full-scale range of the analog input is set at ±1.0 V differential. Do not connect external references when the internal reference is used.

EXTERNAL REFERENCE

When external references are used, the voltages applied to the $V_{REF}+$ and $V_{REF}-$ pins determine the input voltage range which is equal to $\pm(V_{REF}+ - V_{REF}-)$. Externally generated reference voltages must be connected to these pins and should be symmetric about the common mode voltage. (See figure 2, Typical Interface Circuit.)

COMMON MODE OUTPUT VOLTAGE REFERENCE CIRCUIT

The SPT7936 has an on-board common mode voltage reference circuit (V_{CM}). It is set at +1.5 V and can drive loads of up to 20 µA. This circuit is commonly used to drive the center tap of the RF transformer in fully differential applications. For single-ended applications, this output can be used to provide the level shifting required for the single-to-differential converter conversion circuit.

BIAS CIRCUITS

The best AC performance is achieved when the bias currents are optimized for the selected sample rate. Two digital input pins are provided to control the optimum internal bias currents. Table I shows the settings for Bias 0 and Bias 1 at selected frequencies.

Table I - Frequencies for Biases 0 and 1

			Typical Power Dissipation	
Bias 1	**Bias 0**	**Description**	**Ext. Ref.**	**Int. Ref.**
0	0	Sleep mode (power save)*	25 mW	36 mW
0	1	≤5 MHz sampling	61 mW	73 mW
1	0	≤20 MHz sampling	172 mW	184 mW
1	1	≤28 MHz sampling	248 mW	260 mW

*Clock = 28 MHz

CLOCK

The SPT7936 accepts a +3.3 V CMOS logic level at the CLK input. The duty cycle of the clock should be kept as close to 50% as possible. Because consecutive stages in the ADC are clocked in opposite phase to each other, a non-50% duty cycle reduces the settling time available for every other stage, *thus potentially causing a degradation of dynamic performance.*

For optimal performance at high input frequencies, the clock should have low jitter and fast edges. The rise/fall times should be kept shorter than 3 ns. Overshoot and undershoot should be avoided. Clock jitter causes the noise floor to rise proportional to the input frequency. Because jitter can be caused by crosstalk on the PC board, it is recommended that the clock trace be kept as short as possible and standard transmission line practices be followed.

DIGITAL OUTPUTS

The digital output data appears in an offset binary code at 3.3 V CMOS logic levels. A negative full scale input results in an all zeros output code (000…0). A positive full scale input results in an all 1's code (111…1). The output data is available 8 clock cycles after the data is sampled. The input signal is sampled on the high to low transition of the input clock. Output data should be latched on the low to high clock transition as shown in figure 1, the Timing Diagram. The output data is invalid for the first 20 clock cycles after the device is powered up.

OUT OF RANGE OUTPUT (OR)

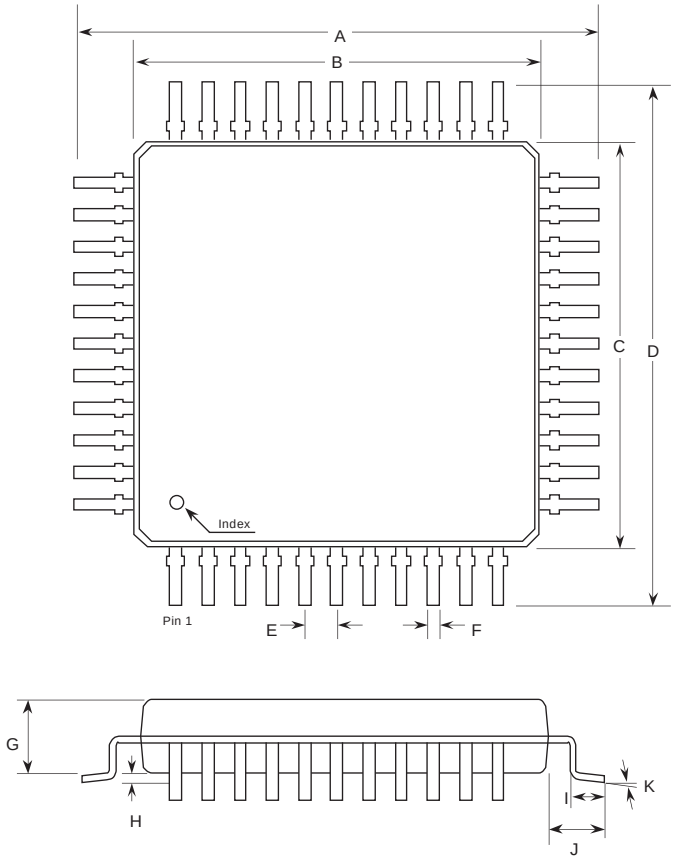
The digital output OR goes to a logic high to indicate that the analog input is out of range.

EVALUATION BOARD

The EB7936 Evaluation Board is available to aid designers in demonstrating the full performance capability of the SPT7936. The board includes an on-board clock driver, adjustable voltage references, adjustable bias current circuits, single-to-differential input buffers with adjustable levels, a single-to-differential transformer (1:1), digital output buffers and 3.3/5 V adjustable logic outputs. An application note (AN7936) is also available which describes the operation of the evaluation board and provides an example of the recommended power and ground layout and signal routing. Contact the factory for price and availability.

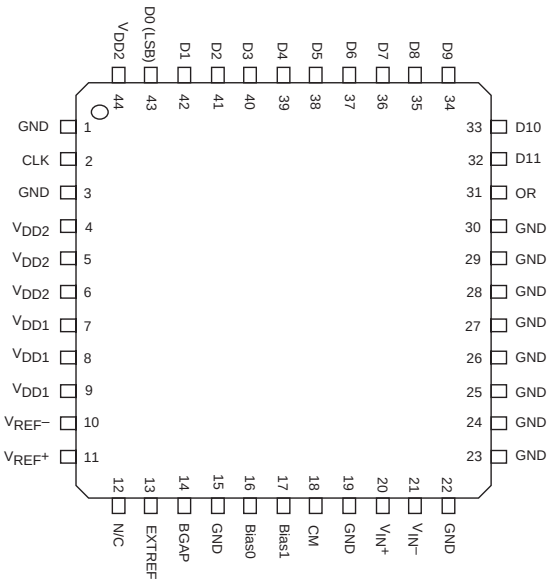
PACKAGE OUTLINE

44L TQFP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.472 Typ		12.00 Typ	
B	0.394 Typ		10.00 Typ	
C	0.394 Typ		10.00 Typ	
D	0.472 Typ		12.00 Typ	
E	0.031 Typ		0.80 Typ	
F	0.012	0.018	0.300	0.45
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.018	0.030	0.450	0.750
J	0.039 Typ		1.00 Typ	
K	0-7°		0-7°	

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
V_{IN}+, V_{IN}-	Differential input signal pins.
V_{REF}+, V_{REF}-	Reference input pins. Bypass with 100 nF capacitors close to the pins. See Application Information.
EXTREF	Digital input: Reference select. EXTREF=1: Use external reference. Internal reference powered down. EXTREF=0: Internal reference is used.
BIAS0, BIAS1 BIAS1=0, BIAS0=0: BIAS1=0, BIAS0=1: BIAS1=1, BIAS0=0: BIAS1=1, BIAS0=1:	Digital inputs for maximum sampling rate programming. Sleep mode (power save) Max. 5 MHz sampling Max. 20 MHz sampling (Default by internal pull up/pull down) Max. 28 MHz sampling
CLOCK	Clock input
CM	Common mode voltage output. (1.5 V typ)
D11-DØ	Digital outputs (MSB to LSB)
OR	Out-of-Range digital output. OR=1 indicates input out of range
V_{DD1} V_{DD2}	Analog power supply Digital power supply
GND	Analog Ground
N/C	No Connect Pins. Recommended to connect to analog ground.
BGAP	Internal Bandgap Reference Output: Bypass to ground for normal operation.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7936SCT	0 to +70 °C	44L TQFP

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.