SP8400

Very Low Phase Noise Synthesiser Divider

September 2005

The SP8400 is a very low phase noise programmable divider which is based on a divide by 8/9 dual modulus prescaler and a 12 stage control counter. This gives a minimum division ratio of 56 (64 for fractional - N synthesis applications), and a maximum division ratio of 4103. Special circuit techniques have been used to reduce the phase noise considerably below that produced by standard dividers.The data inputs are CMOS or TTL compatible.

The SP8400 is packaged in a 28 pin plastic SO package.

FEATURES

- Very low Phase Noise (Typically -156dBc/Hz at 1kHz offset)
- Supply Voltage 5V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.5V
Output Current	20mA
Storage Temperature Range	-55°C to +125°C
Maximum Clock Input Voltage	2.5V p-p

Ordering Information

SP8400/KG/MPES	28 Pin SOIC	Tubes
SP8400/KG/MPFP	28 Pin SOIC*	Tubes

*Pb Free Matte Tin

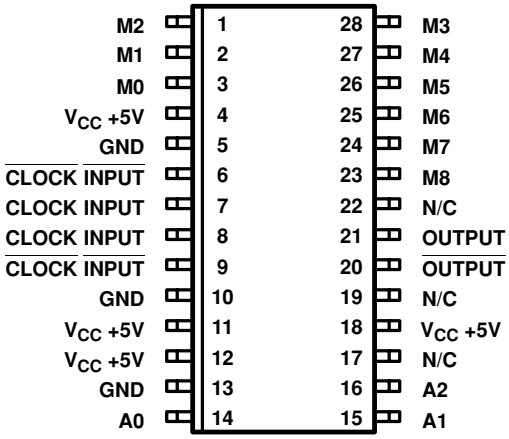

Fig.1 Pin connections - top view

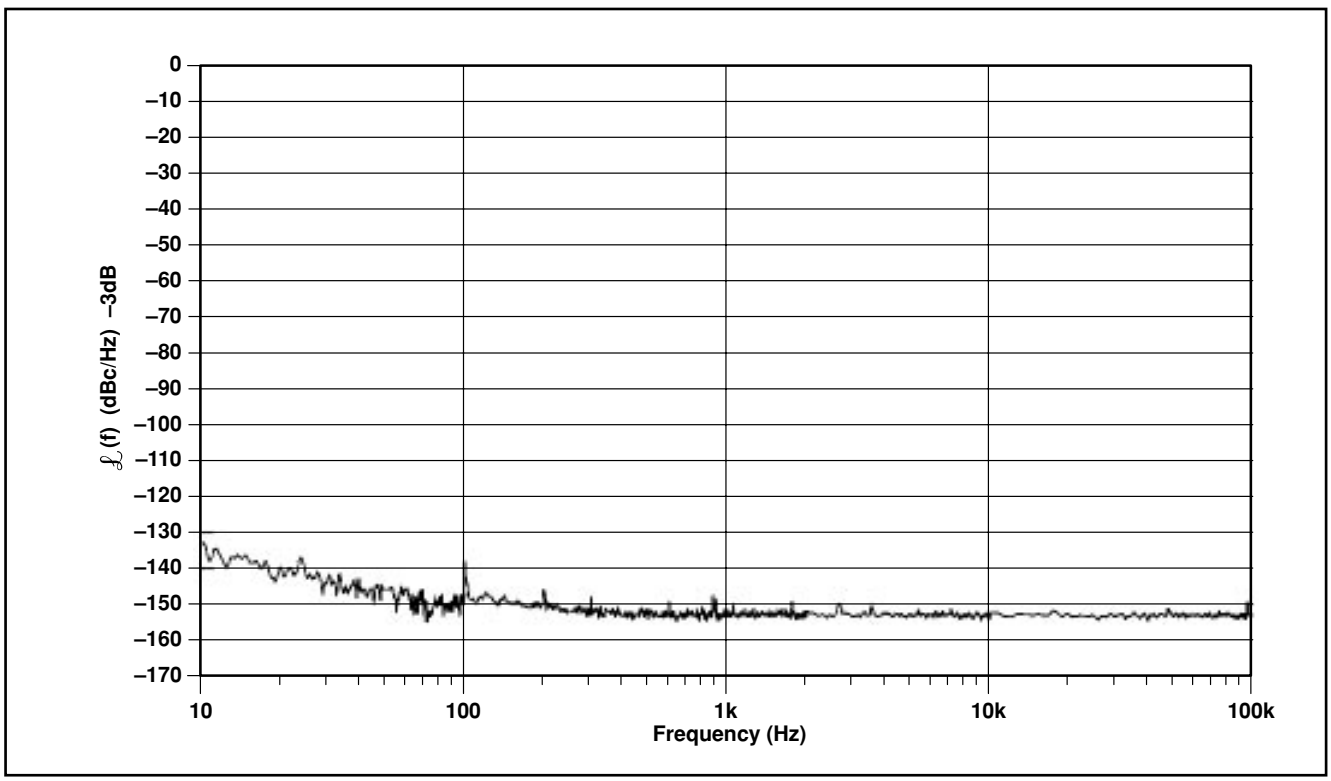

Fig.2 Typical single sideband phase noise measured at 300MHz

ELECTRICAL CHARACTERISTICS

Guaranteed over: Supply voltage V_{CC} = +4.75V to +5.25V Temperature T_{amb} = -10°C to +75°C
Tested at +4.75V and +5.25V at T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	4, 11, 12, 18	122	137	152	mA	Output loaded with 300R See Fig.4
Output voltage swing	20, 21	320	410		mV	p-p @ 1.5GHz input ÷ 71 mode See Fig.4
Input sensitivity 200MHz to 1.5GHz	7, 8			140	mV	RMS Sine wave into 50 Ohms
				(-4)	dBm	(dBm equivalent) See Fig.3
Data Inputs						
Logic high voltage		2.2			V	
Low low voltage				0.8	V	
Input current				180	µA	5V Data input voltage

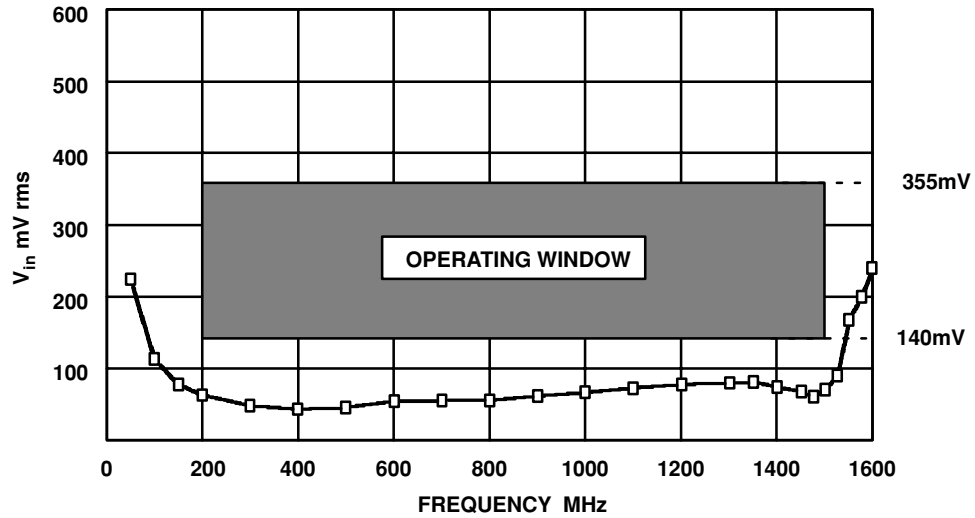

Fig.3 Typical input sensitivity

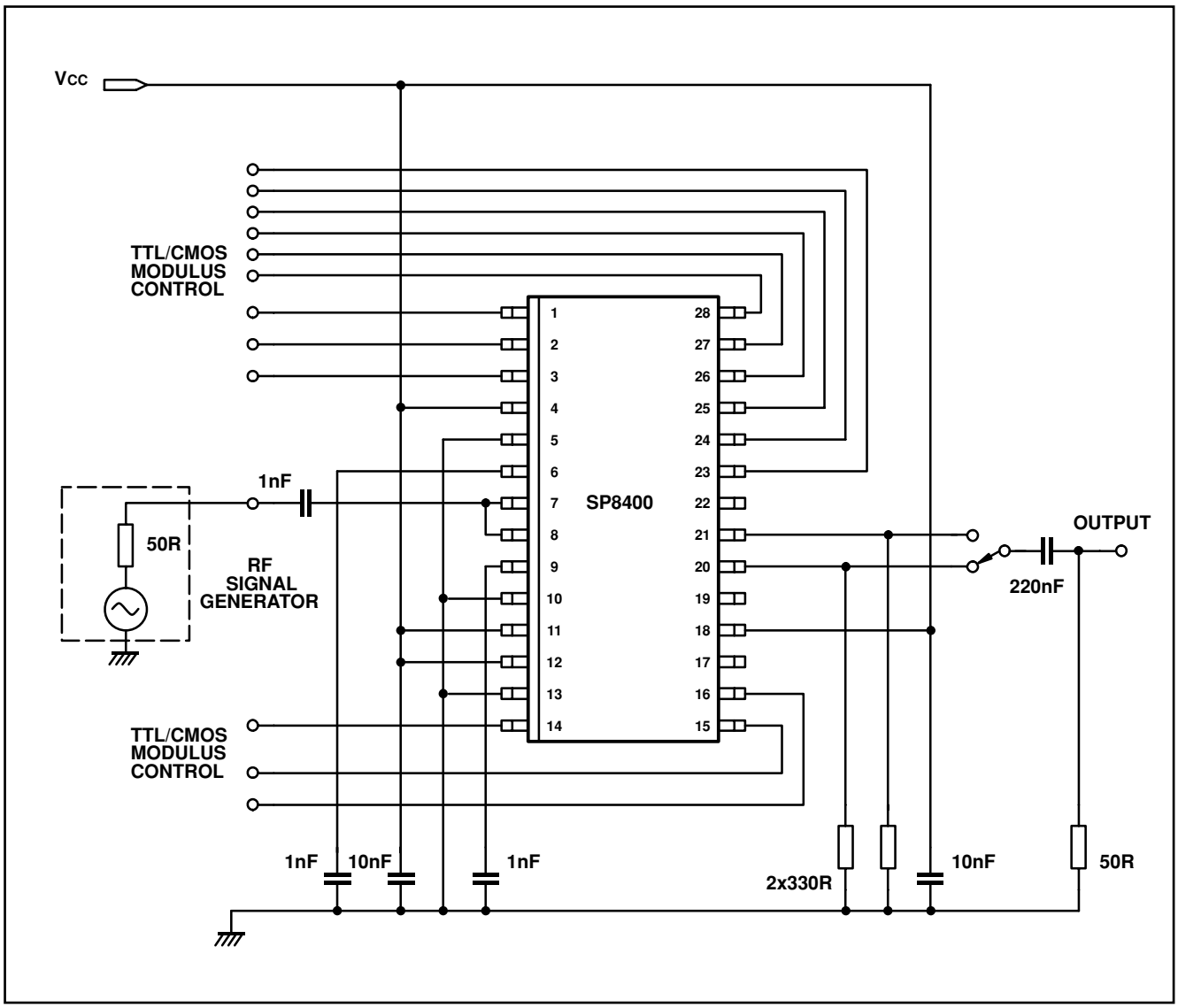

Fig.4 Test circuit

APPLICATIONS INFORMATION

Circuit description, synthesiser divider

The divider is based on a divide by 8/9 modulus prescaler, and a 12 stage control counter. This gives minimum fractional – N division ratio of 64 (56 for general division), and a maximum division ratio of 4103. The inputs to the control counter are TTL/CMOS compatible. There is a fixed offset of 8 between the number on the data lines and the actual division ratio.

The output is one transition only per divide cycle. This eliminates the problem of where to put the redundant edge when the divider is used in a fractional–N system, and also avoids the problem of how to define the output pulse width. This means that the overall division ratio conventionally defined in terms of the rate of edges of the same polarity is twice the selected division ratio.

Equations for division

The M and A data inputs form a 12 bit number with A0 being the least significant bit and M8 being the most significant bit.

Definition 1: Division ratio – (input frequency to out put edges, positive or negative).

= Number loaded + 8

Definition 2: Division ratio – (input frequency to out put frequency).

= (Number loaded + 8) x 2

Available division ratio

All division ratios of 64 to 4103 (Definition 1) will return the divider to the same internal state at the end of the count and hence these are the only divisional ratios to be used for fractional–N synthesiser application.
All division ratios of 56 to 4103 are available for general division purposes. Additional division ratios available for general division are:-

8,9
16, 17, 18
24, 25, 26, 27
32, 33, 34, 35, 36
40, 41, 42, 43, 44, 45
48, 49, 50, 51, 52, 53, 54

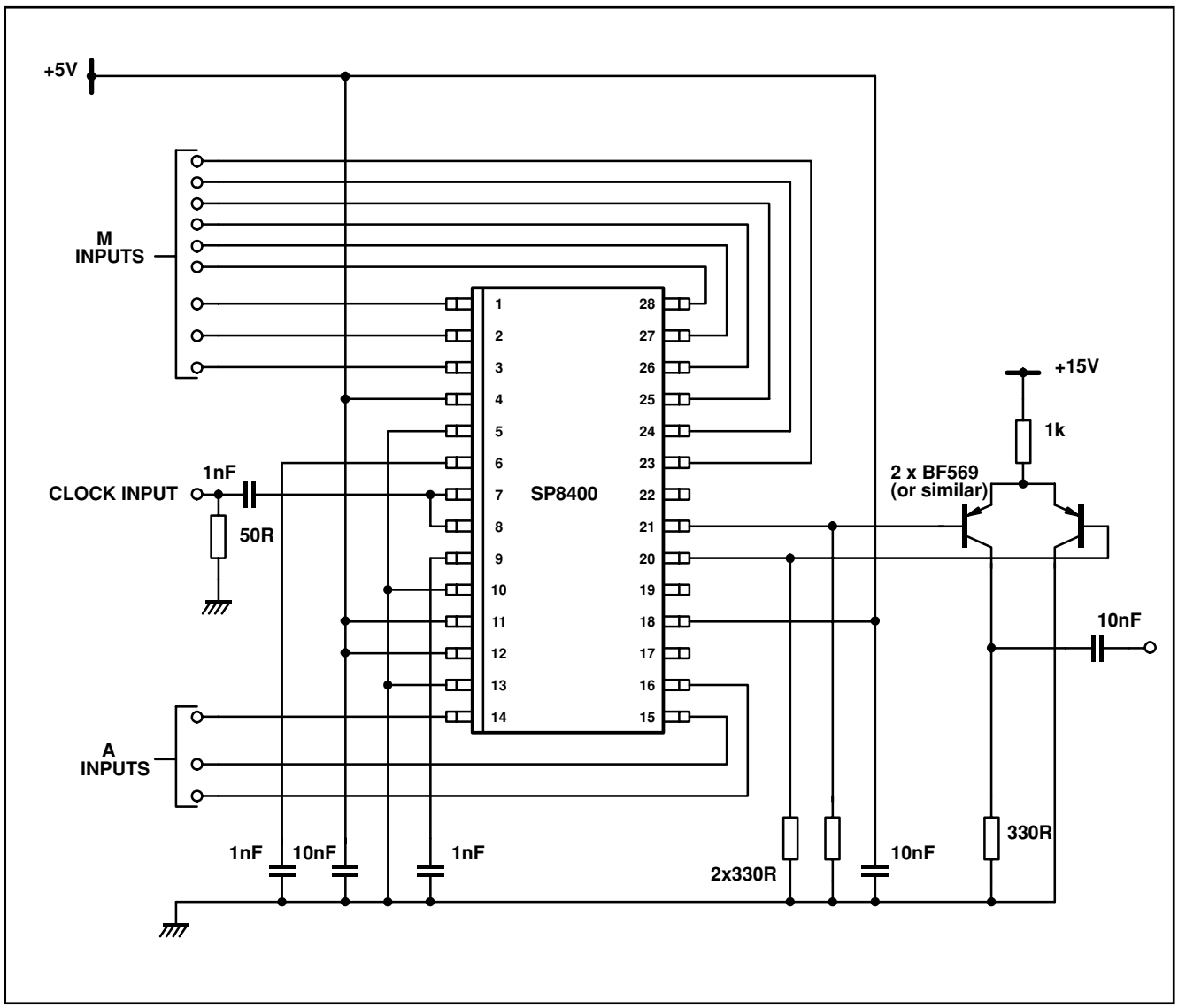

Fig.5 Typical application combining output to increase signal and retain low phase noise

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