SONiX Dual Mode Camera Processor

SN9C2028AF Specification

Released Version 1.0

Dec 31, 2003

Revision Number	Date	Description
0.91	Apr 22, 2002	A brief specification and release to Marketing
0.92	Jan 23, 2003	A preliminary specification and release to Agent
0.93	Apr 1, 2003	Modify the USB detection function in this Specification (AF version)
1.00	Dec 31, 2003	Original Specification

SN9C2028AF

DUAL MODE CAMERA PROCESSOR

1.General description:

SN9C2028AF is designed for low cost dual mode CMOS camera solution. It highly integrated single chip solution that included CMOS sensor interface, SDRAM interface, USB interface, compression engine, LCD driver, embedded 16bit DSP and low battery detection function.

This dual mode camera solution is not only for DSC function but also with the live video mode when attached to PC.

SN9C2028AF provide a solution that can makes balance both in performance and price and most flexible in function for customers design their own style.

2. Feature:

- Dual mode camera- PC camera mode and DSC mode.
- Support - Hynix- HV7131D, HV7131E (VGA) and HV7121B (CIF), Pixart-PAS202B (VGA) and PAS106B (CIF), ICMEDIA -ICM105A, ICM105B (VGA) and ICM102A (CIF), TASC- TAS5130B (VGA) and TAS5110B (CIF) CMOS image sensors.
- 9-bit CMOS image sensor raw data.
- Provide scaling and panning function.
- Built in proprietary compression engine.
- Up to 30fps @ CIF, 12fps @VGA in PC video mode.
- Support SDRAM 4Mb, 16Mb, 64Mb, 128Mb
- Embedded 16bit-DSP for camera control and USB transceiver.
- USB 1.1 compliance and support suspend mode.
- 6 USB endpoints: Control pipe, Iso chronous pipe, Bulk pipe, Interrupt pipe and Audio pipe.
- Build in 8 segment x 4 common, 1/3 bias status LCD driver.
- Embedded low battery detection function.
- Support flashlight function.
- 12MHz crystal and 3.3Volt only.
- 128 pin LQFP package.

3. Pin description:

No	PIN NAME	DIR	Driving Capability (mA)	TEST=0 (INT_ROM)	TEST=1 (EXT_ROM)	Description
1	LCD_COM0	B	4	LCD_COM0	LCD_COM0	Common 0 for LCD
2	LCD_COM1	B	4	LCD_COM1	LCD_COM1	Common 1 for LCD
3	LCD_COM2	B	4	LCD_COM2	LCD_COM2	Common 2 for LCD
4	LCD_COM3	B	4	LCD_COM3	LCD_COM3	Common 3 for LCD
5	LCD_SEG0	B	4	LCD_SEG0	LCD_SEG0	Segment0 for LCD
6	LCD_SEG1	B	4	LCD_SEG1	LCD_SEG1	Segment1 for LCD
7	LCD_SEG2	B	4	LCD_SEG2	LCD_SEG2	Segment2 for LCD
8	LCD_SEG3	B	4	LCD_SEG3	LCD_SEG3	Segment3 for LCD
9	LCD_SEG4	B	4	LCD_SEG4	LCD_SEG4	Segment4 for LCD
10	LCD_SEG5	B	4	LCD_SEG5	LCD_SEG5	Segment5 for LCD
11	LCD_SEG6	B	4	LCD_SEG6	LCD_SEG6	Segment6 for LCD
12	LCD_SEG7	B	4	LCD_SEG7	LCD_SEG7	Segment7 for LCD
13	LCD_VA	B	4	LCD_VA	LCD_VA	Voltage A for LCD
14	LCD_VB	B	4	LCD_VB	LCD_VB	Voltage B for LCD
15	LCD_VC	B	4	LCD_VC	LCD_VC	Voltage C for LCD
16	ADIO3	B	4	ADIO3	ADIO3	Audio I/O
17	GND	P				GND for I/O and core
18	VDD	P				VDD for I/O and core
19	ADIO2	B	4	ADIO2	ADIO2	Audio I/O
20	ADIO1	B	4	ADIO1	ADIO1	Audio I/O
21	ADIO0	B	4	ADIO0	ADIO0	Audio I/O
22	GPIO1	B	8	GPIO1	GPIO1	General purpose I/O
23	XVDD	P				VDD for oscillator
24	XIN	I		~CLK	~CLK	OSC input
25	XOUT	B	4	X	X	OSC output
26	XVSS	P				GND for oscillator
27	KEY0	I		KEY0	KEY0	KEY0 input (MODE)

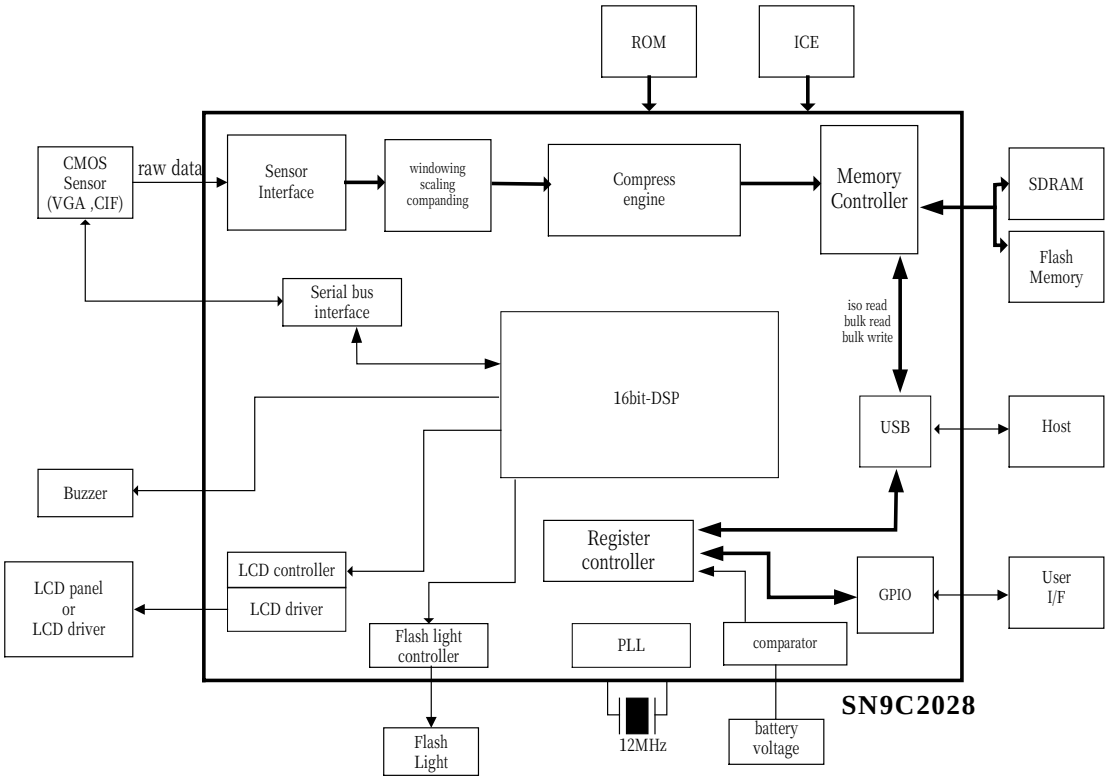
28	KEY1	I		KEY1	KEY1	KEY1 input (ENTER)
29	VA0	B	4	VA0	VA0	Address bus for SDRAM
30	VA1	B	4	VA1	VA1	Address bus for SDRAM
31	VA2	B	4	VA2	VA2	Address bus for SDRAM
32	VA3	B	4	VA3	VA3	Address bus for SDRAM
33	VDD	P				VDD for I/O and core
34	GND	P				GND for I/O and core
35	VA4	B	4	VA4	VA4	Address bus for SDRAM
36	VA5	B	4	VA5	VA5	Address bus for SDRAM
37	ROM_A3	B	4	L	ROM_A3	DSP and ROM interface
38	VA6	B	4	VA6	VA6	Address bus for SDRAM
39	ROM_A4	B	4	L	ROM_A4	DSP and ROM interface
40	VA7	B	4	VA7	VA7	Address bus for SDRAM
41	ROM_A5	B	4	L	ROM_A5	DSP and ROM interface
42	VA8	B	4	VA8	VA8	Address bus for SDRAM
43	ROM_A6	B	4	L	ROM_A6	DSP and ROM interface
44	VA9	B	4	VA9	VA9	Address bus for SDRAM
45	ROM_A7	B	4	L	ROM_A7	DSP and ROM interface
46	VA10	B	4	VA10	VA10	Address bus for SDRAM
47	ROM_A12	B	4	L	ROM_A12	DSP and ROM interface
48	VA11	B	4	VA11	VA11	Address bus for SDRAM
49	ROM_A14	B	4	L	ROM_A14	DSP and ROM interface
50	VDDS	P				VDD for I/O and core
51	ROM_A13	B	4	L	ROM_A13	DSP and ROM interface
52	GNDS	P				GND for I/O and core
53	ROM_A8	B	4	L	ROM_A8	DSP and ROM interface
54	VA12	B	4	VA12	VA12	Address bus for SDRAM
55	ROM_A9	B	4	L	ROM_A9	DSP and ROM interface
56	VA13	B	4	VA13	VA13	Address bus for SDRAM
57	ROM_A11	B	4	L	ROM_A11	DSP and ROM interface
58	VD_CS	O	4	VD_CS	VD_CS	CS for SDRAM
59	VD_RAS	O	4	VD_RAS	VD_RAS	RAS for SDRAM

60	VD_CAS	O	4	VD_CAS	VD_CAS	CAS for SDRAM
61	VD_WE	O	4	VD_WE	VD_WE	WE for SDRAM
62	VD_UDQM	O	4	VD_UDQM	VD_UDQM	UDQM for SDRAM
63	VD_LDQM	O	4	VD_LDQM	VD_LDQM	LDQM for SDRAM
64	VDD	P				VDD for I/O and core
65	GND	P				GND for I/O and core
66	VD_CLK	O	4	VD_CLK	VD_CLK	CLK for SDRAM
67	VD_CKE	O	4	VD_CKE	VD_CKE	CKE for SDRAM
68	VD3	B	4	VD3	VD3	Data bus for SDRAM
69	VD2	B	4	VD2	VD2	Data bus for SDRAM
70	VD1	B	4	VD1	VD1	Data bus for SDRAM
71	VD0	B	4	VD0	VD0	Data bus for SDRAM
72	VD4	B	4	VD4	VD4	Data bus for SDRAM
73	VD5	B	4	VD5	VD5	Data bus for SDRAM
74	VD6	B	4	VD6	VD6	Data bus for SDRAM
75	VD7	B	4	VD7	VD7	Data bus for SDRAM
76	DSPIO3	B	8	DSPIO3	DSPIO3	DSP GPIO
77	TEST0	I		0	1	Test mode
78	TEST1	I		0	0	Test mode
79	TAVSS	P				GND for USB driver
80	DN	B		DN	DN	D- for USB
81	DP	B		DP	DP	D+ for USB
82	TAVDD	P				VDD for USB driver
83	BAT_SW	B	4	BAT_SW	BAT_SW	Battery resister array switch for power down
84	BAT_DET	I		BAT_DET	BAT_DET	Low voltage detection for battery
85	AVSS	P				GND for PLL
86	AVDD	P				VDD for PLL
87	USB_DET	I		USB_DET	USB_DET	USB dectection
88	BAT_EN	O	4	BAT_EN	BAT_EN	
89	PWR_DOWN	O	4	PWR_DOWN	PWR_DOWN	Power down for whole chip

90	N_RST	I		N_RST	N_RST	Chip reset
91	FLH_TRG	O	4	FLH_TRG	FLH_TRG	Flash light trigger signal
92	DSPIO4	B	8	DSPIO4	DSPIO4	DSP GPIO
93	GPIO0	B	8	GPIO0	GPIO0	General purpose I/O
94	S_PWR_DN	O	4	S_PWR_DN	S_PWR_DN	Power down for sensor
95	VDD	P				VDD for I/O and core
96	NC					
97	GND	P				GND for I/O and core
98	SEN_CLK	O	4	SEN_CLK	SEN_CLK	Sensor clock
99	DSPIO1	B	8	DSPIO1	DSPIO1	DSP GPIO
100	ROM_A10	B	4	L	ROM_A10	DSP and ROM interface
101	DSPIO2	B	4	DSPIO2	DSPIO2	DSP GPIO
102	ROM_D7	B	4	L	ROM_D7	DSP and ROM interface
103	S_PCK	B	4	S_PCK	S_PCK	Sensor pixel clock
104	ROM_D6	B	4	L	ROM_D6	DSP and ROM interface
105	S_VSYNC	B	4	S_VSYNC	S_VSYNC	Sensor vsync
106	ROM_D5	B	4	L	ROM_D5	DSP and ROM interface
107	S_HSYNC	B	4	S_HSYNC	S_HSYNC	Sensor hsync
108	ROM_D4	B	4	L	ROM_D4	DSP and ROM interface
109	S_IMG0	I		S_IMG0	S_IMG0	Sensor image data
110	ROM_D3	B	4	L	ROM_D3	DSP and ROM interface
111	VDDS	P				VDD for I/O and core
112	ROM_D2	B	4	L	ROM_D2	DSP and ROM interface
113	GNDS	P				GND for I/O and core
114	ROM_D1	B	4	L	ROM_D1	DSP and ROM interface
115	S_IMG1	B	4	S_IMG1	S_IMG1	Sensor image data
116	ROM_D0	B	4	L	ROM_D0	DSP and ROM interface
117	S_IMG2	B	4	S_IMG2	S_IMG2	Sensor image data
118	ROM_A0	B	4	L	ROM_A0	DSP and ROM interface
119	S_IMG3	B	4	S_IMG3	S_IMG3	Sensor image data
120	ROM_A1	B	4	L	ROM_A1	DSP and ROM interface
121	S_IMG4	B	4	S_IMG4	S_IMG4	Sensor image data

122	ROM_A2	B	4	L	ROM_A2	DSP and ROM interface
123	S_IMG5	B	4	S_IMG5	S_IMG5	Sensor image data
124	S_IMG6	B	4	S_IMG6	S_IMG6	Sensor image data
125	S_IMG7	B	4	S_IMG7	S_IMG7	Sensor image data
126	S_IMG8	B	4	S_IMG8	S_IMG8	Sensor image data
127	GND	P				GND for I/O and core
128	VDD	P				VDD for I/O and core

4. Block diagram:



5. USB Description:

Endpoint #	Function	Transfer Type	MaxPsz (byte)
0	STD Commands	Control	64
1	ISO Read	ISO	0, 128, 256, 384,512,680,800,900, 1007
2	Bulk Read	Bulk	64
3	Interrupt Read	Interrupt	1
4	ISO Read	ISO	0,16
5	Bulk Write	Bulk	64

6. DC electrical characteristics:

a. Absolute maximum ratings:

Symbol	Parameter	Rating	Units
Vcc	Power Supply	-0.3 to 3.6	V
Vin	Input Voltage	-0.3 to Vcc+0.3	V
Vout	Output Voltage	-0.3 to Vcc+0.3	V
Tstg	Storage Temperature	-55 to 150	°C

b. Recommended operating conditions:

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Power Supply	3.0	3.3	3.6	V
Vin	Input voltage	0		Vcc	V
Topr	Operating Temperature	0		70	°C

c. DC electrical characteristics:

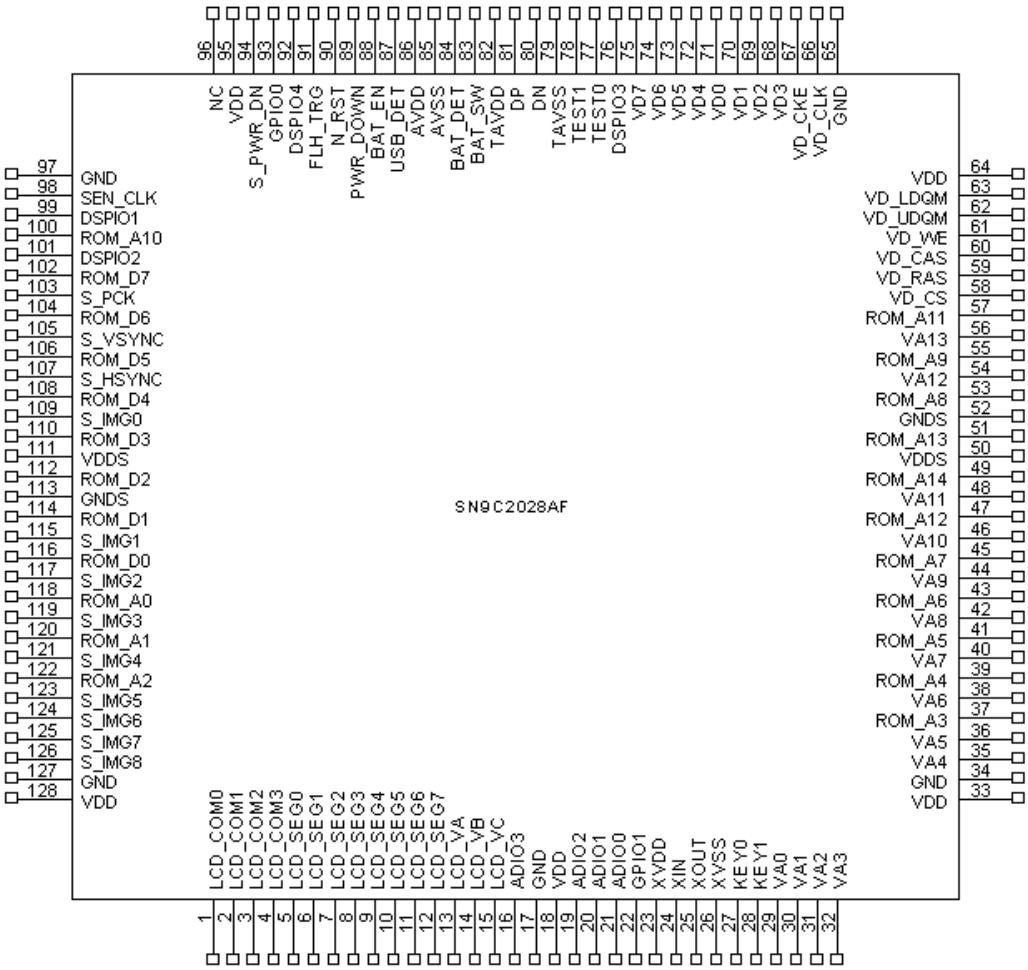
(Under Recommended Operating Conditions and Vcc=3.0 ~ 3.6V, Tj=0 to +115 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input low voltage	LVTTL	-0.3		0.8	V
Vih	Input high voltage	LVTTL	2.0		Vcc+0.3	V
Iil	Input low current	No pull-up or pull-down	-1		1	uA

Iih	Input high current	No pull-up or pull-down	-1		1	uA
Ioz	Tri-state leakage current		-1		1	uA
Vol	Output Low voltage	*			0.4	V
Voh	Output high voltage	*	2.4			V
Cin	Input capacitance			2.8		pF
Cout	Output capacitance		2.7		4.9	pF
Cbid	Bi-directional buffer Capacitance		2.7		4.9	pF

* : Maximum output current 4mA or 8mA I/O pin.

6. Pin Assignment:



8. Package outline- LQFP128