12-BIT SCHOTTKY BARRIER DIODE BUS TERMINATOR

Features

- 24 integrated diodes in a single package offers 12 channel, dual rail clamping action
- Provides proper bus termination independent of external line or card loading conditions
- Schottky diode technology; excellent forward voltage and reverse recovery characteristics
- Enhanced performance over existing device
- 16-pin SOIC package

Applications

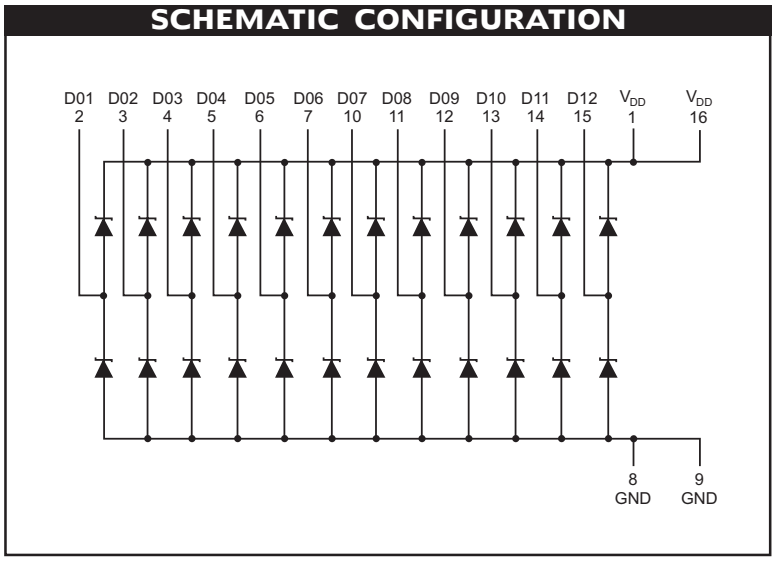
- Local high speed bus termination for all popular RISC and embedded microprocessor applications
- High speed memory and SDRAM memory bus termination

Product Description

Reflections on high speed data lines lead to undershoot and overshoot disturbances which may result in improper system operation. Resistor terminations, when used to terminate high speed data lines, increase power consumption and degrade output (high) levels resulting in reduced noise immunity. Schottky diode termination is the best overall solution for applications in which power consumption and noise immunity are critical considerations.

This integrated Schottky diode network provides very effective termination performance for high speed data lines under variable loading conditions. The device supports up to 12 terminated lines per package — each of which can be simultaneously clamped to both ground and power supply rail.

SCHEMATIC CONFIGURATION



C0220298D

STANDARD SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating
Supply Voltage	V_{DD}	-0.3V to +7V
Channel clamp current (continuous)	I_{clamp}	±50mA
Operating Temperature		0°C to 70°C
Storage Temperature	Tstg	-65°C to +150°C
Package Power Rating		625mW, max.

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing the device to its absolute maximum rating may affect its reliability.

DIODE CHARACTERISTICS (T_A = 0° to 70°C)

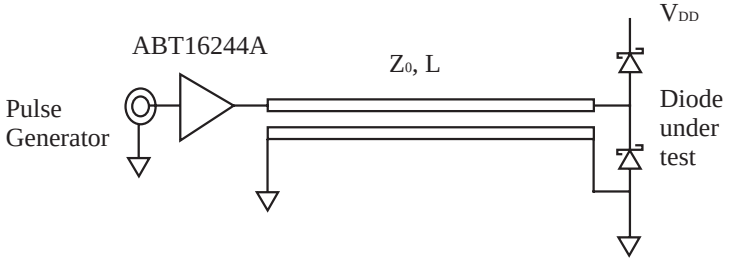
Parameter	Conditions		Min	Typ	Max
Diode foward voltage	To V_{DD}	I_F = 16 mA		0.55V	0.70V
		I_F = 50 mA	0.55V	0.70V	0.90V
	From GND	I_F = 16 mA		0.50V	0.65V
		I_F = 50 mA	0.50V	0.65V	0.85V
Reverse Recovery Time (See Note 1)	I_F = 50mA (estimated)				<400pS
Channel leakage	$0 \le V_{IN} \le V_{DD}$			0.1μA	5μA
Input Capacitance	f = 1 MHz, V_{IN} = 2.5V, T_A = 25°C, V_{DD} = 5.0V			5pF	
ESD Protection	MIL-STD-883, Method 3015		4KV		

STANDARD PART ORDERING INFORMATION

Package		Ordering Part Number		
Pins	Style	Tubes	Tape & Reel	Part Marking
16	SOIC Narrow	SN 74S1051/T	SN 74S1051/R	SN 74S1051

Note 1:

The test circuit depicts the Schottky diodes in their typical application. The impact of a reverse recovery time is measured using a narrow pulse with 670- pS rise and fall times. This pulse propagates down a 60 cm, 54 ohm strip line fabricated on a multi-layer, controlled impedance printed circuit board. In testing the ground clamp diode, the negative going edge of the pulse causes a reflection which forces the diode under test to become forward biased. The positive going edge of the pulse attempts to pull this diode out of forward conduction. A reverse recovery phenomenon would cause a delay between the known arrival time of the positive edge and the observed edge due to the time it takes for the forward biased diode to actually become reversed biased. In this measurement, however, there is no observable difference and therefore no delay for the positive edge due to the presence of the diode. The waveforms are adjusted to individually test the ground and V_{DD} clamps. See test circuit.



Test Circuit. Line length, pulse width and duty cycle are selected such as that only one reflection is involved in the measurement.