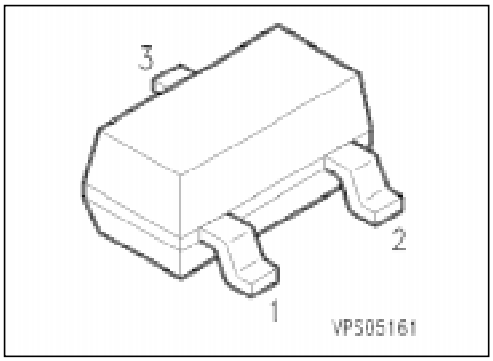
SIEMENS

NPN Silicon Darlington Transistor — SMBT 6427

- For general amplifier applications
- High collector current
- High current gain



Type	Marking	Ordering Code (tape and reel)	Pin Configuration 1	2	3	Package[1]
SMBT 6427	s1V	Q68000-A8320	B	E	C	SOT-23

Maximum Ratings

Parameter	Symbol	Values	Unit
Collector-emitter voltage	V_{CE0}	40	V
Collector-base voltage	V_{CB0}	40	
Emitter-base voltage	V_{EB0}	12	
Collector current	I_C	500	mA
Peak collector current	I_{CM}	800	
Total power dissipation, T_S = 74 ˚C	P_{tot}	360	mW
Junction temperature	T_j	150	˚C
Storage temperature range	T_{stg}	– 65 … + 150	

Thermal Resistance

Junction - ambient[2]	$R_{th\ JA}$	≤ 280	K/W
Junction - soldering point	$R_{th\ JS}$	≤ 210	

1) For detailed information see chapter Package Outlines.

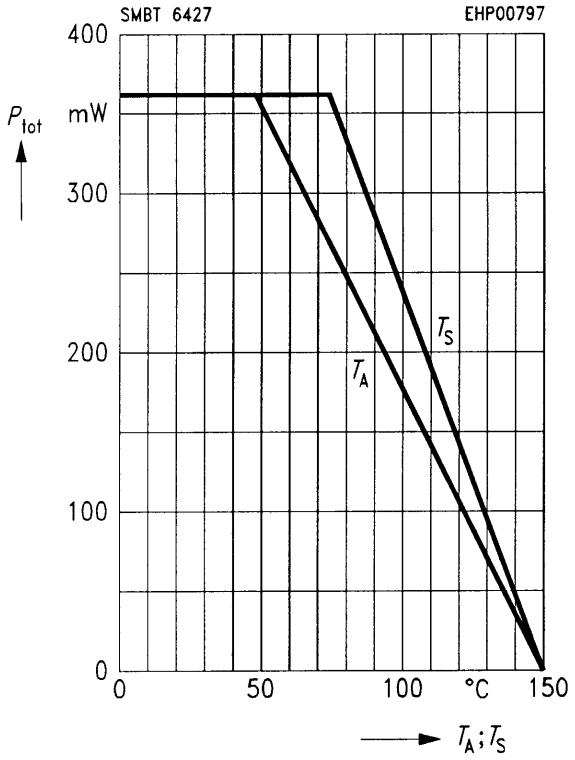
2) Package mounted on epoxy pcb 40 mm × 40 mm × 1.5 mm/6 cm² Cu.

Electrical Characteristics
at T_A = 25 °C, unless otherwise specified.

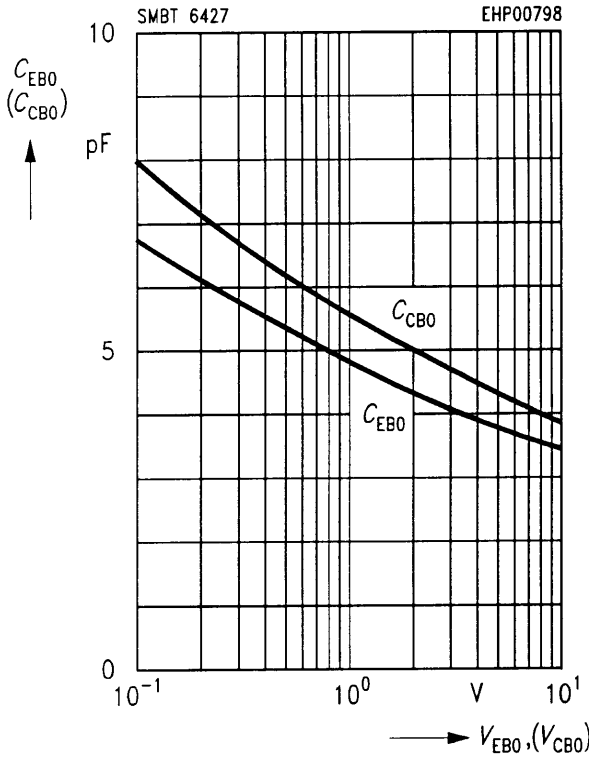
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Collector-emitter breakdown voltage I_C = 10 mA	$V_{(BR)CE0}$	40	–	–	V
Collector-base breakdown voltage I_C = 100 µA	$V_{(BR)CB0}$	40	–	–	
Emitter-base breakdown voltage, I_E = 10 µA	$V_{(BR)EB0}$	12	–	–	
Collector-base cutoff current V_{CB} = 30 V, I_E = 0 V_{CB} = 30 V, I_E = 0, T_A = 150 °C	I_{CB0}	 – –	 – –	 50 10	 nA µA
Collector cutoff current V_{CE} = 30 V, I_B = 0	I_{CE0}	–	–	1	µA
Emitter-base cutoff current V_{EB} = 10 V, I_C = 0	I_{EB0}	–	–	50	nA
DC current gain I_C = 10 mA, V_{CE} = 5 V I_C = 100 mA, V_{CE} = 5 V I_C = 500 mA, V_{CE} = 5 V	h_{FE}	 10000 20000 14000	 – – –	 100000 200000 140000	–
Collector-emitter saturation voltage[1)] I_C = 50 mA, I_B = 0.5 mA I_C = 500 mA, I_B = 0.5 mA	V_{CEsat}	 – –	 – –	 1.2 1.5	V
Base-emitter saturation voltage[1)] I_C = 500 mA, I_B = 0.5 mA	V_{BEsat}	–	–	2.0	
Base-emitter voltage I_C = 50 mA, V_{CE} = 5 V	$V_{BE(on)}$	–	–	1.75	
AC characteristics					
Transition frequency I_C = 50 mA, V_{CE} = 5 V, f = 100 MHz	f_T	130	–	–	MHz
Output capacitance V_{CB} = 10 V, f = 1 MHz	C_{obo}	–	–	7	pF
Input capacitance V_{EB} = 0.5 V, f = 1 MHz	C_{ibo}	–	–	25	
Noise figure I_C = 1 mA, V_{CE} = 5 V, R_S = 100 kΩ f = 1 kHz to 15 kHz	NF	–	–	10	dB

1) Pulse test conditions: $t \leq 300$ µs, $D \leq 2$ %.

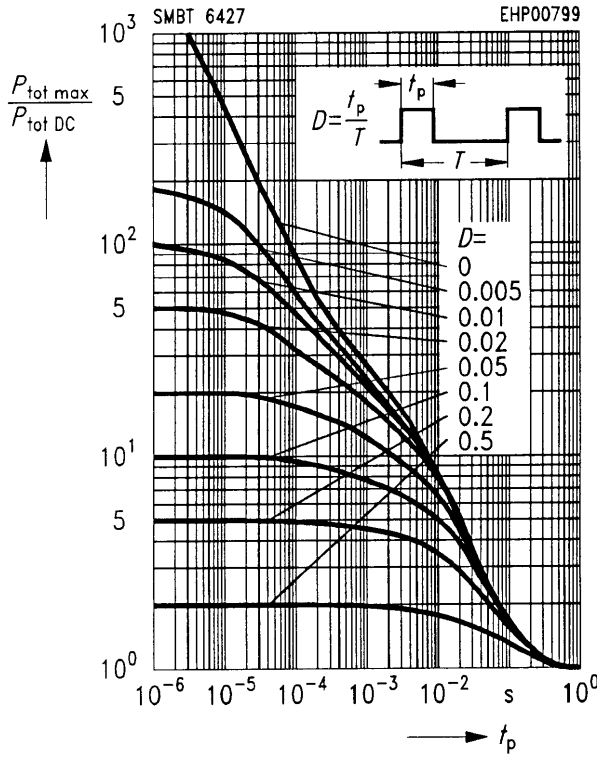
Total power dissipation $P_{tot} = f(T_A^*; T_S)$
* Package mounted on epoxy



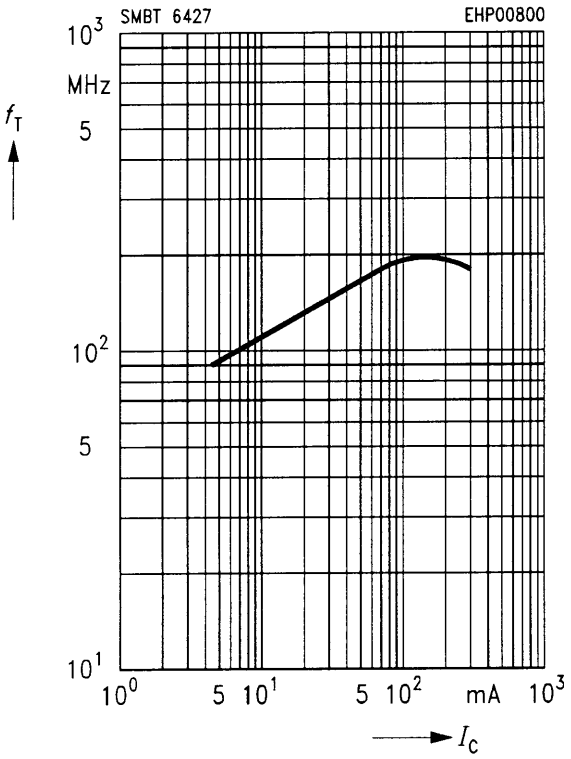
Collector-base capacitance $C_{CB0} = f(V_{CB0})$
Emitter-base capacitance $C_{EB0} = f(V_{EB0})$



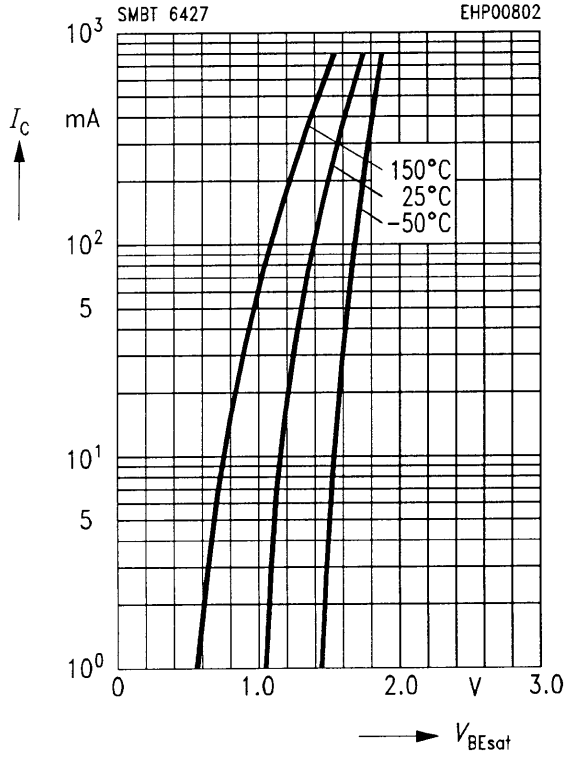
Permissible pulse load $P_{tot\,max}/P_{tot\,DC} = f(t_p)$



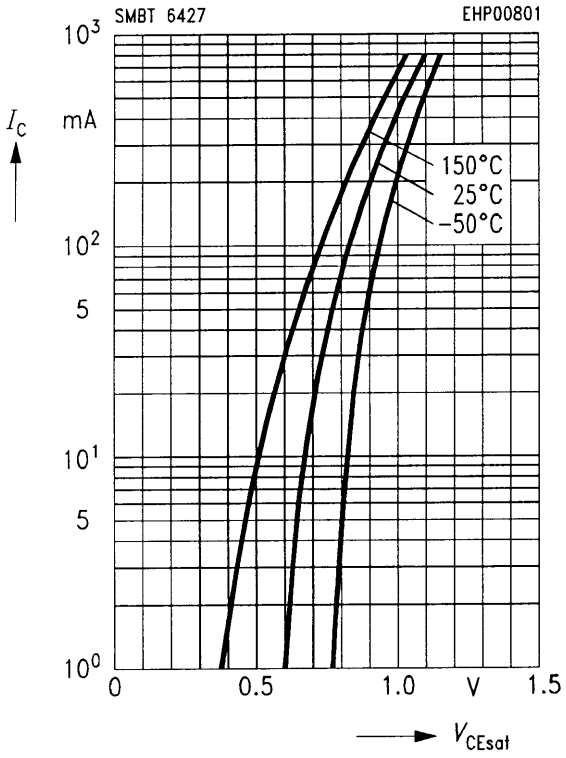
Transition frequency $f_T = f(I_C)$
V_{CE} = 5 V



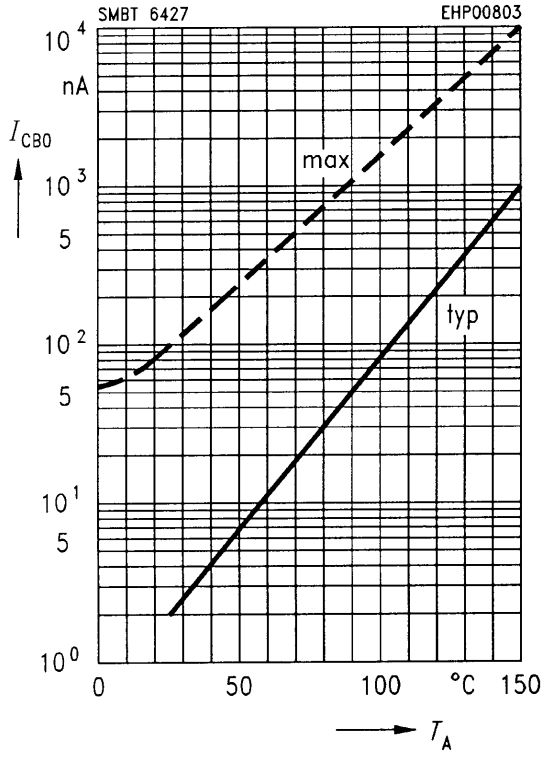
Base-emitter saturation voltage
$I_C = f(V_{BE\,sat})$, $h_{FE} = 1000$



Collector-emitter saturation voltage
$I_C = f(V_{CE\,sat})$, $h_{FE} = 1000$



Collector cutoff current $I_{CB0} = f(T_A)$
$V_{CB} = V_{CE\,max}$



DC current gain $h_{FE} = f(I_C)$
$V_{CE} = 5$ V