

SL74HCT240

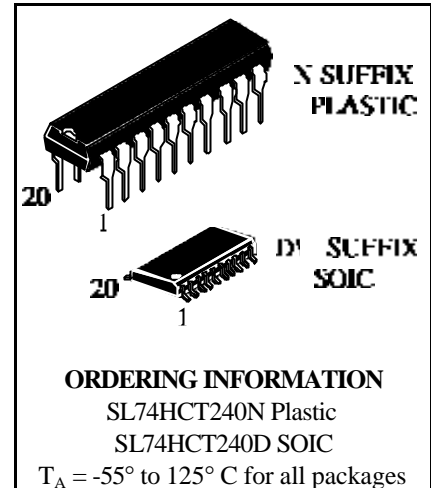
Octal 3-State Inverting Buffer/Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

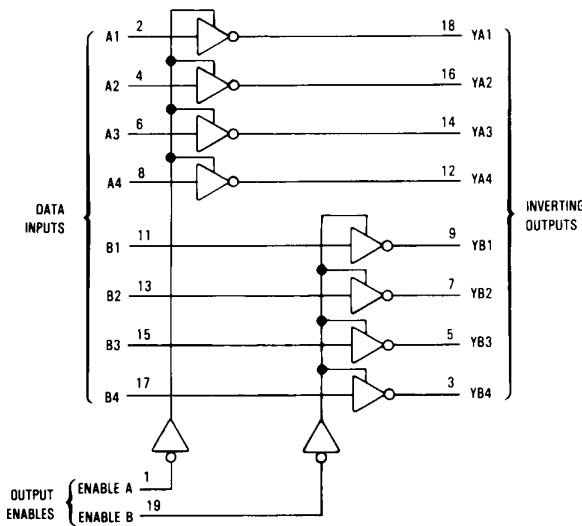
The SL74HCT240 is identical in pinout to the LS/ALS240. The SL74HCT240 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This octal inverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A



LOGIC DIAGRAM



PIN 20 = V_{CC}
 PIN 10 = GND

PIN ASSIGNMENT

ENABLE A	1	20	V_{CC}
A1	2	19	ENABLE B
YB1	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	1	B1

FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A,B	YA,YB
L	L	H
L	H	L
H	X	Z

X = don't care
 Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 +Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
 SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

SL74HCT240

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V I _{OUT} ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = V _{CC} -0.1 V I _{OUT} ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IL} I _{OUT} ≤ 20 μA	4.5	4.4	4.4	4.4	V
		5.5	5.4	5.4	5.4		
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IL} I _{OUT} ≤ 6.0 mA	4.5	3.98	3.84	3.7	V
		5.5	0.1	0.1	0.1		
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} I _{OUT} ≤ 20 μA	4.5	0.1	0.1	0.1	V
		5.5	0.1	0.1	0.1		
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} I _{OUT} ≤ 6.0 mA	4.5	0.26	0.33	0.4	V
		5.5	0.26	0.33	0.4		
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum three State Leakage Current	Output in High-Impedance State V _{IN} = V _{IL} or V _{IH} V _{OUT} =V _{CC} or GND	5.5	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	5.5	4.0	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{IN} = 2.4 V, Any One Input V _{IN} =V _{CC} or GND, Other Inputs I _{OUT} =0μA	5.5	≥-55°C	25°C to 125°C		mA
				2.9	2.4		

NOTE: Total Supply Current = I_{CC} + ΣΔI_{CC}

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	20	25	30	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	28	35	42	ns
t_{PZH} , t_{PZL}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	25	31	38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{IN}	Maximum Input Capacitance	10	10	10	pF
C_{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Enable Output)	Typical @25°C, $V_{CC}=5.0\text{ V}$		pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	55		

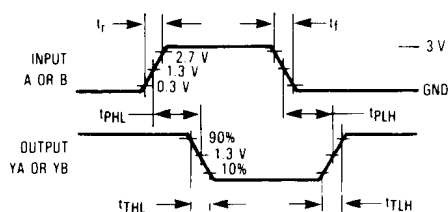


Figure 1. Switching Waveforms

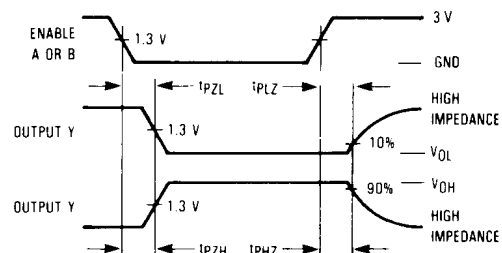
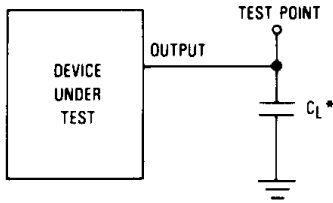
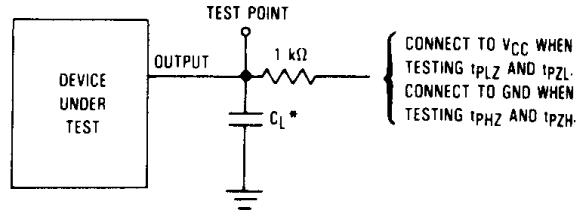


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM

(1/8 of the Device)

