

# Quad 2-Input AND Gate

## High-Performance Silicon-Gate CMOS

The SL74HCT08 may be used as a level converter for intertacing TTL or NMOS outputs to high-speed CMOS inputs.

The SL74HCT08 is identical in pinout to the LS/ALS08.

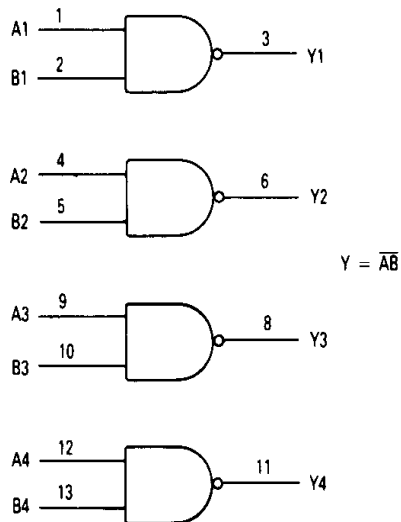
- TTL/NMOS-Compatible Input Levels.
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A

**N SUFFIX PLASTIC**

**D SUFFIX SOIC**

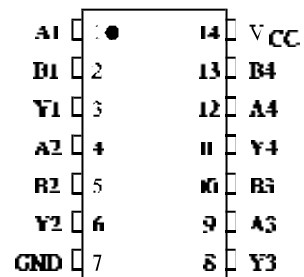
**ORDERING INFORMATION**  
 SL74HCT08N Plastic  
 SL74HCT08D SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



PIN 14 =  $V_{CC}$   
 PIN 7 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

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## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.



## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> =0.1 V   I <sub>OUT</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub>   I <sub>OUT</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
		V <sub>IN</sub> =V <sub>IH</sub>   I <sub>OUT</sub>   ≤ 4.0 mA	5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA	5.5	0.1	0.1	0.1	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	5.5	1.0	10	40	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>IN</sub> = 2.4 V, Any One Input V <sub>IN</sub> =V <sub>CC</sub> or GND, Other Inputs I <sub>OUT</sub> =0μA	5.5	≥-55°C	25°C to 125°C		mA
				2.9	2.4		

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## AC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5.0\text{ V} \pm 10\%$ , $C_L=50\text{ pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	Guaranteed Limits			Unit
		25 °C to -55°C	≤85°C	≤125°C	
$t_{PLH}, t_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	19	24	28	ns
$t_{TLH}, t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
$C_{IN}$	Maximum Input Capacitance	10	10	10	pF

$C_{PD}$	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C, $V_{CC}=5.0\text{ V}$		pF
		20		

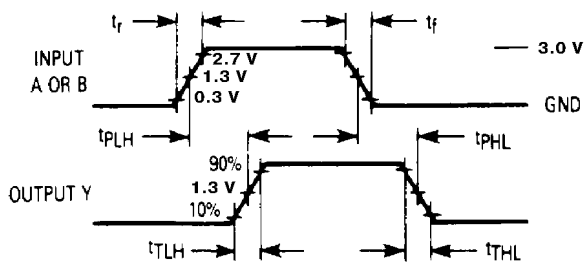
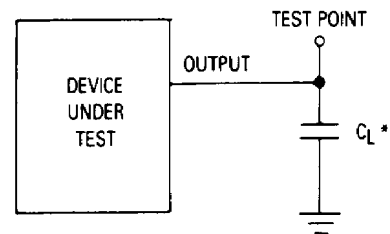


Figure 1. Switching Waveforms.



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM (1/4 of the Device)

