

# Dual 2-Bit Transparent Latch

## High-Performance Silicon-Gate CMOS

The SL74HC75 is identical in pinout to the LS/ALS75. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device consists of two independent 2-bit transparent latches and can be used as temporary storage for binary information between processing units and input/output or indicator units. Each latch stores the input data while Latch Enable is at a logic low. The outputs follow the data inputs when Latch Enable is at a logic high.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices

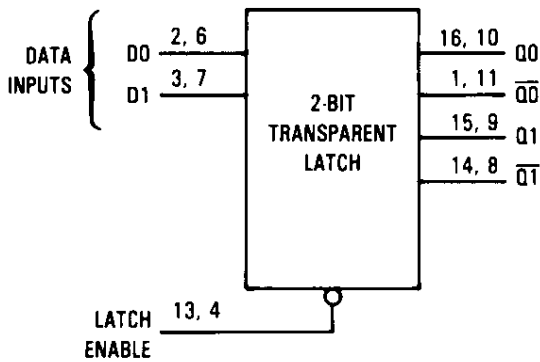


**V SUFFIX PLASTIC**

**D SUFFIX SOIC**

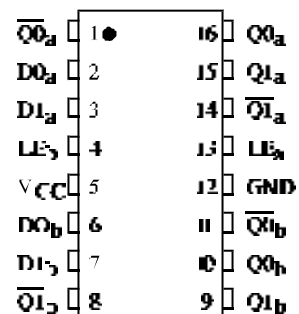
**ORDERING INFORMATION**  
 SL74HC75N Plastic  
 SL74HC75D SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



PIN 5 =  $V_{CC}$   
 PIN 12 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Outputs	
D	Latch Enable	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q0	$\overline{Q0}$

X = Don't Care  
 Q0 = latched data

# SL74HC75

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)			
	V <sub>CC</sub> =2.0 V	0	1000	ns
	V <sub>CC</sub> =4.5 V	0	500	
	V <sub>CC</sub> =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	4.0	40	80	μA

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## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub>=50pF, Input t<sub>r</sub>=t<sub>f</sub>=6.0 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, D to Q (Figures 1 and 5)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, D to Q̄ (Figures 1 and 5)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Q̄ (Figures 2 and 5)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>IN</sub>	Maximum Input Capacitance	-	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Latch)	Typical @25°C, V <sub>CC</sub> =5.0 V			pF
	Used to determine the no-load dynamic power consumption: P <sub>D</sub> =C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f+I <sub>CC</sub> V <sub>CC</sub>	35			

## TIMING REQUIREMENTS (C<sub>L</sub>=50pF, Input t<sub>r</sub>=t<sub>f</sub>=6.0 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>SU</sub>	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>H</sub>	Minimum Hold Time, Latch Enable to D (Figure 4)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable Input (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

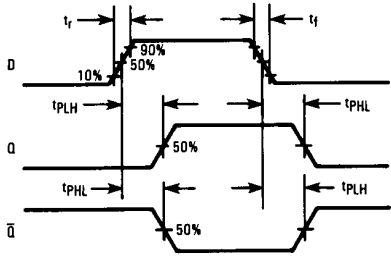


Figure 1. Switching Waveforms

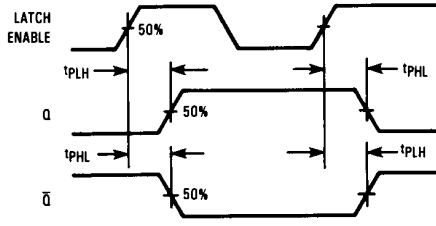


Figure 2. Switching Waveforms

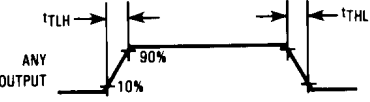


Figure 3. Switching Waveforms

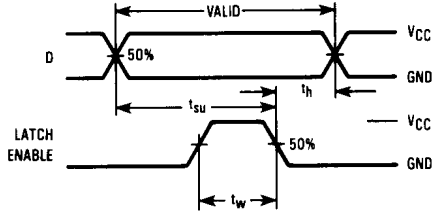
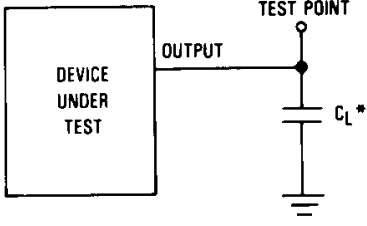


Figure 4. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM

