

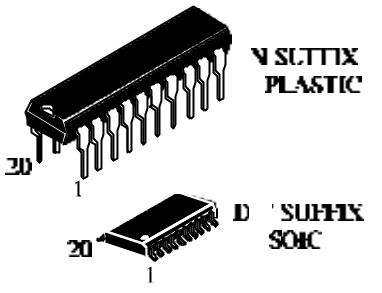
## Octal 3-State Noninverting Bus Transceiver

### High-Performance Silicon-Gate CMOS

The SL74HC623 is identical in pinout to the LS/ALS623. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

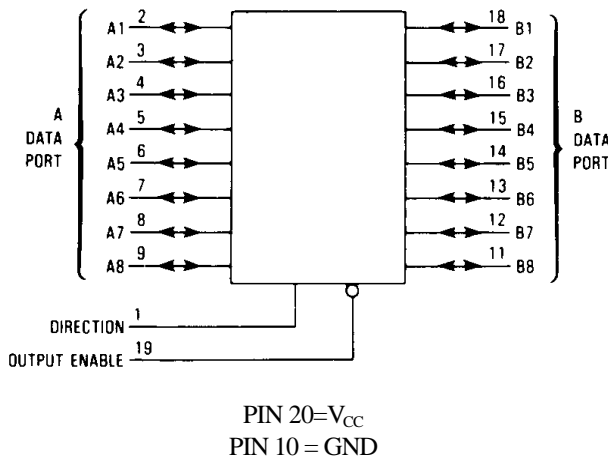
The SL74HC623 is a 3-state noninverting transceiver that is used for 2-way communication between data buses. Two separate enables are available. The enable for bus A to B is active-high, the enable for bus B to A is active-low.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices



**ORDERING INFORMATION**  
 SL74HC623N Plastic  
 SL74HC623D SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



### PIN ASSIGNMENT

DIRECTION	1	20	$V_{CC}$
A1	2	19	OUTPUT ENABLE
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

### FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	L	Buses Isolated
L	H	(High Impedance State)

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 +Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
 SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)			
	V <sub>CC</sub> =2.0 V	0	1000	ns
	V <sub>CC</sub> =4.5 V	0	500	
	V <sub>CC</sub> =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.



# SL74HC623

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.7	
6.0	5.48		5.34	5.2			
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5	0.26	0.33	0.4	
6.0	0.26		0.33	0.4			
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND, Pin 1 or 19	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND, I/O Pins	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	8.0	80	160	μA

## AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to B , B to A (Figures 1 and 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>PLZ</sub> , t <sub>PZH</sub>	Maximum Propagation Delay , Direction or Output Enable to A or B (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay , Direction or Output Enable to A or B (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>IN</sub>	Maximum Input Capacitance (Pin 1 or Pin 19)	-	10	10	10	pF
C <sub>OUT</sub>	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	-	15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @25°C, V <sub>CC</sub> =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	40			

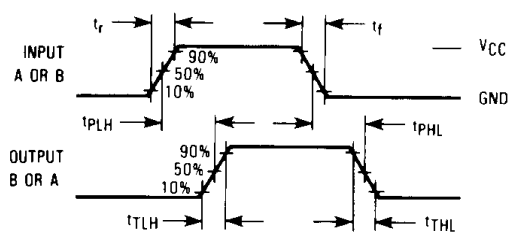


Figure 1. Switching Waveforms

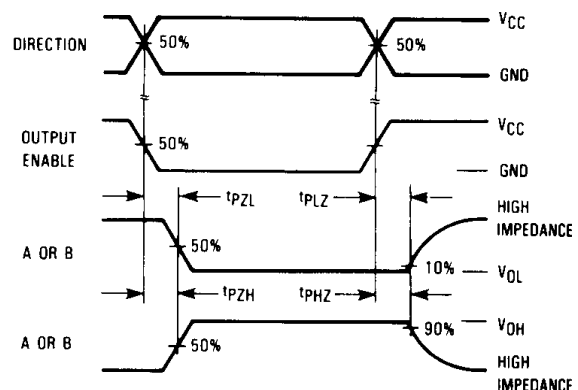
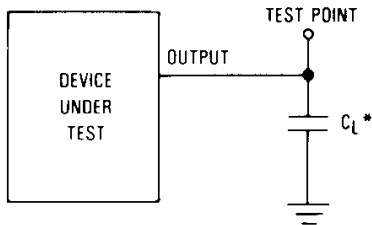
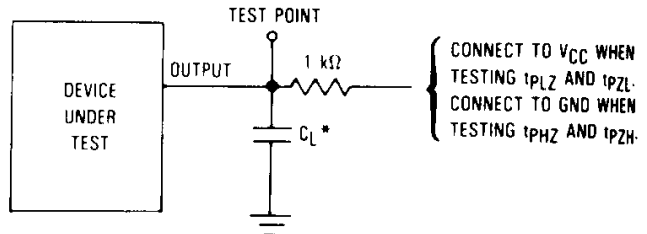


Figure 2. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 3. Test Circuit



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM

