

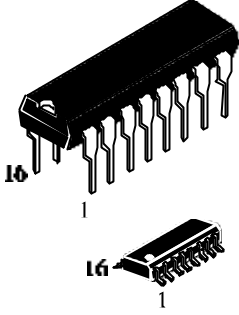
## 8-Bit Serial or Parallel-Input/ Serial-Output Shift Register with Input Latch

### High-Performance Silicon-Gate CMOS

The SL74HC597 is identical in pinout to the LS/ALS597. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device consists of an 8bit input latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table).

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices

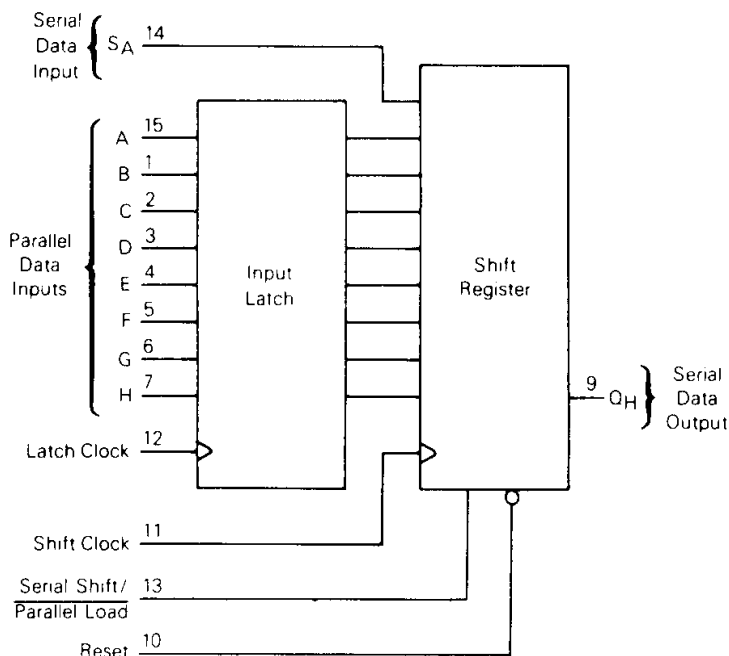


**V SUFFIX PLASTIC**

**D SUFFIX SOIC**

**ORDERING INFORMATION**  
 SL74HC597N Plastic  
 SL74HC597D SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



PIN 16 =  $V_{CC}$   
 PIN 8 = GND

### PIN ASSIGNMENT

R	1	16	$V_{CC}$
C	2	15	A
D	3	14	SA
E	4	13	Serial Shift/ Parallel Load
F	5	12	Latch Clock
G	6	11	Shift Clock
H	7	10	Reset
GND	8	9	$Q_H$

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 +Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
 SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)			
	V <sub>CC</sub> =2.0 V	0	1000	ns
	V <sub>CC</sub> =4.5 V	0	500	
	V <sub>CC</sub> =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	8.0	80	160	μA

## AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
$f_{max}$	Minimum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
$t_{PLH}, t_{PHL}$	Maximum Propagation Delay, Latch Clock to $Q_H$ (Figures 1 and 8)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
$t_{PLH}, t_{PHL}$	Maximum Propagation Delay, Shift Clock to $Q_H$ (Figures 2 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
$t_{PHL}$	Maximum Propagation Delay, Reset to $Q_H$ (Figures 3 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
$t_{PLH}, t_{PHL}$	Maximum Propagation Delay, Serial Shift/ Parallel Load to $Q_H$ (Figures 4 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
$t_{TLH}, t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{IN}$	Maximum Input Capacitance	-	10	10	10	pF
$C_{PD}$	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C, $V_{CC}=5.0\text{ V}$			pF	
		50				

## TIMING REQUIREMENTS ( $C_L=50\text{pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
$t_{su}$	Minimum Setup Time, Parallel Data Inputs A-H to Latch Clock (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_{su}$	Minimum Setup Time, Serial Data Input $S_A$ to Shift Clock (Figure 6)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_{su}$	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_h$	Minimum Hold Time, Latch Clock to Parallel Data Inputs A-H (Figure 5)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
$t_h$	Minimum Hold Time, Shift Clock to Serial Data Input $S_A$ (Figure 6)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_w$	Minimum Pulse Width, Latch Clock and Shift Clock (Figures 1 and 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Reset (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Reset	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S <sub>A</sub>	Parallel Inputs A-H	Latch Contents	Shift Register Contents	Output Q <sub>H</sub>
Reset shift register	L	X		X	X	X	U	L	L
Reset shift register; load parallel data into data latch	L	X		X	X	a-h	a-h	L	L
Load parallel data into data latch	H	H			X	a-h	a-h	U	U
Transfer latch contents to shift register	H	L		X	X	X	U	LR <sub>N</sub> → SR <sub>N</sub>	LR <sub>H</sub>
Contents of data latch and shift register are unchanged	H	H			X	X	U	U	U
Load parallel data into data latch and shift register	H	L		X	X	a-h	a-h	a-h	h
Shift serial data into shift register	H	H	X		D	X	*	SR <sub>A</sub> =D; SR <sub>N</sub> → SR <sub>N+1</sub>	SR <sub>G</sub> → SR <sub>H</sub>
Load parallel data into data latch and shift serial data into shift register	H	H			D	a-h	a-h	SR <sub>A</sub> =D; SR <sub>N</sub> → SR <sub>N+1</sub>	SR <sub>G</sub> → SR <sub>H</sub>

SR = shift register contents  
 LR = latch register contents  
 D = data (L,H) at serial data input S<sub>A</sub>  
 U = remains unchanged

X = don't care  
 a-h = data at parallel data inputs A-H  
 \* = depends on Latch Clock input

**INPUTS:**

**A, B, C, D, E, F, G, H** - Parallel data inputs. Data on these inputs is stored in the input latch on the rising edge of the Latch Clock input.

**S<sub>A</sub>** - Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

**SERIAL SHIFT/PARALLEL LOAD** - Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the input latch, and serial shifting is inhibited.

**RESET** - Asynchronous, Active-low shift register reset. A low level applied to this input resets the shift register to a low level, but does not change the data in the input latch.

**SHIFT CLOCK** - Serial shift register clock. A low-to-high transition on this input shifts data on the Serial Data Input into the shift register and data in stage H is shifted out Q<sub>H</sub>, being replaced by the data previously stored in stage G.

**LATCH CLOCK** - A low-to-high transition on this input loads the parallel data on inputs A-H into the input latch.

**OUTPUT:**

**Q<sub>H</sub>** - Serial data output. This pin is the output from the last stage of the shift register.

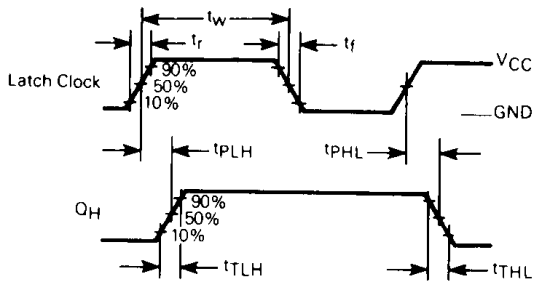


Figure 1. (Serial Shift/Parallel Load = L)

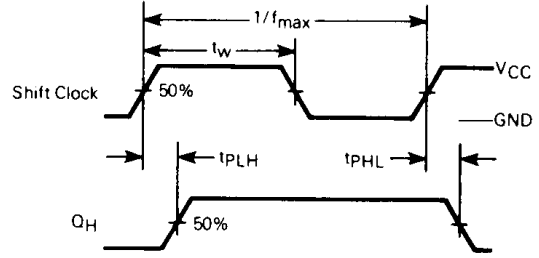


Figure 2. (Serial Shift/Parallel Load = H)

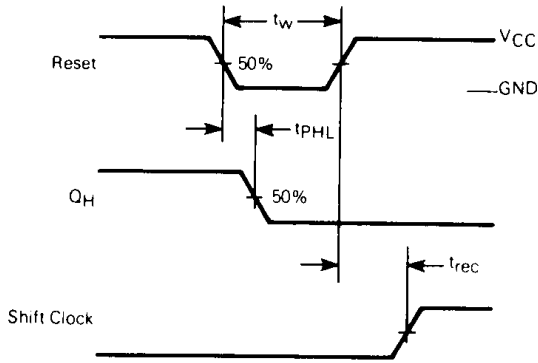


Figure 3. Switching Waveforms

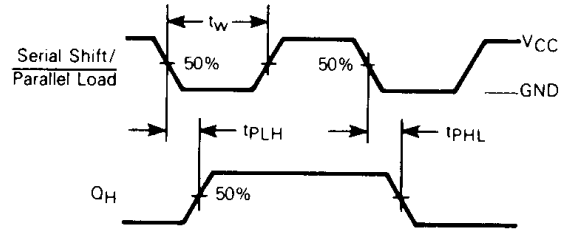


Figure 4. Switching Waveforms

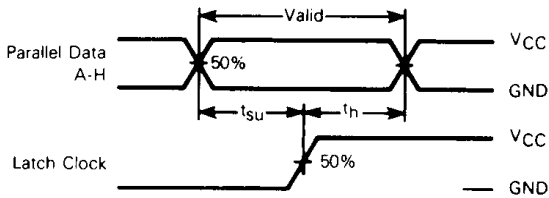


Figure 5. Switching Waveforms

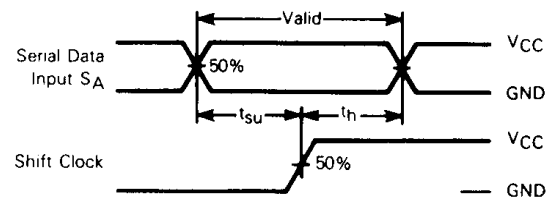


Figure 6. Switching Waveforms

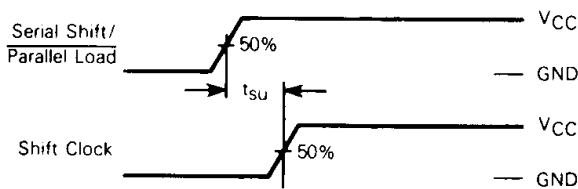
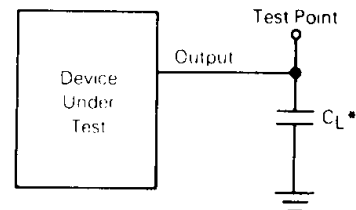


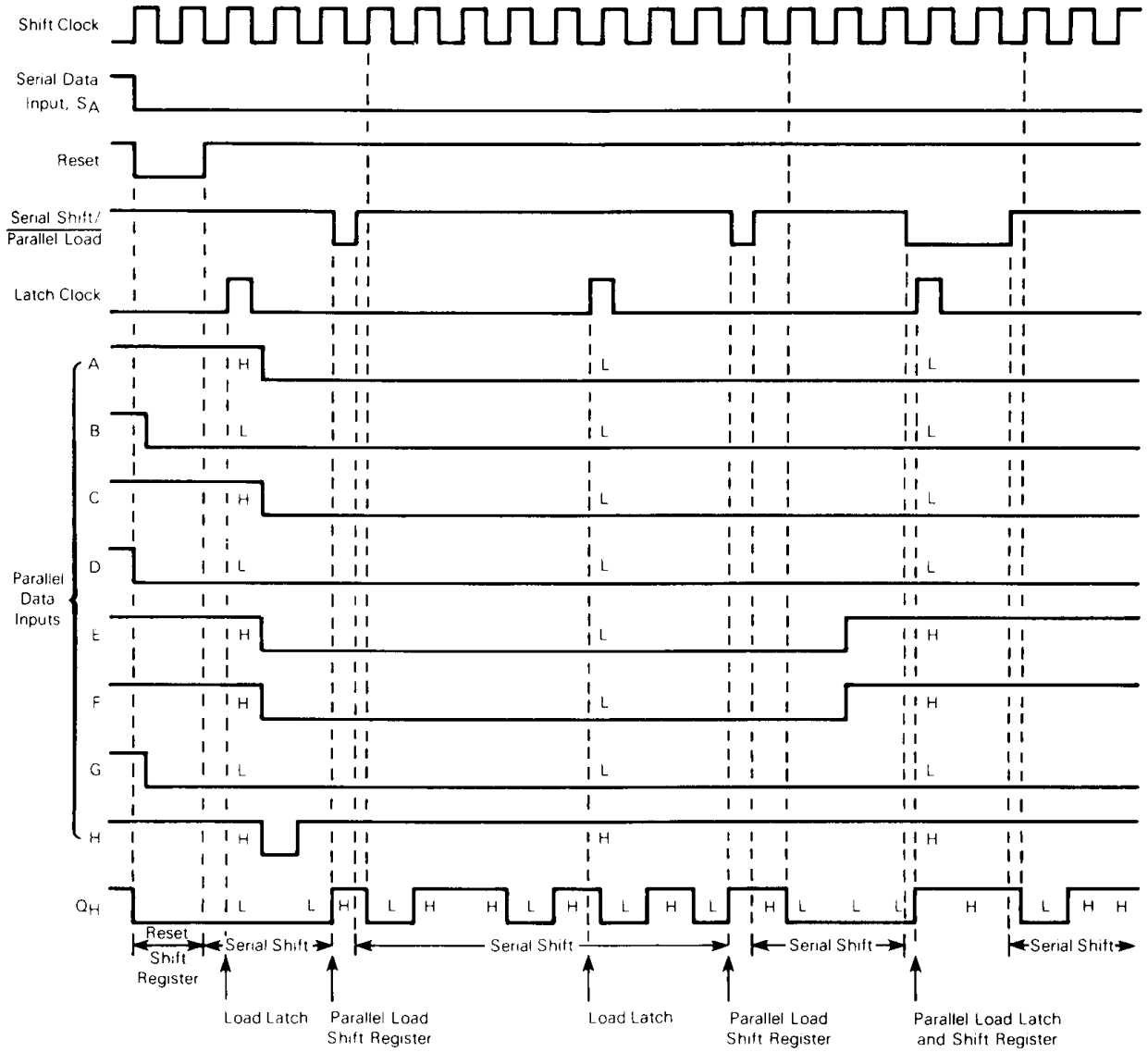
Figure 7. Test Circuit



\* Includes all probe and jig capacitance

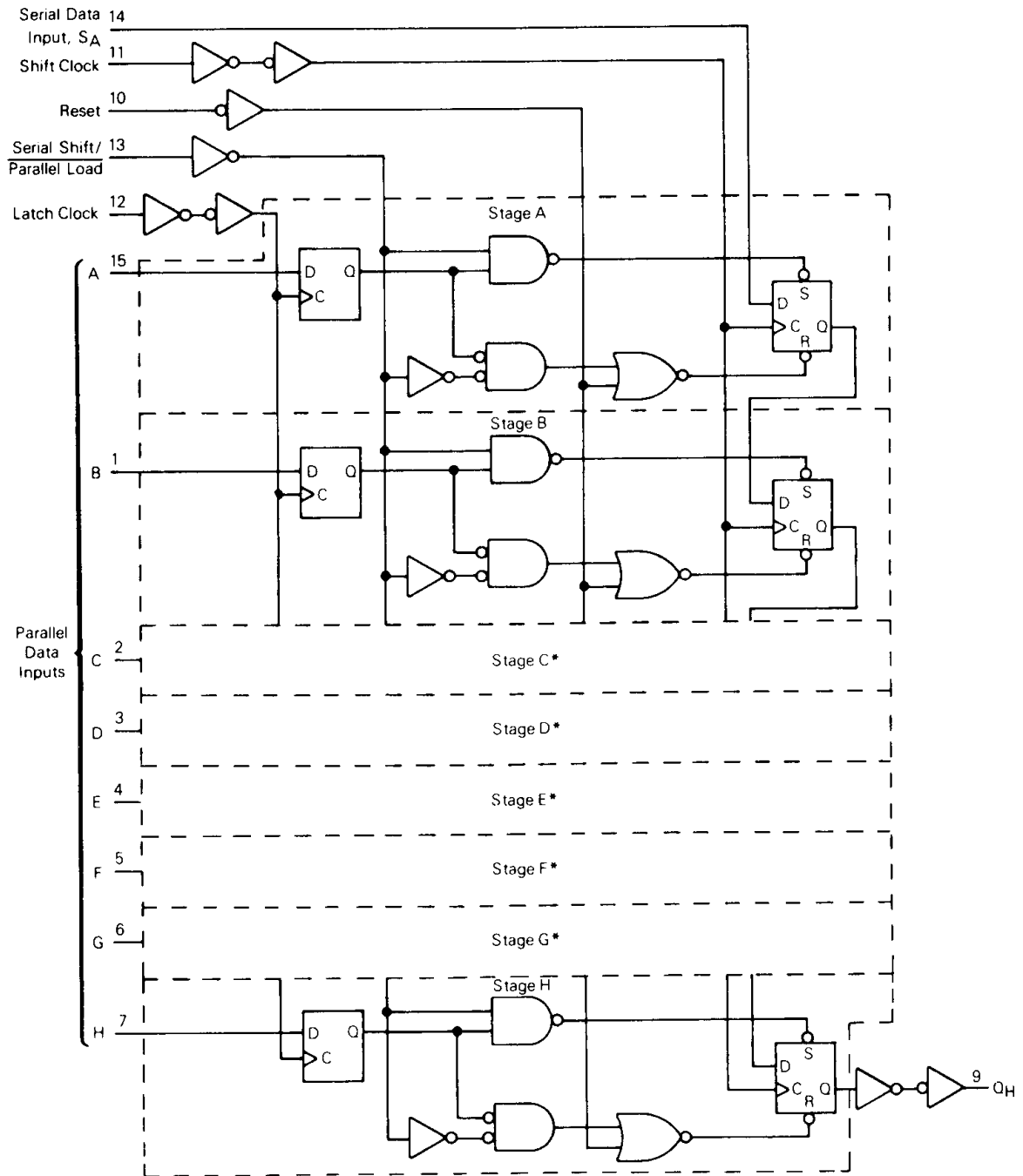
Figure 8. Test Circuit

TIMING DIAGRAM





## EXPANDED LOGIC DIAGRAM



\*NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.