

# Analog Multiplexer Demultiplexer

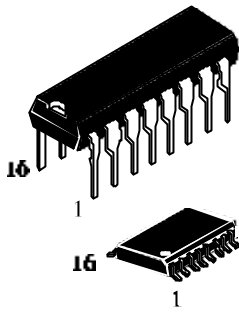
## High-Performance Silicon-Gate CMOS

The SL4053B analog multiplexer/demultiplexer is digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20V (if  $V_{CC} - GND = 3V$ , a  $V_{CC} - V_{EE}$  of up to 13 V can be controlled; for  $V_{CC} - V_{EE}$  level differences above 13V a  $V_{CC} - GND$  of at least 4.5V is required).

These multiplexer circuits dissipate extremely low quiescent power over the full  $V_{CC} - GND$  and  $V_{CC} - V_{EE}$  supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the ENABLE input terminal all channels are off.

The SL4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an enable input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1  $\mu A$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
  - 2.5 V min @ 15.0 V supply

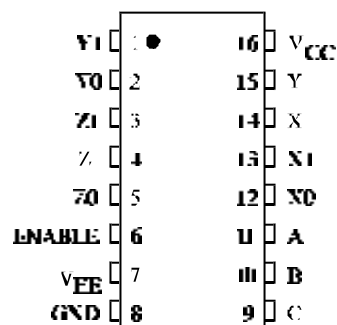


**N SUFFIX PLASTIC**

**D SUFFIX SOIC**

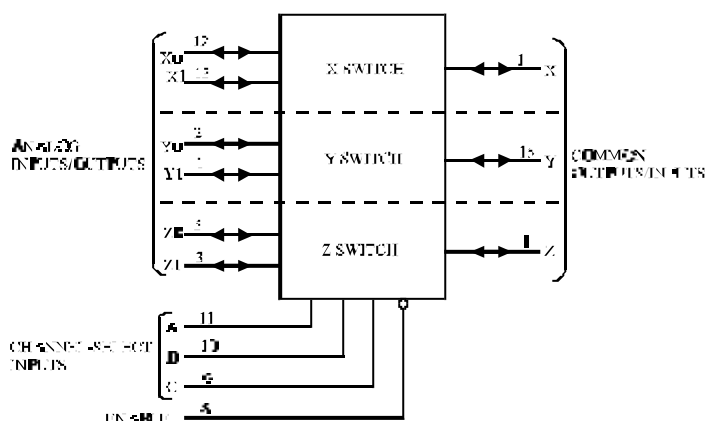
**ORDERING INFORMATION**  
 SL4053BN Plastic  
 SL4053BD SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

### PIN ASSIGNMENT



### LOGIC DIAGRAM

Triple Single-Pole, Double-Position  
Plus Common Off



PIN 16 =  $V_{CC}$   
 PIN 7 =  $V_{EE}$   
 PIN 8 = GND

### FUNCTION TABLE

Enable	Control Inputs			ON Channels		
	C	B	A	Z0	Y0	X0
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	None		

X = don't care

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P <sub>D</sub>	Power Dissipation per Output Transistor	100	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0	18	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
I	Multiplexer Switch Input Current Capability*	-	25	mA
R <sub>OH</sub>	Output Load Resistance	100	-	Ω

\* In certain applications, the external load-resistor current may include both V<sub>CC</sub> and signal-line components.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused digital pins must be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused Analog I/O pins may be left open or terminated.

**DC ELECTRICAL CHARACTERISTICS** Digital Section

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				≥ -55 °C	≤ 25 °C	≤ 125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	V <sub>IS</sub> =V <sub>CC</sub> thru 1kΩ V <sub>EE</sub> =GND I <sub>IS</sub> <2μA on all OFF Channels R <sub>L</sub> =1kΩ to GND	5	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V <sub>IL</sub>	Maximum Low -Level Input Voltage, Channel-Select or Enable Inputs	V <sub>IS</sub> =V <sub>CC</sub> thru 1kΩ V <sub>EE</sub> =GND I <sub>IS</sub> <2μA on all OFF Channels R <sub>L</sub> =1kΩ to GND	5	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
I <sub>IN</sub>	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V <sub>IN</sub> =V <sub>CC</sub> or GND	18	±0.1	±0.1	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	Channel Select = V <sub>CC</sub> or GND	5	5	5	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	

**DC ELECTRICAL CHARACTERISTICS** Analog Section

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				≥ -55 °C	≤ 25 °C	≤ 125 °C	
R <sub>ON</sub>	Maximum “ON” Resistance	V <sub>EE</sub> =GND=0 V <sub>IS</sub> = GND to V <sub>CC</sub>	5	800	1050	1300	Ω
			10	310	400	550	
			15	200	240	320	
ΔR <sub>ON</sub>	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V <sub>EE</sub> =GND=0	5	-	10	-	Ω
			10	-	15	-	
			15	-	5	-	
I <sub>OFF</sub>	Maximum Off- Channel Leakage Current, Any One Channel	V <sub>EE</sub> =GND=0	18	±100	±100	±1000	nA
	Maximum Off- Channel Leakage Current, Common Channel	V <sub>EE</sub> =GND=0	18	±100	±100	±1000	



## AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , Input $t_r=t_f=20.0\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			≥ -55 °C	≤ 25 °C	≤ 125 °C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay , Analog Input to Analog Output (Figure 1) R <sub>L</sub> =200kΩ	5	60	60	120	ns
		10	30	30	60	
		15	20	20	40	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay , Address to Analog Output (Figure 2) R <sub>L</sub> =10kΩ V <sub>EE</sub> =GND=0	5	720	720	1440	ns
		10	320	320	640	
		15	240	240	480	
	V <sub>EE</sub> =-5V	5	450	450	900	
t <sub>PLZ</sub> , t <sub>PZL</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 2) R <sub>L</sub> =10kΩ V <sub>EE</sub> =GND=0	5	720	720	1440	ns
		10	320	320	640	
		15	240	240	480	
	V <sub>EE</sub> =-10V	5	400	400	800	
t <sub>PHZ</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 2) R <sub>L</sub> =10kΩ V <sub>EE</sub> =GND=0	5	450	450	900	ns
		10	210	210	420	
		15	160	160	320	
	V <sub>EE</sub> =-10V	5	300	300	600	
C <sub>IN</sub>	Maximum Input Capacitance, Channel-Select or Enable Inputs	-	7.5	7.5	7.5	pF
C <sub>I/O</sub>	Maximum Capacitance V <sub>EE</sub> =GND=-5V C <sub>IS</sub> C <sub>OS</sub> Feedthrough C <sub>IOS</sub>	5	-	5	-	pF
		5	-	9	-	
		5	-	0.2	-	

## ADDITIONAL APPLICATION CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	V <sub>IS</sub> V	Limit*	Unit
					25 °C	
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (-3db)	V <sub>EE</sub> =GND R <sub>L</sub> =1kΩ 20 log(V <sub>OS</sub> /V <sub>IS</sub> )=-3db  V <sub>OS</sub> at Common OUT/IN	10	5*	30	MHz
		V <sub>OS</sub> at Any Channel	10	5*	60	
	(-40db) Feedthrough Frequency (All Channels OFF)	V <sub>EE</sub> =GND R <sub>L</sub> =1kΩ 20 log(V <sub>OS</sub> /V <sub>IS</sub> )=-40db V <sub>OS</sub> at Common OUT/IN	10	5*	8	
		V <sub>OS</sub> at Any Channel	10	5*	8	
	(-40db) Signal Crosstalk Frequency	V <sub>EE</sub> =GND R <sub>L</sub> =1kΩ 20 log(V <sub>OS</sub> /V <sub>IS</sub> )=-40db Between any 2 Sections : In Pin 2, Out Pin 14 In Pin 15, Out Pin 14			2.5 6	
THD	Total Harmonic Distortion	V <sub>EE</sub> =GND f <sub>IS</sub> =1kHz sine wave	5	2*	0.3	%
			10	3*	0.2	
			15	5*	0.12	
-	Address-or Enable to Signal Crosstalk	V <sub>EE</sub> =GND R <sub>L</sub> =10kΩ** t <sub>r</sub> ,t <sub>f</sub> =20ns Square Wave	10	-	65	mv (peak)

\* Peak-to-peak voltage symmetrical about (V<sub>DD</sub>-V<sub>EE</sub>)/2

\*\*Both ends of channel



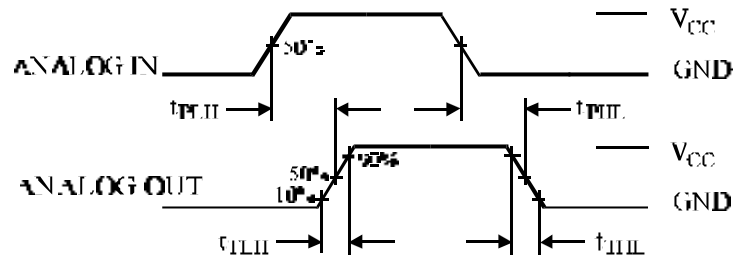


Figure 1. Switching Waveforms

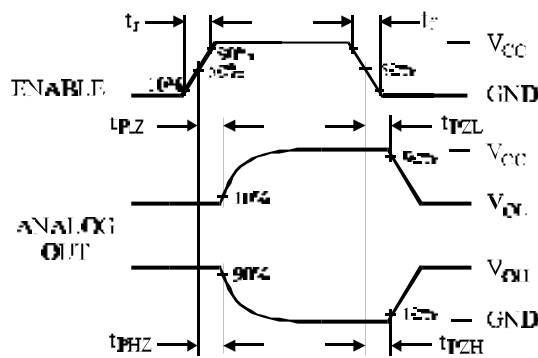


Figure 2. Switching Waveforms

## EXPANDED LOGIC DIAGRAM

