

Counter/Divider

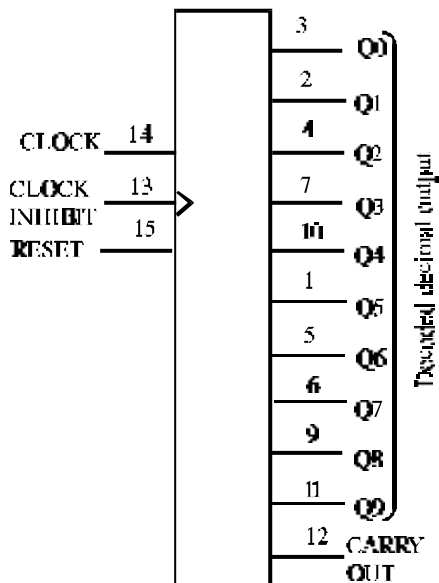
High-Voltage Silicon-Gate CMOS

The SL4017B is 5-stage Johnson counter having 10 decoded outputs. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high-speed operation, 2-input decode-gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the SL4017B.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

H SUFFIX PLASTIC

D SUFFIX SOIC

ORDERING INFORMATION
SL4017BN Plastic
SL4017BD SOIC
T_A = -55° to 125° C for all packages

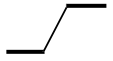


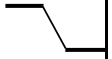
PIN ASSIGNMENT

Q5	1	16	V _{CC}
Q1	2	15	RESET
Q3	3	14	CLOCK
Q2	4	13	CLOCK INHIBIT
Q6	5	12	CARRY OUT
Q7	6	11	Q9
Q8	7	10	Q4
GND	8	9	Q5

- Noise margin (over full package temperature range):
1.0 V min @ 5.0 V supply
2.0 V min @ 10.0 V supply
2.5 V min @ 15.0 V supply



FUNCTION TABLE

Clock	Clock Enable	Reset	Output State *
L	X	L	no change
X	H	L	no change
X	X	H	reset counter Q0=H, Q1- Q9=L, C0=H
	L	L	Advance to next state
	X	L	no change
X		L	no change
H		L	Advance to next state

* Carry Out=H for Q0,Q1,Q2,Q3 or Q4=H
Carry Out = L otherwise, X=don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P _D	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.



SL4017B

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5V or V _{CC} - 0.5V V _{OUT} =1.0V or V _{CC} - 1.0V V _{OUT} =1.5V or V _{CC} - 1.5V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.5V or V _{CC} - 0.5V V _{OUT} =1.0V or V _{CC} - 1.0V V _{OUT} =1.5V or V _{CC} - 1.5V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	µA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	5	5	150	µA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2.0	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	



AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
f_{\max}	Maximum Clock Frequency	5.0	2.5	2.5	1.25	MHz
		10	5	5	2.5	
		15	5.5	5.5	2.75	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Decode Output (Figure 1)	5.0	650	650	1300	ns
		10	270	270	540	
		15	170	170	340	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Carry Output (Figure 1)	5.0	600	600	1200	ns
		10	250	250	500	
		15	160	160	320	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Carry Output or Decode Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Reset to Carry Output or Decode Output (Figure 1)	5.0	530	530	1060	ns
		10	230	230	460	
		15	170	170	340	
C_{IN}	Maximum Input Capacitance	-		5		pF

TIMING REQUIREMENTS ($V_{CC}=5.0\text{V}\pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=20\text{ ns}$, $R_L=200\text{k}\Omega$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0	200	200	400	ns
		10	90	90	180	
		15	60	60	120	
t_r , t_f	Maximum Input Rise and Fall Times, Clock (Figure 1)	5.0	UNLIMITED			μs
		10				
		15				
t_w	Minimum Pulse Width, Reset (Figure 1)	5.0	260	260	520	ns
		10	110	110	220	
		15	60	60	120	
t_{rem}	Minimum Removal Time, Reset (Figure 1)	5.0	400	400	800	ns
		10	280	280	560	
		15	150	150	300	



SL4017B

t _{SU}	Minimum Setup Time, Clock Inhibit to Clock (Figure 1)	5.0	230	230	460	ns
		10	100	100	200	
		15	70	70	140	

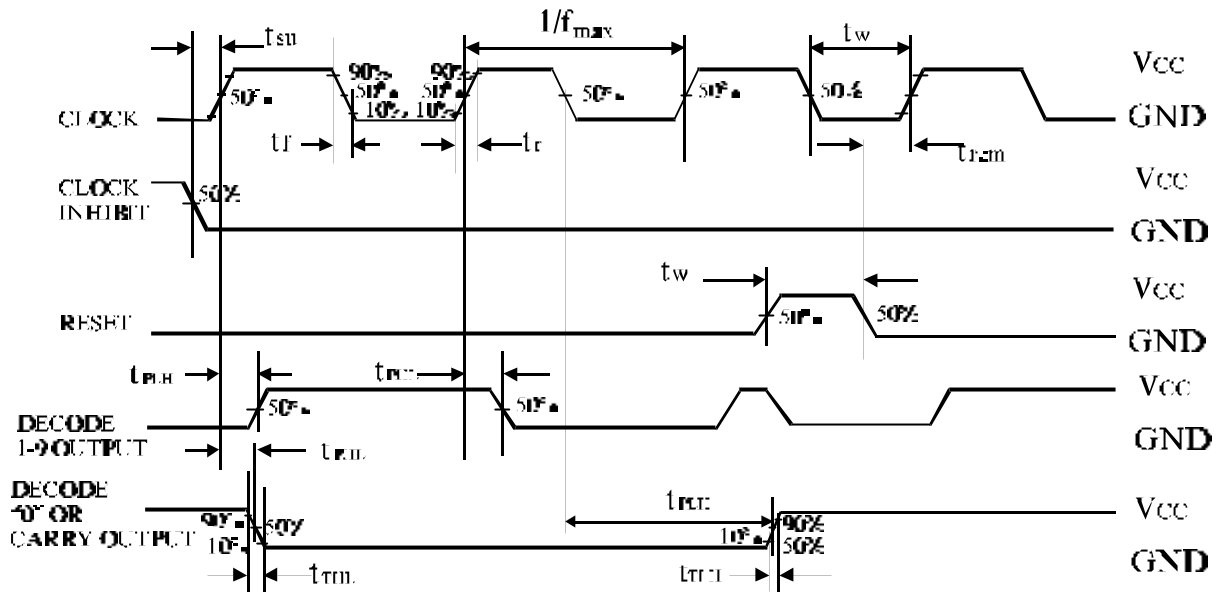
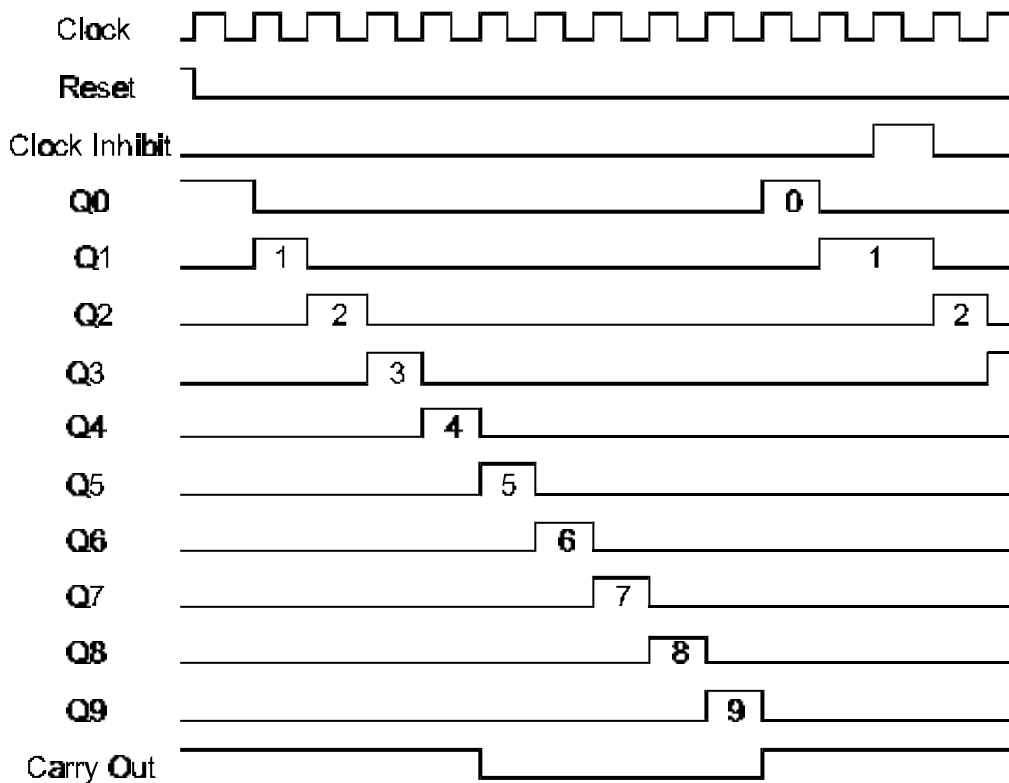


Figure 1. Switching Waveforms

Timing diagram



EXPANDED LOGIC DIAGRAM

