Description

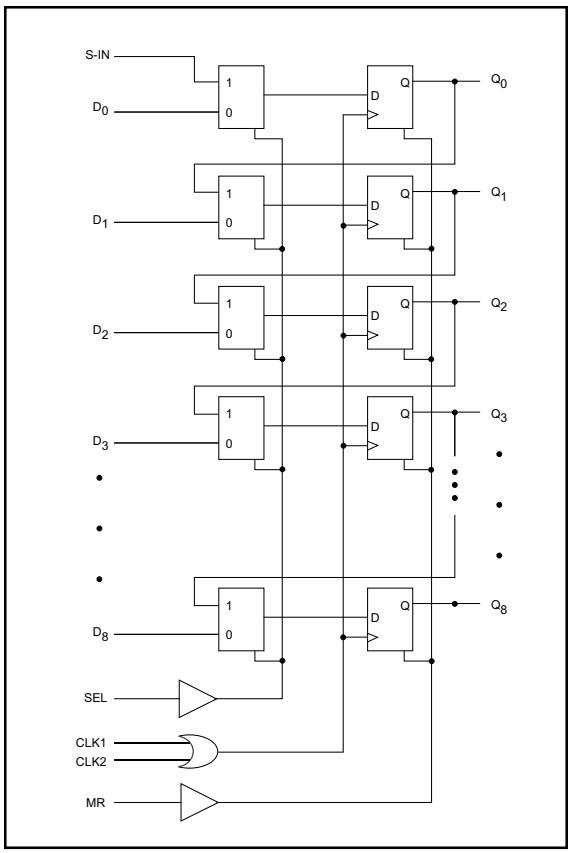
The SK10E/100E142 is a 9-bit shift register, designed with byte-parity applications in mind. The E142 performs serial/parallel in and serial/parallel out, shifting in one direction. The nine inputs D0 – D8 accept parallel input data, while S-IN accepts serial input data. The Qn outputs do not need to be terminated for the shift operation to function. To minimize noise and power, any Q output not used should be left unterminated.

The SEL (Select) input pin is used to switch between the two modes of operation – SHIFT and LOAD. The shift direction is from bit 0 to bit 8. Input data is accepted by the registers at set-up time before the posiitive going edge of CLK1 or CLK2. Shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

Features

- 700 MHz Minimum Shift Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of –4.2 to –5.5V
- 75KΩ Internal Input Pulldown Resistors
- Fully Compatible with MC10/100E142
- Specified over Industrial Temperature Range: –40°C to 85°C
- ESD Protection of >4000V
- Available in 28 Lead PLCC Package

Functional Block Diagram

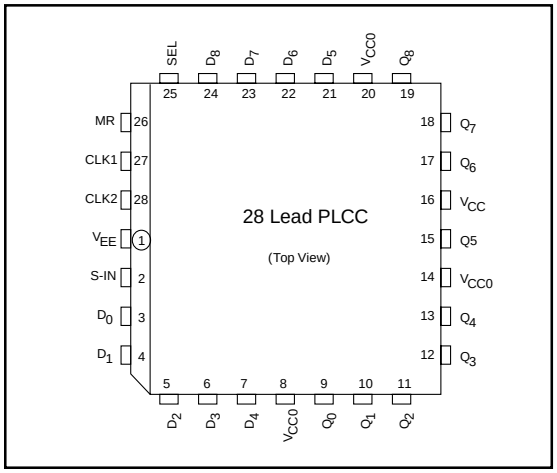


PIN Description

Pin Names

Pin	Function
D0 - D8	Parallel Data Inputs
S-IN	Serial Data Input
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0 - Q8	Data Outputs

Pinout

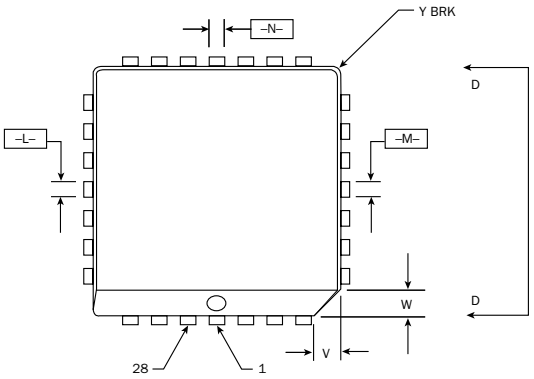


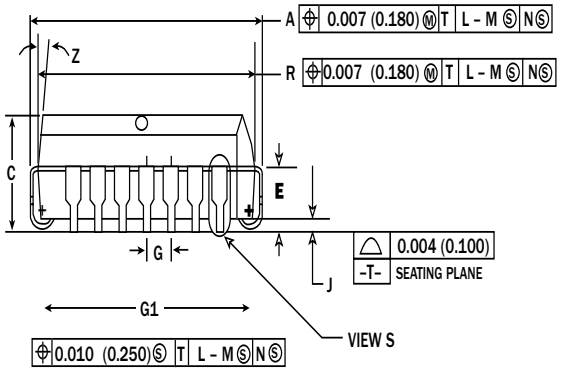
Functions

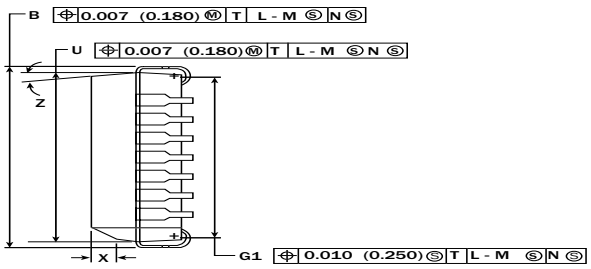
SEL	Mode
L	Load
H	Shift

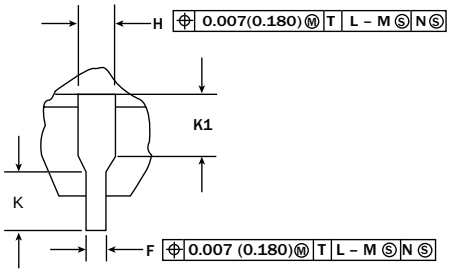
HIGH-PERFORMANCE PRODUCTS

Package Information









View S

NOTES:

1. Datums -L-, -M-, and -N- determined where top of lead shoulder exits plastic body at mold parting line.
2. DIM G1, true position to be measured at Datum -T-, Seating Plane.
3. DIM R and U do not include mold flash. Allowable mold flash is 0.010 (0.250) per side.
4. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
5. Controlling Dimension: Inch.
6. The package top may be smaller than the package bottom by up to 0.012 (0.300). Dimensions R and U are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
7. Dimension H does not include Dambar protrusion or intrusion. The Dambar protrusion(s) shall not cause the H dimension to be greater than 0.037 (0.940). The Dambar intrusion(s) shall not cause the H dimension to be smaller than 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	–	0.51	–
K	0.025	–	0.64	–
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	–	0.020	–	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	–	1.02	–

DC Characteristics

SK10/100E142 DC Electrical Characteristics *(Notes 1, 2, 4)*

V_{CC} – V_{EE} = 4.2V to 5.5V; V_{OUT} Loaded 50Ω to VCC – 2.0V)

Symbol	Characteristic	TA = –40°C		TA = 0°C		TA = +25°C		TA = +85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{IH}	Input HIGH Current		150		150		150		150	µA
I_{EE}	Power Supply Current 10E 100E	 67 69	 108 112	 70 74	 112 120	 71 78	 114 125	 74 86	 119 138	 mA mA

AC Characteristics

SK10/100E142 AC Electrical Characteristics

V_{CC} – V_{EE} = 4.2V to 5.5V; V_{OUT} Loaded 50Ω to VCC – 2.0V)

		TA = –40°C			TA = 0°C			TA = +25°C			TA = +85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		700	900		MHz
 t_{PLH} t_{PHL}	Propagation Delay to Output CLK MR	 788 831	 	 1053 989	 795 836	 	 1043 994	 800 840	 	 1037 987	 813 851	 	 1023 976	 ps ps
t_S	Setup Time D SEL	 50 300	 	 	 50 300	 	 	 50 300	 	 	 50 300	 	 	ps
t_H	Hold Time D SEL	 300 75	 	 	 300 75	 	 	 300 75	 	 	 300 75	 	 	ps
t_{RR}	Reset Recovery Time	900			900			900			900			ps
t_{PW}	Minimum Pulse Width CLK, MR	 400	 	 	 400	 	 	 400	 	 	 400	 	 	 ps
t_{SKEW}	Within Device Skew[3]		50			50			50			50		ps
t_r t_f	Rise/Fall Times (20% - 80%)	255		574	266		566	270		525	282		428	ps

AC Characteristics *(continued)*

Notes:

1. 10E circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to VCC–2.0V.
2. 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
3. Within device skew is defined as identical transitions on similar paths through a device.
4. For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
5. For part ordering description, see HPP Part Ordering Information Data Sheet.

Ordering Information

Ordering Code	Package ID	Temperature Range
SK10E142PJ	28-PLCC	Industrial
SK10E142PJT	28-PLCC	Industrial
SK100E142PJ	28-PLCC	Industrial
SK100E142PJT	28-PLCC	Industrial

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