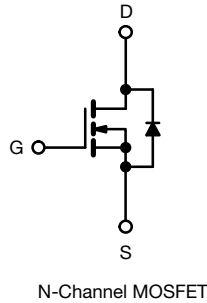# D Series Power MOSFET

TO-220 FULLPAK

N-Channel MOSFET

FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance (C_{iss})
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): R_{on} x Q_g
  - Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

RoHS*
Available

APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- Battery chargers

PRODUCT SUMMARY

V_{DS} (V) at T_J max.		450
$R_{DS(on)}$ max. (Ω) at 25 °C	V_{GS} = 10 V	1.0
Q_g max. (nC)		18
Q_{gs} (nC)		3
Q_{gd} (nC)		4
Configuration		Single

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF6N40D-E3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER				SYMBOL	LIMIT	UNIT
Drain-Source Voltage				V_{DS}	400	V
Gate-Source Voltage				V_{GS}	± 30	
Gate-Source Voltage AC (f > 1 Hz)					30	
Continuous Drain Current (T_J = 150 °C) [e]	V_{GS} at 10 V	T_C = 25 °C		I_D	6	A
		T_C = 100 °C			4	
Pulsed Drain Current [a]				I_{DM}	13	
Linear Derating Factor					0.24	W/°C
Single Pulse Avalanche Energy [b]				E_{AS}	104	mJ
Maximum Power Dissipation				P_D	30	W
Operating Junction and Storage Temperature Range				T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T_J = 125 °C			dV/dt	24	V/ns
Reverse Diode dV/dt [d]					0.48	
Soldering Recommendations (Peak temperature) [c]	For 10 s				300	°C
Mounting Torque	M3 screw				0.6	Nm

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.3 mH, R_g = 25 Ω, I_{AS} = 9.5 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, starting T_J = 25 °C.
e. Limited by maximum junction temperature.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	4.1	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ µA		400	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 250$ µA		-	0.53	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ µA		3	-	5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30$ V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 400$ V, $V_{GS} = 0$ V		-	-	1	µA
		$V_{DS} = 320$ V, $V_{GS} = 0$ V, $T_J = 125$ °C		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 3$ A	-	0.85	1.0	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50$ V, $I_D = 3$ A		-	1.7	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 100$ V, f = 1 MHz		-	311	-	pF
Output Capacitance	C_{oss}			-	38	-	
Reverse Transfer Capacitance	C_{rss}			-	7	-	
Effective output capacitance, energy related [a]	$C_{o(er)}$	$V_{GS} = 0$ V, $V_{DS} = 0$ V to 320 V		-	44	-	
Effective output capacitance, time related [b]	$C_{o(tr)}$			-	54	-	
Total Gate Charge	Q_g	$V_{GS} = 10$ V	$I_D = 3$ A, $V_{DS} = 320$ V	-	9	18	nC
Gate-Source Charge	Q_{gs}			-	3	-	
Gate-Drain Charge	Q_{gd}			-	4	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400$ V, $I_D = 3$ A, $V_{GS} = 10$ V, $R_g = 9.1$ Ω		-	12	24	ns
Rise Time	t_r			-	11	22	
Turn-Off Delay Time	$t_{d(off)}$			-	14	28	
Fall Time	t_f			-	8	16	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	1.9	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6	A
Pulsed Diode Forward Current	I_{SM}			-	-	24	
Diode Forward Voltage	V_{SD}	$T_J = 25$ °C, $I_S = 3$ A, $V_{GS} = 0$ V		-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25$ °C, $I_F = I_S = 3$ A, dI/dt = 100 A/µs, $V_R = 20$ V		-	236	-	ns
Reverse Recovery Charge	Q_{rr}			-	1.1	-	µC
Reverse Recovery Current	I_{RRM}			-	9	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)
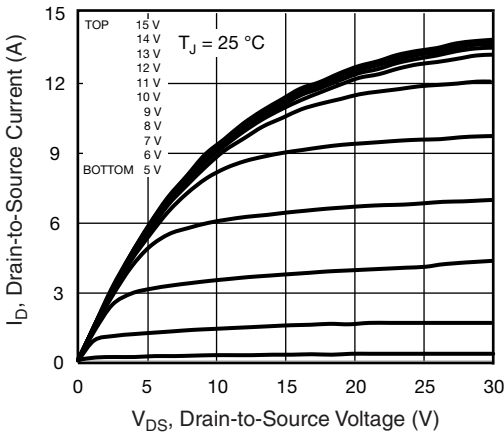
Fig. 1 - Typical Output Characteristics

Fig. 2 - Typical Output Characteristics

Fig. 3 - Typical Transfer Characteristics
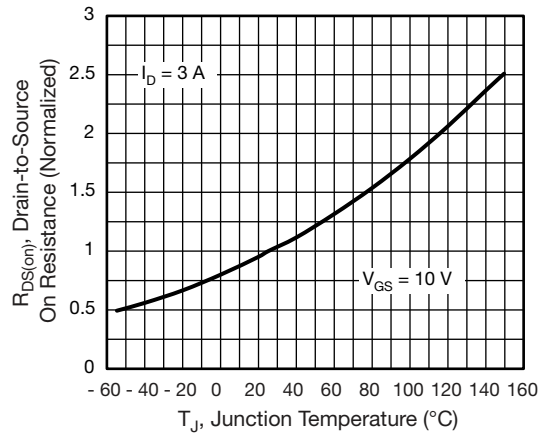
Fig. 4 - Normalized On-Resistance vs. Temperature
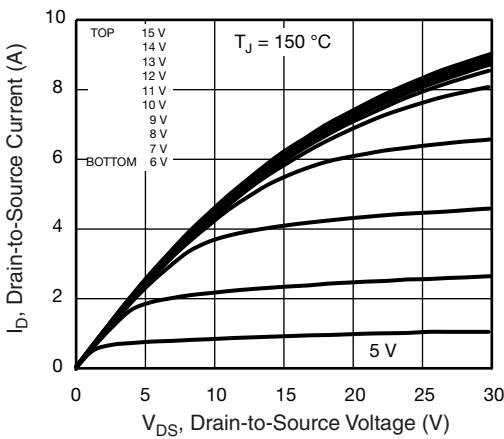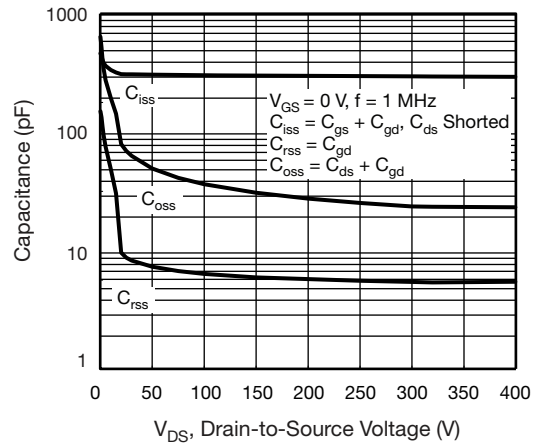
Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage
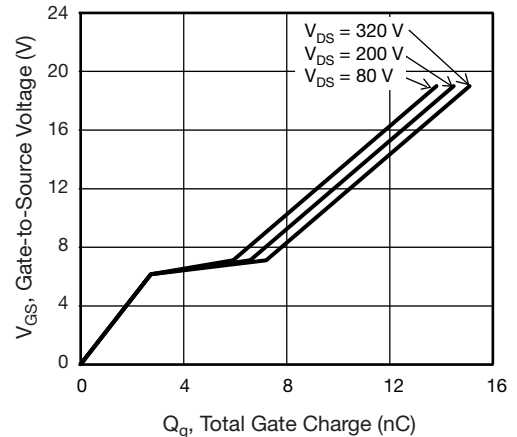
Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage
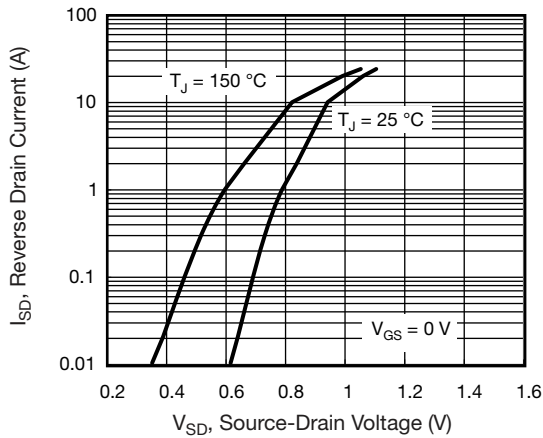
Fig. 7 - Typical Source-Drain Diode Forward Voltage
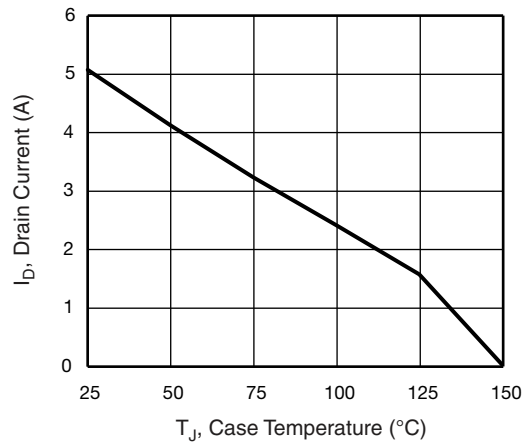
Fig. 9 - Maximum Drain Current vs. Case Temperature
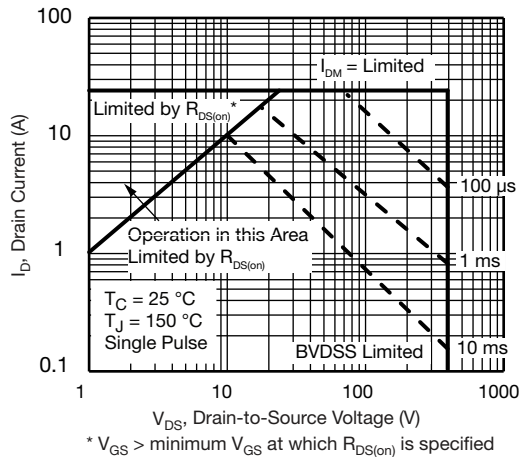
Fig. 8 - Maximum Safe Operating Area
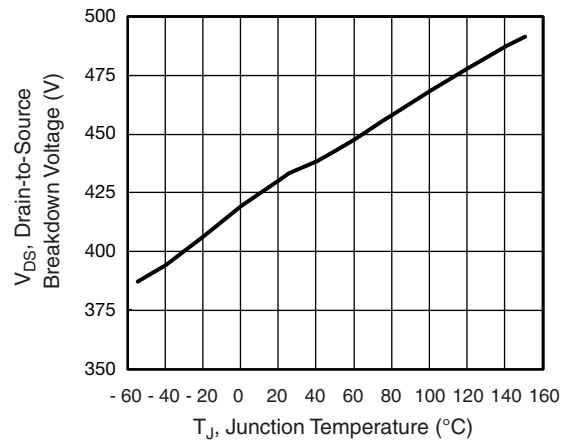
Fig. 10 - Temperature vs. Drain-to-Source Voltage
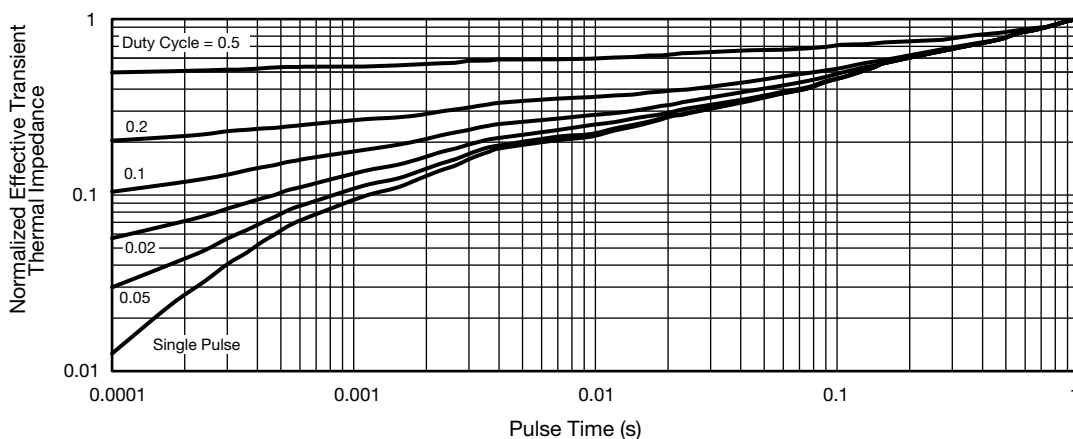
Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

For technical questions, contact: hvm@vishay.com

Fig. 12 - Switching Time Test Circuit

Fig. 16 - Basic Gate Charge Waveform

Fig. 13 - Switching Time Waveforms

Fig. 17 - Gate Charge Test Circuit
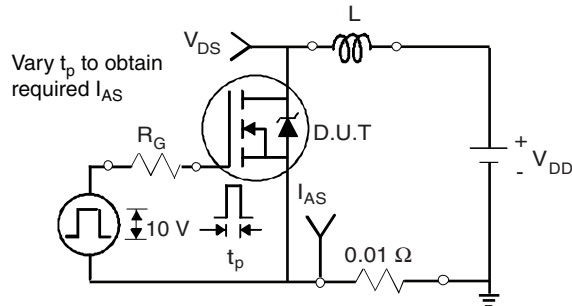
Fig. 14 - Unclamped Inductive Test Circuit
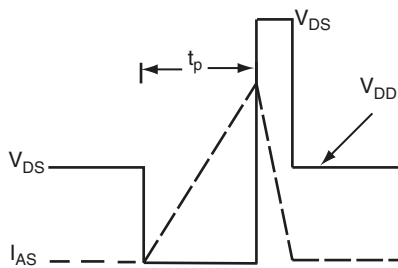
Fig. 15 - Unclamped Inductive Waveforms

Peak Diode Recovery dV/dt Test Circuit

Circuit layout considerations
- Low stray inductance
- Ground plane
- Low leakage inductance current transformer

D.U.T.

- dV/dt controlled by R_g
- Driver same type as D.U.T.
- I_{SD} controlled by duty factor "D"
- D.U.T. - device under test

V_{DD}

① Driver gate drive

$$D = \frac{P.W.}{Period}$$

$V_{GS} = 10\ V^a$

② D.U.T. I_{SD} waveform

Reverse recovery current

Body diode forward current

dI/dt

③ D.U.T. V_{DS} waveform

Diode recovery dV/dt

V_{DD}

Re-applied voltage

Body diode forward drop

④ Inductor current

Ripple ≤ 5 %

I_{SD}

Note

a. $V_{GS} = 5\ V$ for logic level devices

Fig. 18 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9

DIM.	MILLIMETERS		
	MIN.	**NOM.**	**MAX.**
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

OPTION 2: FACILITY CODE = Y
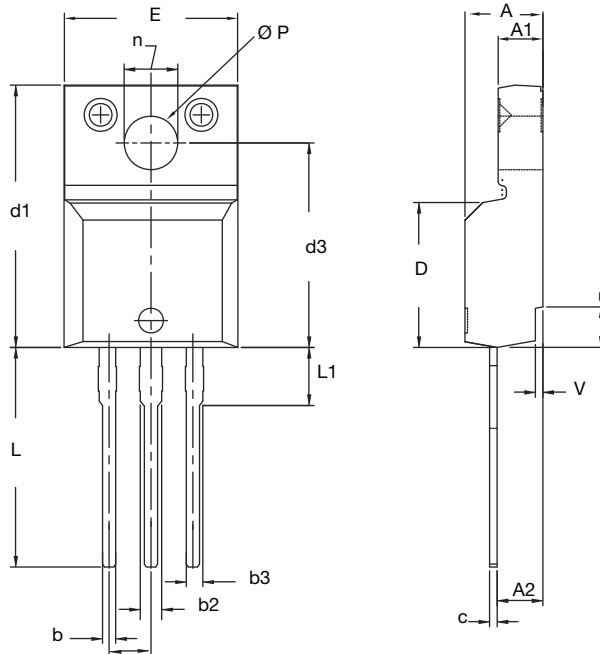
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020
ECN: E19-0180-Rev. D, 08-Apr-2019 DWG: 5972				

Notes

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2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

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