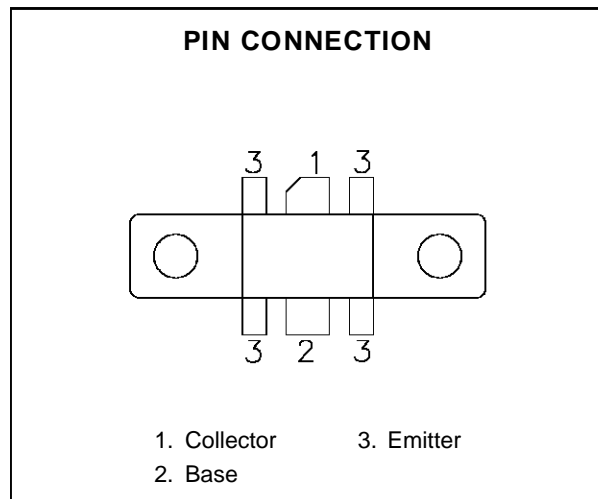
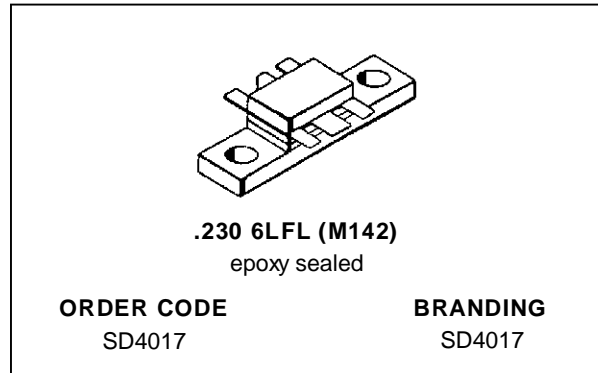


RF & MICROWAVE TRANSISTORS 806-960 MHz CELLULAR BASE STATIONS

- GOLD METALLIZATION
- DIFFUSED EMITTER BALLASTING
- INTERNAL INPUT MATCHING
- DESIGNED FOR LINEAR OPERATION
- HIGH SATURATED POWER CAPABILITY
- COMMON EMITTER CONFIGURATION
- $P_{OUT} = 30$ W MIN. WITH 7.5 dB GAIN
- $\eta_C = 55\%$ TYPICAL
- TYPICAL LOAD MISMATCH CAPABILITY:
20:1 ALL ANGLES RATED CONDITIONS
10:1 ALL ANGLES @ $\pm 20\%$ RATED VOLTAGE
- TYPICAL OVERDRIVE SURVIVABILITY
5 dB


DESCRIPTION

The SD4017 is a gold metallized epitaxial silicon NPN planar transistor using diffused emitter ballast resistors for high linearity class AB operation for cellular base station applications.

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	48	V
V_{CEO}	Collector-Emitter Voltage	25	V
V_{EBO}	Collector-Supply Voltage	3.5	V
P_{DISS}	Power Dissipation	88	W
I_C	Device Current	7.5	A
T_J	Junction Temperature	200	$^{\circ}C$
T_{STG}	Storage Temperature	- 65 to +150	$^{\circ}C$

THERMAL DATA

$R_{TH(j-c)}$	Junction-Case Thermal Resistance	2.0	$^{\circ}C/W$
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SD4017**ELECTRICAL SPECIFICATIONS** ($T_{\text{case}} = 25^{\circ}\text{C}$)

STATIC

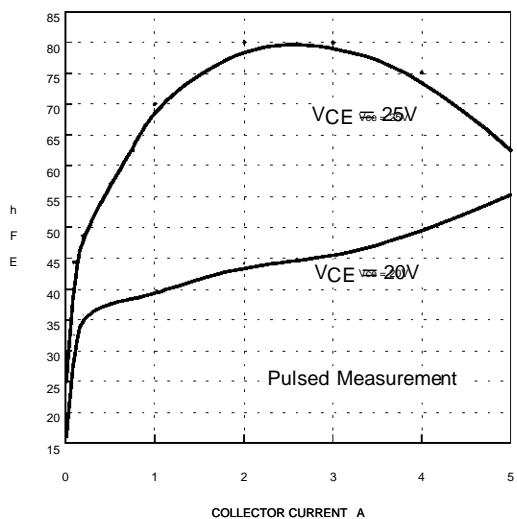
Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
BV_{CBO}	$I_{\text{C}} = 100 \text{ mA}$	48	55	—	V
BV_{EBO}	$I_{\text{E}} = 10 \text{ mA}$	3.5	5	—	V
BV_{CEO}	$I_{\text{C}} = 40 \text{ mA}$	25	28	—	V
BV_{CER}	$I_{\text{C}} = 40 \text{ mA}$ $R_{\text{BE}} = 150 \ \Omega$	30	40	—	V
I_{CBO}	$V_{\text{CE}} = 24 \text{ V}$	10	—	—	mA
h_{FE}	$V_{\text{CE}} = 20 \text{ V}$ $I_{\text{C}} = 2 \text{ A}$	15	40	100	—

DYNAMIC

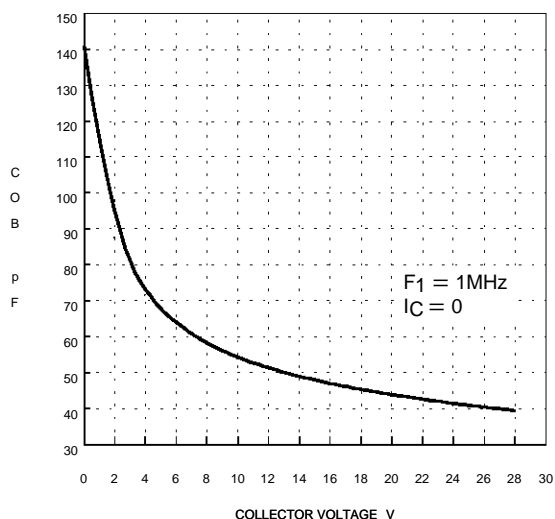
Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
P_{OUT}	$f = 860 \text{ MHz}$ $V_{\text{CE}} = 25 \text{ V}$ $I_{\text{CQ}} = 60 \text{ mA}$	30	—	—	W
η_{c}	$f = 860 \text{ MHz}$ $V_{\text{CE}} = 25 \text{ V}$ $I_{\text{CQ}} = 60 \text{ mA}$	—	55	—	%
P_{G}	$f = 860 \text{ MHz}$ $V_{\text{CE}} = 25 \text{ V}$ $I_{\text{CQ}} = 60 \text{ mA}$	7.5	9	—	dB
C_{OB}	$V_{\text{CB}} = 25 \text{ V}$ $f_{\text{o}} = 1 \text{ MHz}$	—	42	—	pf
IMD_3	$P_{\text{OUT}} = 30 \text{ WPEP}$ $f_1 = 860.0 \text{ MHz}$ $f_2 = 860.1 \text{ MHz}$	—	-35	—	dBc
VSWR_1	$\text{VSWR} = 20:1$ $V_{\text{CE}} = 25 \text{ V}$ $\text{VSWR} = 10:1$ $V_{\text{CE}} = 25 \text{ V} \pm 20\%$	No Degradation in Output Device			Typ.
VSWR_2	$\text{VSWR} = 5:1$ $V_{\text{CE}} = 25 \text{ V} \pm 20\%$ $P_{\text{IN}} = P_{\text{IN}}(\text{norm}) + 3\text{dB}$	No Degradation in Output Device			Typ.
OVD	$P_{\text{IN}}(\text{norm}) = +5\text{dB}$ $V_{\text{CE}} = 25 \text{ V}$ $P_{\text{IN}}(\text{norm}) = +3\text{dB}$ $V_{\text{CE}} = 25 \text{ V} \pm 20\%$	No Degradation in Output Device			Typ.

TYPICAL PERFORMANCE

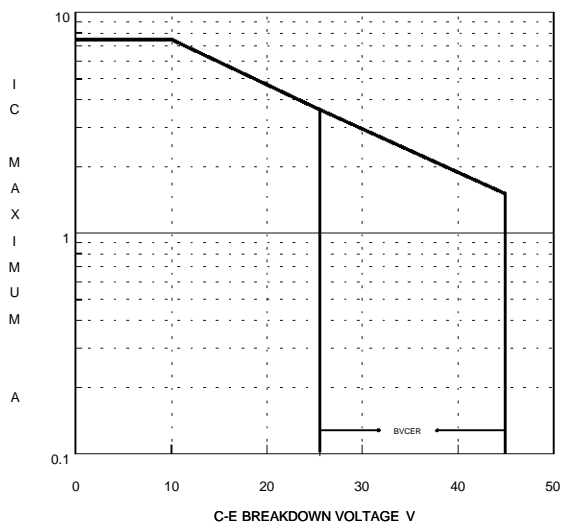
DC CURRENT GAIN vs COLLECTOR CURRENT



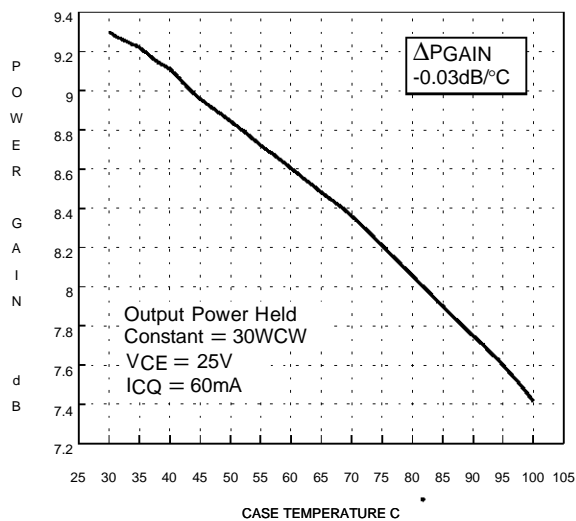
OUTPUT CAPACITANCE vs C-B VOLTAGE



DC SAFE OPERATING AREA

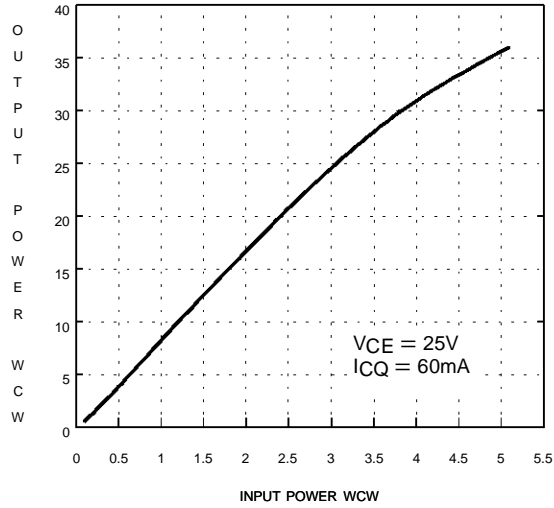


POWER GAIN vs CASE TEMPERATURE

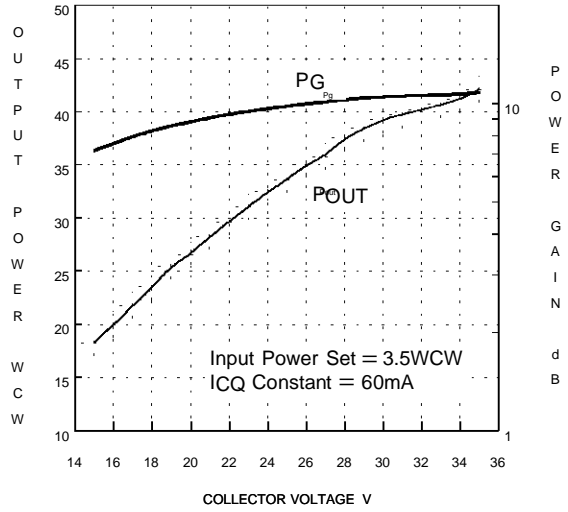


TYPICAL PERFORMANCE (cont'd)

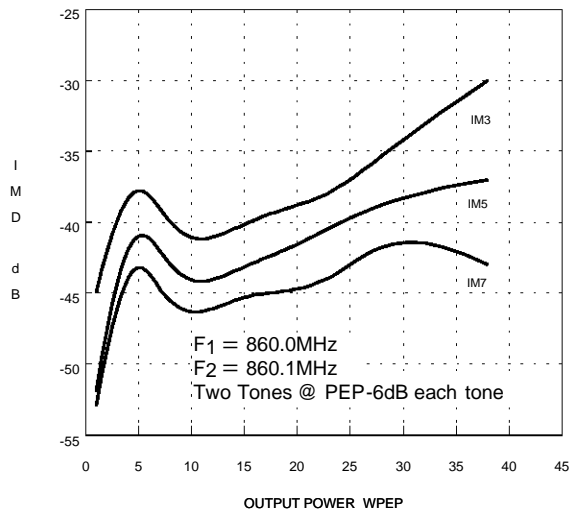
OUTPUT POWER vs INPUT POWER



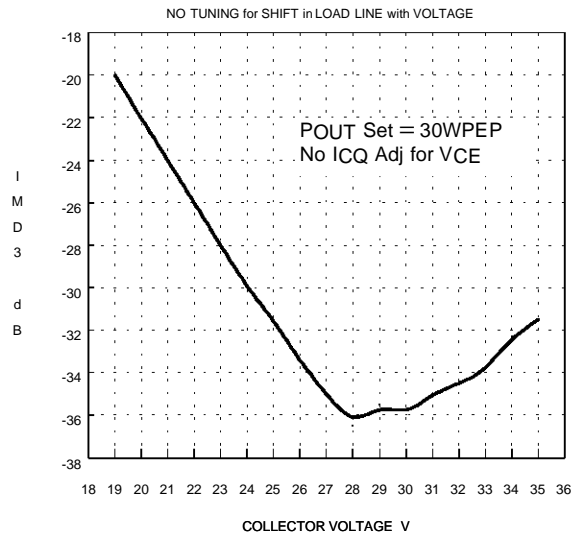
OUTPUT POWER & GAIN vs VOLTAGE



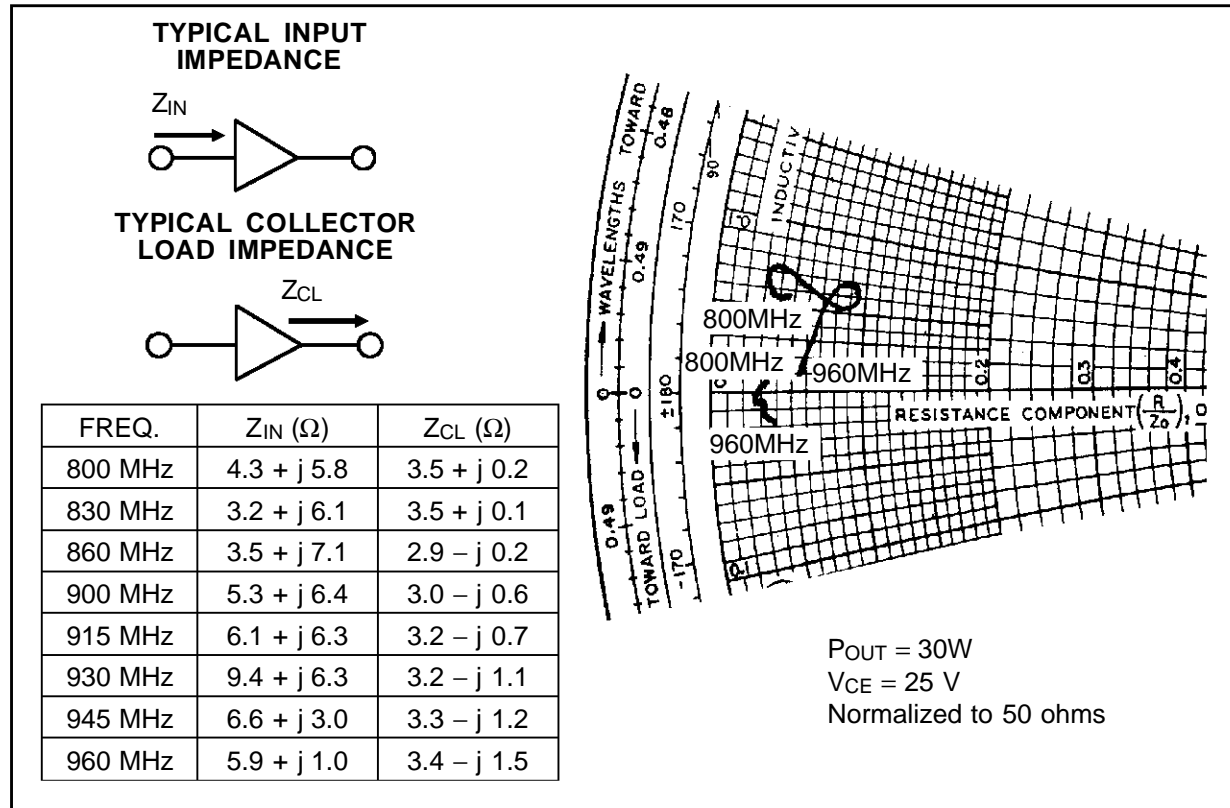
IM DISTORTION vs OUTPUT POWER



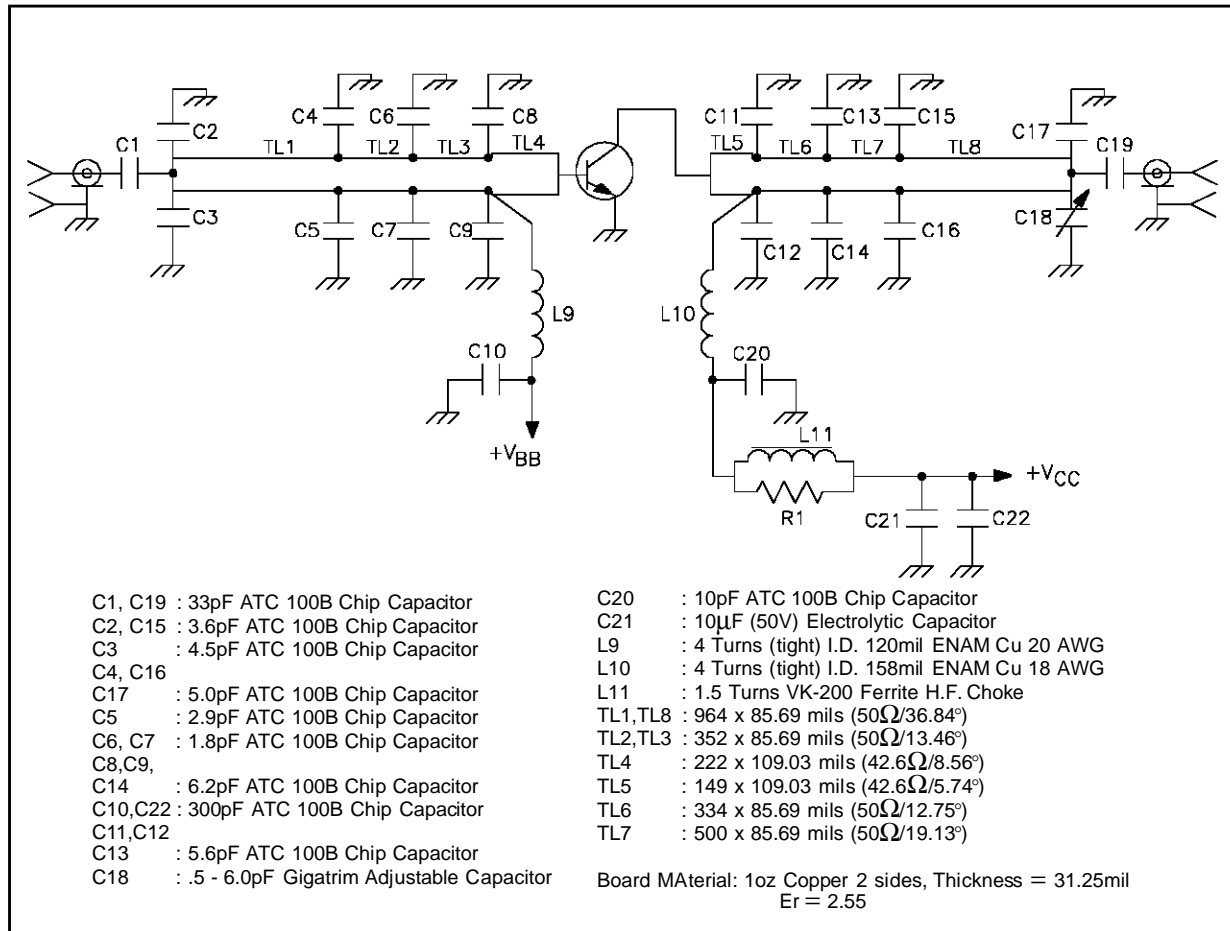
IM3 DISTORTION vs SUPPLY VOLTAGE



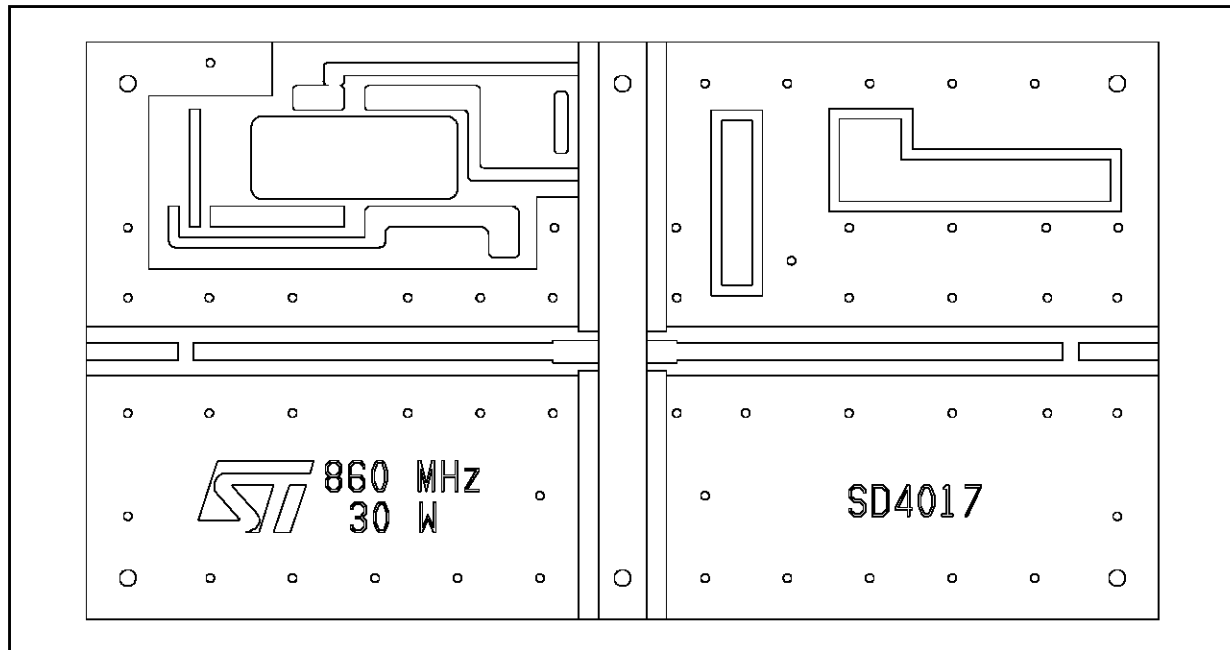
IMPEDANCE DATA



TEST CIRCUIT

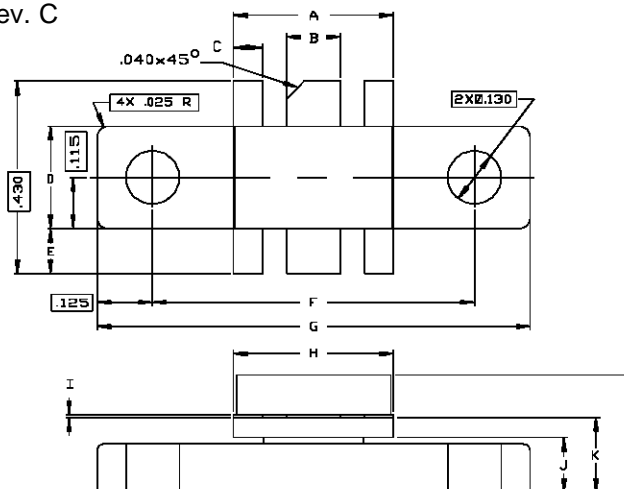


BOARD LAYOUT



PACKAGE MECHANICAL DATA

Ref. Dwg.No. 12-0142 rev. C



SGS-THOMSON MICROELECTRONICS			CONT'D		
	MINIMUM Inches/mm	MAXIMUM Inches/mm		MINIMUM Inches/mm	MAXIMUM Inches/mm
A	.355/9,02	.365/9,27	K	.160/4,06	.180/4,57
B	.115/2,92	.125/3,18	L	.230/5,84	.260/6,60
C	.075/1,91	.085/2,16			
D	.225/5,72	.235/5,97			
E	.090/2,29	.110/2,79			
F	.720/18,29	.730/18,54			
G	.970/24,64	.980/24,89			
H	.355/9,02	.365/9,27			
I	.004/0,10	.006/0,15			
J	.120/3,05	.130/3,30			

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