SEMTECH

SC4609

Low Input, MHz Operation, High Efficiency Synchronous Buck

POWER MANAGEMENT

Description

The SC4609 is a voltage mode step down (buck) regulator controller that provides accurate high efficiency power conversion from an input supply range of 2.7V to 5.5V. A high level of integration reduces external component count, and makes it suitable for low voltage applications where cost, size and efficiency are critical. The SC4609 is capable of producing an output voltage as low as 0.5V.

The SC4609 drives external, N-channel MOSFETs with a peak gate current of 1A. A non-overlap protection is provided for the gate drive signals to prevent shoot through of the MOSFET pair. The SC4609 features lossless current sensing of the voltage drop across the drain to source resistance of the high side MOSFET during its conduction period. Its switching frequency can be programmed up to 1MHz.

The quiescent supply current in sleep mode is typically lower than 10µA. A external soft start is provided to prevent output voltage overshoot during start-up.

The SC4609 is an ideal choice for converting 3.3V, 5V or other low input supply voltages. It's available in 12 pin MLP package.

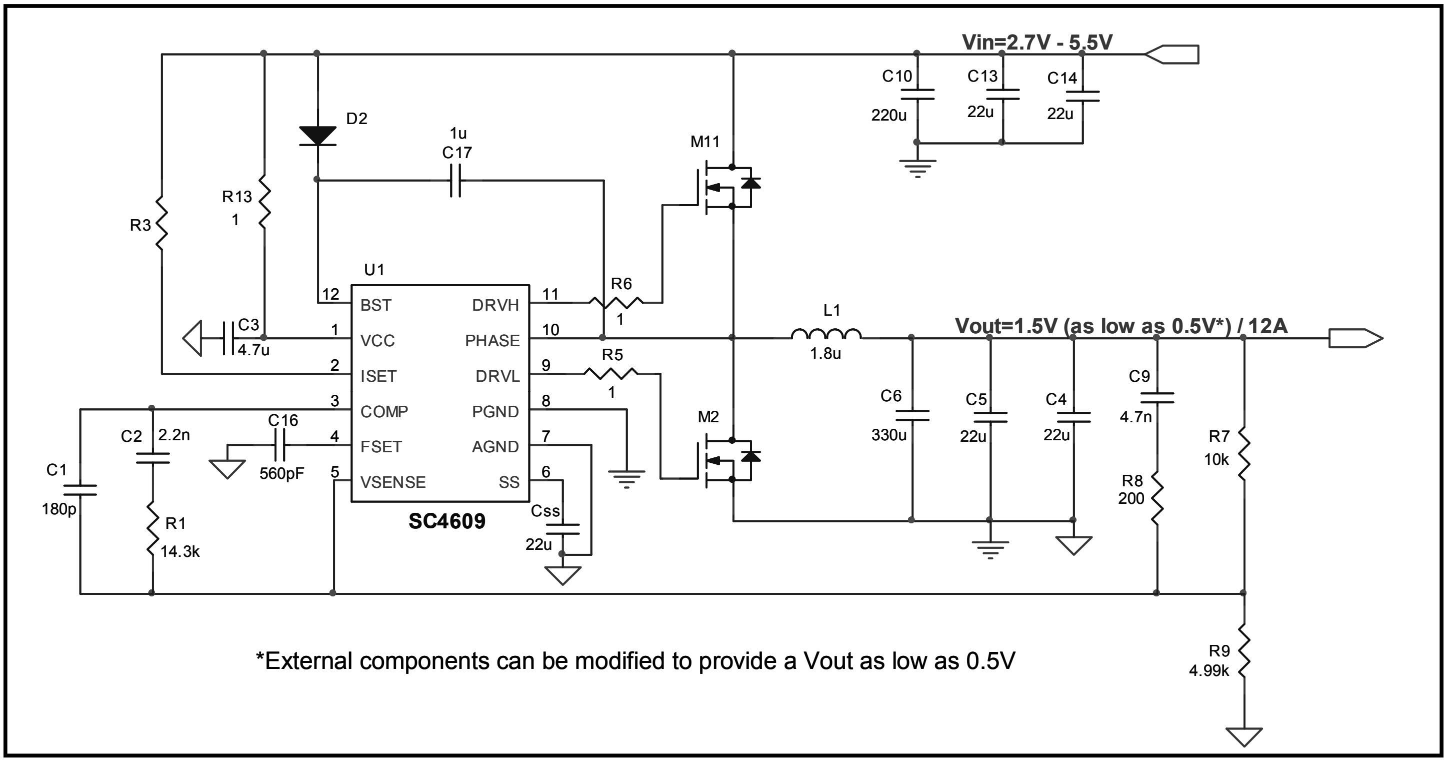
Features

- Asynchronous start up
- Programmable switching frequency up to 1MHz
- BiCMOS voltage mode PWM controller
- 2.7V to 5.5V input voltage range
- Output voltage as low as 0.5V
- +/-1% reference accuracy
- Sleep mode (Icc = 10µA typ)
- Adjustable lossless short circuit current limiting
- Combination pulse by pulse & hiccup mode current limit
- High efficiency synchronous switching
- 1A peak current driver
- External soft start
- 12-pin MLP Lead-free package, fully WEEE and RoHS compliant

Applications

- Distributed power architecture
- Servers/workstations
- Local microprocessor core power supplies
- DSP and I/O power supplies
- Battery-powered applications
- Telecommunications equipment
- Data processing applications

Typical Application Circuit



*External components can be modified to provide a Vout as low as 0.5V

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage (V_{CC})		6	V
PGND		±0.3	V
Output Drivers (DRVH, DRVL) Currents Continuous		±0.25	A
Peak		±1.00	A
Inputs (VSENSE, COMP, FSET, ISET, SS)		-0.3 to 6	V
BST		12	V
PHASE		-0.3 to 6	V
PHASE Pulse tpulse < 50ns		-2 to 7	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Maximum Junction Temperature	T_J	+150	°C
Peak IR Reflow Temperature, 10 - 40s	T_{PKG}	260	°C
ESD Rating (Human Body Model)	ESD	4	kV

All voltages with respect to AGND. Currents are positive into, negative out of the specified terminal.

Electrical Characteristics

Unless otherwise specified, VCC = 3.3V, CT = 270pF, T_A = -40°C to 85°C, $T_A = T_J$

Note: (1). Guaranteed by design.

Parameter	Test Conditions	Min	Typ	Max	Unit
Overall					
Supply Voltage				5.5	V
Supply Current, Sleep	FSET = 0V		10	15	µA
Supply Current, Operating	V_{CC} = 5.5V		2	3.75	mA
VCC Turn-on Threshold	T_A = -40°C to 85°C			2.7	V
VCC Turn-off Hysteresis			350		mV
Error Amplifier					
Input Voltage (Internal Reference)	T_A = 25°C	0.495	0.5	0.505	V
	V_{CC} = 2.7V - 5.5V, T_A = 25°C	0.4925	0.5	0.5075	
	T_A = -40°C to 85°C	0.4925		0.5075	
VSENSE Bias Current	V_{SENSE} = 0.5V		200		nA
Open Loop Gain (1)	V_{COMP} = 0.5 to 2.5V		90		dB
Unity Gain Bandwidth (1)			8		MHz

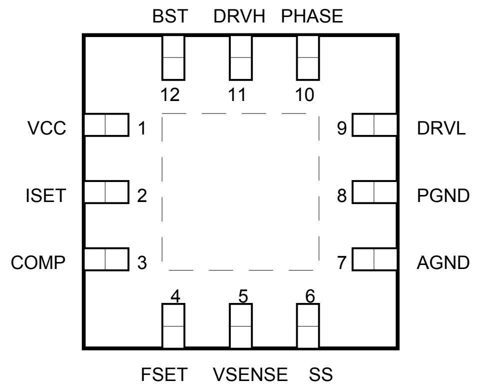
Electrical Characteristics (Cont.)

Unless otherwise specified, VCC = 3.3V, CT = 270pF, T_A = -40°C to 85°C, T_A=T_J

Parameter	Test Conditions	Min	Typ	Max	Unit
Error Amplifier (Cont.)					
Slew Rate (1)			2.4		V/µs
VOUT High	I_{COMP} = -5.5mA	V_{CC} - 0.5	V_{CC} - 0.3		V
VOUT Low	I_{COMP} = 5.5mA		0.3	0.45	
Oscillator					
Initial Accuracy	T_A = 25°C	525	575	625	kHz
Voltage Stability	T_A = 25°C, V_{CC} = 2.7V to 5.5V		0.05		%/V
Temperature Coefficient	T_A = -40°C to 85°C		0.02		%/°C
Minimum Operation Frequency (1)		50			kHz
Maximum Operation Frequency (1)				1M	Hz
Ramp Peak to Valley			1		V
Ramp Peak Voltage			1.3		V
Ramp Valley Voltage			0.3		V
Sleep, Soft Start, Current Limit					
Sleep Threshold	Measured at FSET			75	mV
Sleep Input Bias Current	V_{SYNC} = 0V		-1		µA
Programmable Soft Start Time (1)	C = 20nF		1.75		ms
Soft Start Charge Current	T_A = 25°C		-5.75		µA
ISET Bias Current	T_J = 25°C	-45	-50	-55	µA
Temperature Coefficient of ISET			0.28		%/°C
Current Limit Blank Time (1)			130		ns
Gate Drive					
DRVH Minimum OFF Time	T_A = 25°C, V_{SENSE} = 0		160	200	ns
Peak Source (DRVH)	Vgs = 3.3V, I_{SOURCE} = 100mA		2.7		Ω
Peak Sink (DRVH)	Vgs = 3.3V, I_{SINK} = 100mA		1.8		Ω
Peak Source (DRVL) (1)	Vgs = 3.3V, I_{SOURCE} = 100mA		2.2		Ω
Peak Sink (DRVL)	Vgs = 3.3V, I_{SINK} = 100mA		1.5		Ω
Output Rise Time	Vgs = 3.3V, C_{OUT} = 4.7nF		35		ns
Output Fall Time	Vgs = 3.3V, C_{OUT} = 4.7nF		27		ns
Minimum Non-Overlap (1)			40		ns

Pin Configuration

TOP VIEW



(MLP12, 4x4)

Ordering Information

Part Number(1)	Device
SC4609MLTRT(2)	MLP-12
SC4609EVB	Evaluation Board

Notes:

(1) Only available in tape and reel packaging. A reel contains 3000 devices.

(2) Lead free product. This product is fully WEEE and RoHS compliant.

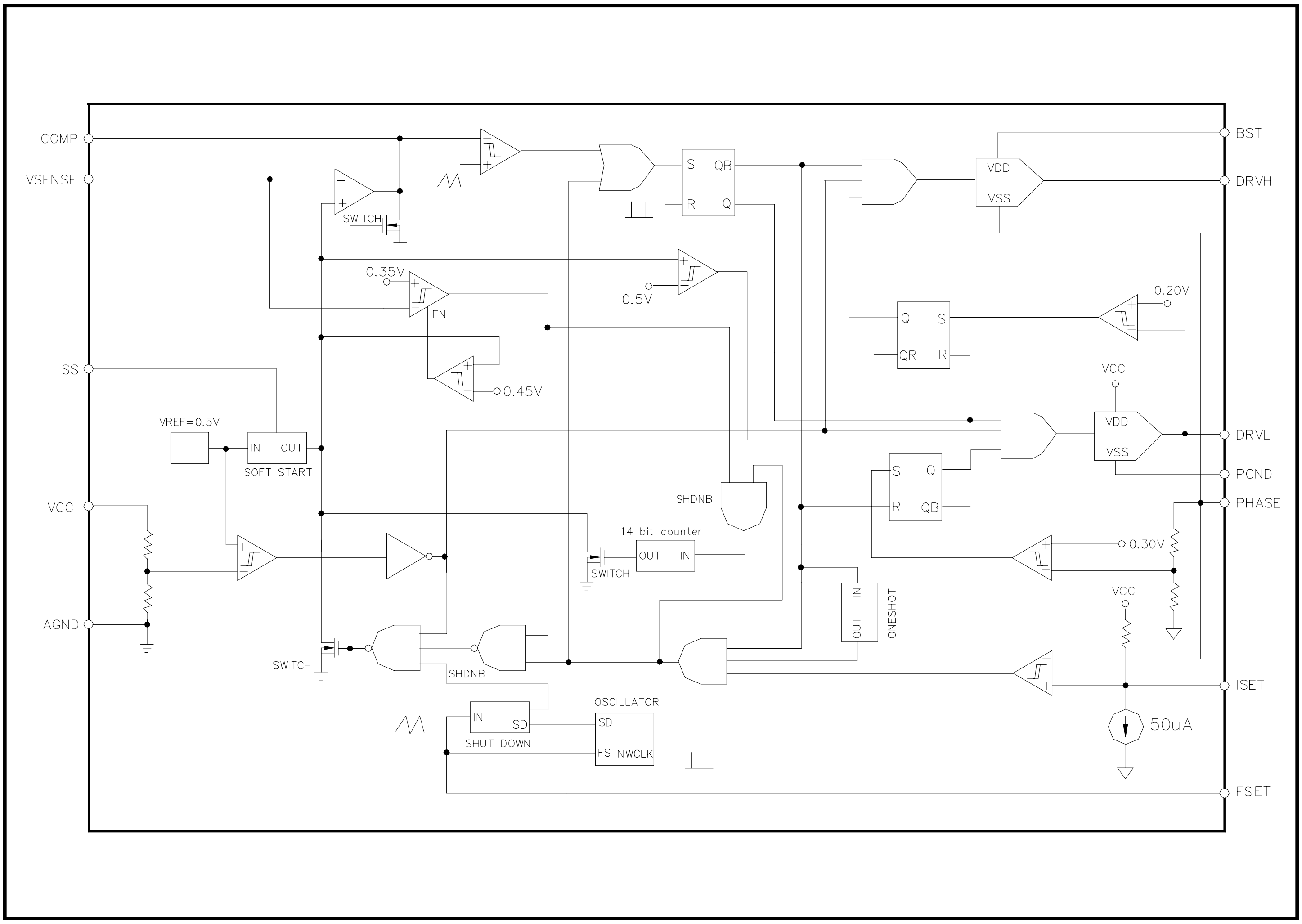
Pin Descriptions

Pin #	Pin Name	Pin Function
1	VCC	Positive supply rail for the IC. Bypass this pin to GND with a 0.1 to 4.7µF low ESL/ESR ceramic capacitor.
2	ISET	The ISET pin is used to limit current in the high side MOSFET. The SC4609 uses the voltage across the V_{IN} and ISET pins in order to set the current limit. The current limit threshold is set by the value of an external resistor (R3 in the Typical Application Circuit Diagram). Current limiting is performed by comparing the voltage drop across the sense resistor with the voltage drop across the drain to source resistance of the high side MOSFET during the MOSFET's conduction period. The voltage drop across the drain to source resistance of the high side MOSFET is obtained from the V_{IN} and PHASE pin.
3	COMP	This is the output of the voltage error amplifier. The voltage at this output is inverted internally and connected to the non-inverting input of the PWM comparator. A lead-lag network from the COMP pin to the VSENSE pin compensates for the two pole LC filter characteristics inherent to voltage mode control. The lead-lag network is required in order to optimize the dynamic performance of the voltage mode control loop.
4	FSET	The FSET pin is used to sets the PWM oscillator frequency through an external timing capacitor that is connected from the FSET pin to the GND pin. When the FSET is pulled and held below 75mV, its sleep mode operation is invoked. Sleep mode operation is invoked by clamping the FSET pin to a voltage below 75mV. The typical supply current during sleep mode is 10µA. The SC4609 can be operated in synchronous mode by placing a resistor in series between the timing capacitor and ground. The other terminal of the timing capacitor will remain connected to the FSET pin.
5	VSENSE	This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the Buck converter. VSENSE is compared to an internal reference value of 0.5V. VSENSE is hardwired to the output voltage when an output of 0.5V is desired. For higher output voltages, a resistor divider network is necessary (R7 and R9 in the Typical Application Circuit Diagram).
6	SS	Soft start. A capacitor to ground sets the soft start time. The soft start time is independent of switching frequency and is defined as $SS = 87.5 \bullet 10^3 \bullet C$. Where C is the external capacitor in nF and soft start time in second.

Pin Descriptions (Cont.)

Pin #	Pin Name	Pin Function
7	AGND	Analog ground.
8	PGND	Power ground.
9	DRVL	DRVL drives the gate of the low side (synchronous rectifier) MOSFET. The output drivers are rated for 1A peak currents. The PWM circuitry provides complementary drive signals to the output stages. The cross conduction of the external MOSFETs is prevented by monitoring the voltage on the driver pins of the MOSFET pair in conjunction with a time delay optimized for FET turn-off characteristics.
10	PHASE	The PHASE pin is used to limit current in the high side MOSFET. The SC4609 uses the voltage across the V_{IN} and ISET pin in order to set the current limit. The current limit threshold is set by the value of an external resistor (R3 in the Typical Application Circuit Diagram). Current limiting is performed by comparing the voltage drop across the sense resistor with the voltage drop across the drain to source resistance of the high side MOSFET during the MOSFET's conduction period. The voltage drop across the drain to source resistance of the high side MOSFET is obtained from the V_{IN} and PHASE pin.
11	DRVH	DRVH drives the gate of the high side (main switch) MOSFET. The output drivers are rated for 1A peak currents. The PWM circuitry provides complementary drive signals to the output stages. The cross conduction of the external MOSFETs is prevented by monitoring the voltage on the driver pins of the MOSFET pair in conjunction with a time delay optimized for FET turn-off characteristics.
12	BST	This pin enables the converter to drive an N-Channel high side MOSFET. BST connects to the external charge pump circuit. The charge pump circuit boosts the BST pin voltage to a sufficient gate-to-source voltage level for driving the gate of the high side MOSFET.
	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Block Diagram



Application Information

Enable

The SC4609 is enabled by applying a voltage greater than 2.7 volts to the VCC pin. The SC4609 is disabled when VCC falls below 2.35 volts or when sleep mode operation is invoked by clamping the FSET pin to a voltage below 75mV. 10µA is the typical current drawn through the VCC pin during sleep mode. During the sleep mode, the high side and low side MOSFETs are turned off and the internal soft start voltage is held low.

Oscillator

The FSET pin is used to set the PWM oscillator frequency through an external timing capacitor that is connected from the FSET pin to the GND pin. The resulting ramp waveform ion the FSET pin is a triangle at the PWM frequency with a peak voltage of 1.3V and a valley voltage of 0.3V. 200ns minimum OFF time for the top switch allows the bootstrap capacitor to be charged during each cycle. The capacitor tolerance adds to the accuracy of the oscillator frequency. The approximate operating frequency and soft start time are both determined by the value of the external timing capacitor as shown in Table 1.

External Timing Capacitor Value (pF)	Frequency (kHz)
120	1000
270	575
470	350
560	295

Table 1. Operating Frequency value Based on the Value of the External Timing Capacitor Placed Across the FSET and GND Pins

Synchronous mode operation is invoked by using a signal from an external clock. A low value resistor (100Ω typical) must be inserted in series with the timing capacitor between the timing capacitor and the GND pin. The other terminal of the timing capacitor will remain connected to the FSET pin. The transformed external clock signal is then connected to the junction of the external timing capacitor and the added resistor R_{SYNC} as shown in Figure 1.

The maximum frequency of the external clock signal can be higher than the natural switching frequency by about 10%.

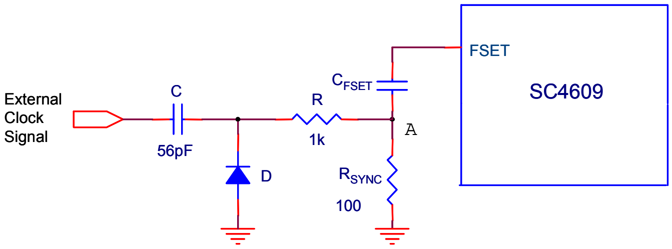


Figure 1

UVLO

When the FSET pin is not pulled and held below 75mV, the voltage on the Vcc pin determines the operation of the SC4609. As Vcc increases during start up, the UVLO block senses Vcc and keeps the high side and low side MOSFETs off and the internal soft start voltage low until Vcc reaches 2.7V. If no faults are present, the SC4609 will initiate a soft start when Vcc exceeds 2.7V. A hysteresis (350mV) in the UVLO comparator provides noise immunity during its start up.

Soft Start

The soft start function is required for step down controllers to prevent excess inrush current through the DC bus during start up. Generally this can be done by sourcing a controlled current into a timing capacitor and then using the voltage across this capacitor to slowly ramp up the error amp reference. The closed loop creates narrow width driver pulses while the output voltage is low and allows these pulses to increase to their steady state duty cycle as the output voltage reaches its regulated value. With this, the inrush current from the input side is controlled. The duration of the soft start in the SC4609 is controlled by an external capacitor. SS, the startup time is difined as:

$$SS = 87.5 \bullet 10^{3} \bullet C$$

where, C is the value of the external capacitor in nF, and SS is the startup time in second.

Over Current Protection

The SC4609 detects over current conditions by sensing the voltage across the drain-to-source of the high side MOSFET. The SC4609 determines the high side MOSFET current level by sensing the drain-to-source conduction voltage across the high side MOSFET via the V_{in} (see the Typical Application Circuit on page 1) and PHASE pin during the high side MOSFET's conduction period. This voltage value is then compared internally to a user programmed current limit threshold. Note that user should place Kelvin sensing connections directly from the high side MOSFET source to the PHASE pin.

The current limit threshold is programmed by the user based on the RDS(on) of the high side MOSFET and the value of the external set resistor RSET (where RSET is represented by R3 in the applications schematics of this document). The SC4609 uses an internal current source to pull a 50µA current from the input voltage to the ISET pin through external resistor RSET.
The current limit threshold resistor (RSET) value is calculated using the following equation:

$$R_{SET} = \frac{I_{MAX} \cdot R_{DS(ON)}}{50\mu A}$$

The $R_{DS(ON)}$ sensing used in the SC4609 has an additional feature that enhances the performance of the over current protection. Because the $R_{DS(ON)}$ has a positive temperature coefficient, the 50µA current source has a positive coefficient of about 0.28%/C° providing first order correction for current sensing vs temperature. This compensation depends on the high amount of thermal transferring that typically exists between the high side N-MOSFET and the SC4609 due to the compact layout of the power supply.

When the converter detects an over current condition ($I > I_{MAX}$) as shown in Figure 2, the first action the SC4609 takes is to enter the cycle by cycle protection mode (Point B to Point C), which responds to minor over current cases. Then the output voltage is monitored. If the over current and low output voltage (set at 70% of nominal output voltage) occur at the same time, the Hiccup mode operation (Point C to Point D) of the SC4609 is invoked and the internal soft start capacitor is discharged. This is like a typical soft start cycle:

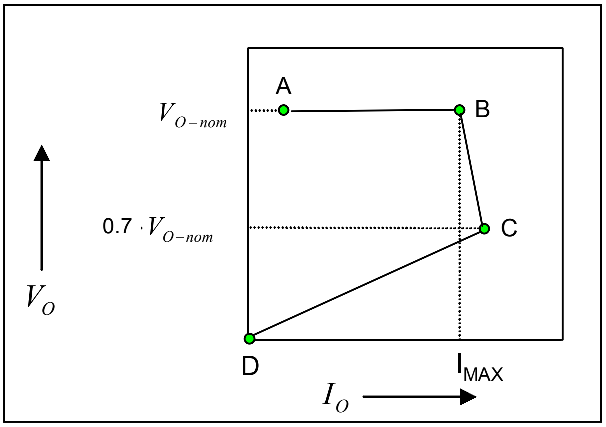


Figure 2. Over current protection characteristic of SC4609

Power MOSFET Drivers

The SC4609 has two drivers which are optimized for driving external power N-Channel MOSFETs.. The driver block consists two 1 Amp drivers. DRVH drives the high side N-MOSFET (main switch), and DRVL drives the low side N-MOSFET (synchronous rectifier transistor).
The output drivers also have gate drive non-overlap mechanism that provides a dead time between DRVH and DRVL transitions to avoid potential shoot through problems in the external MOSFETs. By using the proper design and the appropriate MOSFETs, the SC4609 is capable of driving a converter with up to 12A of output current. As shown in Figure 3, t_{d1} the delay from the top MOSFET off to the bottom MOSFET on is adaptive by detecting the voltage of the phase node. t_{d2}, the delay from the bottom MOSFET off to the top MOSFET on is fixed, is 40ns for the SC4609. This control scheme guarantees avoidance of cross conduction or shoot through between the upper and lower MOSFETs and also minimizes the conduction loss in the body diode of the bottom MOSFET for high efficiency applications.

Application Information (Cont.)

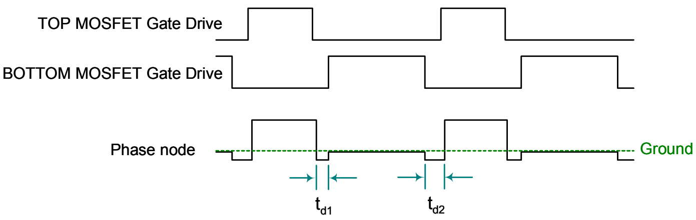


Figure 3. Timing Waveforms for Gate Drives and Phase Node

Inductor Selection

The factors for selecting the inductor include its cost, efficiency, size and EMI. For a typical SC4609 application, the inductor selection is mainly based on its value, saturation current and DC resistance. Increasing the inductor value will decrease the ripple level of the output voltage while the output transient response will be degraded. Low value inductors offer small size and fast transient responses while they cause large ripple currents, poor efficiencies and more output capacitance to smooth out the large ripple currents. The inductor should be able to handle the peak current without saturating and its copper resistance in the winding should be as low as possible to minimize its resistive power loss. A good trade-off among its size, loss and cost is to set the inductor ripple current to be within 15% to 30% of the maximum output current.

The inductor value can be determined according to its operating point and the switching frequency as follows:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot f_s \cdot \Delta I \cdot I_{OMAX}}$$

Where:

f_s = switching frequency and

ΔI = ratio of the peak to peak inductor current to the maximum output load current.

The peak to peak inductor current is:

$$I_{p-p} = \Delta I \bullet I_{OMAX}$$

After the required inductor value is selected, the proper selection of the core material is based on the peak inductor current and efficiency requirements. The core must be able to handle the peak inductor current I_{PEAK} without saturation and produce low core loss during the high frequency operation is:

$$I_{PEAK} = I_{OMAX} + \frac{I_{p-p}}{2}$$

The power loss for the inductor includes its core loss and copper loss. If possible, the winding resistance should be minimized to reduce inductor's copper loss. The core loss can be found in the manufacturer's datasheet. The inductor' copper loss can be estimated as follows:

$$P_{COPPER} = I^2_{LRMS} \cdot R_{WINDING}$$

Where:

I_{LRMS} is the RMS current in the inductor. This current can be calculated as follow is:

$$I_{LRMS} = I_{OMAX} \cdot \sqrt{1 + \frac{1}{3} \cdot \Delta I^2}$$

Output Capacitor Selection

Basically there are two major factors to consider in selecting the type and quantity of the output capacitors. The first one is the required ESR (Equivalent Series Resistance) which should be low enough to reduce the voltage deviation from its nominal one during its load changes. The second one is the required capacitance, which should be high enough to hold up the output voltage. Before the SC4609 regulates the inductor current to a new value during a load transient, the output capacitor delivers all the additional current needed by the load. The ESR and ESL of the output capacitor, the loop parasitic inductance between the output capacitor and the load combined with inductor ripple current are all major contributors to the output voltage ripple. Surface mount speciality polymer aluminum electrolytic chip capacitors in UE series from Panasonic provide low ESR and reduce the total capacitance required for a fast transient response. POSCAP from Sanyo is a solid electrolytic chip capacitor that has a low ESR and good performance for high frequency with a low profile and high capacitance. Above mentioned capacitors are recommended to use in SC4609 application.

Input Capacitor Selection

The input capacitor selection is based on its ripple current level, required capacitance and voltage rating. This capacitor must be able to provide the ripple current by the switching actions. For the continuous conduction mode, the RMS value of the input capacitor can be calculated from:

$$I_{CIN(RMS)} = I_{OMAX} \cdot \sqrt{\frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V^2_{IN}}}$$

This current gives the capacitor's power loss as follows:

$$P_{CIN} = I^2_{CIN(RMS)} \cdot R_{CIN(ESR)}$$

This capacitor's RMS loss can be a significant part of the total loss in the converter and reduce the overall converter efficiency. The input ripple voltage mainly depends on the input capacitor's ESR and its capacitance for a given load, input voltage and output voltage. Assuming that the input current of the converter is constant, the required input capacitance for a given voltage ripple can be calculated by:

$$C_{IN} = I_{OMAX} \cdot \frac{D \cdot (1-D)}{fs \cdot (\Delta V_I - I_{OMAX} \cdot R_{CIN(ESR)})}$$

Where:
$D = V_O/V_I$, duty ratio and
ΔV_I = the given input voltage ripple.

Because the input capacitor is exposed to the large surge current, attention is needed for the input capacitor. If tantalum capacitors are used at the input side of the converter, one needs to ensure that the RMS and surge ratings are not exceeded. For generic tantalum capacitors, it is wise to derate their voltage ratings at a ratio of 2 to protect these input capacitors.

Boost Capacitor Selection

The boost capacitor selection is based on its discharge ripple voltage, worst case conduction time and boost current. The worst case conduction time T_w can be estimated as follows:

$$Tw = \frac{1}{f_s} \cdot D_{max}$$

Where:
f_s = the switching frequency and
Dmax = maximum duty ratio.

The required minimum capacitance for boost capacitor will be:

$$C_{boost} = \frac{I_B}{V_D} \cdot T_W$$

Where:
I_B = the boost current and
V_D= discharge ripple voltage.

With f_s = 300kH, V_D=0.3V and I_B=50mA, the required capacitance for the boost capacitor is:

$$C_{boost} = \frac{I_B}{V_D} \cdot \frac{1}{f_s} \cdot D_{max} = \frac{0.05}{0.3} \cdot \frac{1}{300k} \cdot 0.95 = 528nF$$

Power MOSFET Selection

The SC4609 can drive an N-MOSFET at the high side and an N-MOSFET synchronous rectifier at the low side. The use of the high side N-MOSFET will significantly reduce its conduction loss for high current. For the top MOSFET, its total power loss includes its conduction loss, switching loss, gate charge loss, output capacitance loss and the loss related to the reverse recovery of the bottom diode, shown as follows:

$$P_{TOP\_TOTAL} = I^2_{TOP\_RMS} \cdot R_{TOP\_ON} + \frac{I_{TOP\_PEAK} \cdot V_I \cdot f_s}{V_{GATE}/R_G} \cdot (Q_{GD} + Q_{GS2}) + Q_{GT} \cdot V_{GATE} \cdot f_s + (Q_{OSS} + Q_{rr}) \cdot V_I \cdot f_s$$

Where:
R_G = gate drive resistor,
Q_{GD} = the gate to drain charge of the top MOSFET,
Q_{GS2} = the gate to source charge of the top MOSFET,
Q_{GT} = the total gate charge of the top MOSFET,
Q_{OSS} = the output charge of the top MOSFET and
Q_{rr} = the reverse recovery charge of the bottom diode.

For the top MOSFET, it experiences high current and high voltage overlap during each on/off transition. But for the bottom MOSFET, its switching voltage is the bottom diode's forward drop during its on/off transition. So the switching loss for the bottom MOSFET is negligible. Its total power loss can be determined by:

$$P_{BOT\_TOTAL} = I^2_{BOT\_RMS} \cdot R_{BOT\_ON} + Q_{GB} \cdot V_{GATE} \cdot f_s + I_{D\_AVG} \cdot V_F$$

Where:
Q_{GB} = the total gate charge of the bottom MOSFET and
V_F = the forward voltage drop of the bottom diode.

Application Information (Cont.)

For a low voltage and high output current application such as the 3.3V/1.5V@12A case, the conduction loss is often dominant and selecting low $R_{DS(ON)}$ MOSFETs will noticeably improve the efficiency of the converter even though they give higher switching losses.

The gate charge loss portion of the top/bottom MOSFET's total power loss is derived from the SC4609. This gate charge loss is based on certain operating conditions (f_s, V_{GATE}, and I_O).

The thermal estimations have to be done for both MOSFETs to make sure that their junction temperatures do not exceed their thermal ratings according to their total power losses P_{TOTAL}, ambient temperature T_A and their thermal resistance $R\theta JA$ as follows:

$$T_{J(max)} < T_A + \frac{P_{TOTAL}}{R_{\theta JA}}$$

Loop Compensation Design

For a DC/DC converter, it is usually required that the converter has a loop gain of a high cross-over frequency for fast load response, high DC and low frequency gain for low steady state error, and enough phase margin for its operating stability. Often one can not have all these properties at the same time. The purpose of the loop compensation is to arrange the poles and zeros of the compensation network to meet the requirements for a specific application.

The SC4609 has an internal error amplifier and requires the compensation network to connect among the COMP pin and VSENSE pin, GND, and the output as shown in Figure 4. The compensation network includes C1, C2, R1, R7, R8 and C9. R9 is used to program the output voltage according to

$$V_O = 0.5 \cdot (1 + \frac{R_7}{R_9})$$

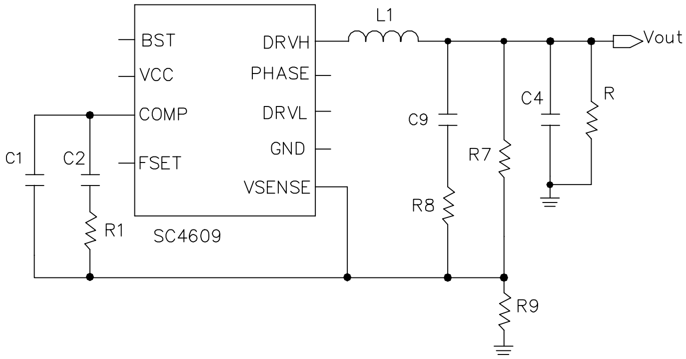


Figure 4. Compensation network provides 3 poles and 2 zeros.

For voltage mode step down applications as shown in Figure 4, the power stage transfer function is:

$$G_{VD}(s) = V_I \frac{1 + \frac{s}{\frac{1}{R_C \cdot C_4}}}{1 + s\frac{L_1}{R} + s^2 L_1 C_4}$$

Where:
R = load resistance and
R_C = C_4's ESR.

The compensation network will have the characteristic as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s} \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot \frac{1 + \frac{s}{\omega_{Z2}}}{\cdot 1 + \frac{s}{\omega_{P2}}}$$

Where

$$\omega_I = \frac{1}{R_7 \cdot (C_1 + C_2)}$$

$$\omega_{Z1} = \frac{1}{R_1 \cdot C_2}$$

$$\omega_{Z2} = \frac{1}{(R_7 + R_8) \cdot C_9}$$

$$\omega_{P1} = \frac{C_1 + C_2}{R_1 \cdot C_1 \cdot C_2}$$

Application Information (Cont.)

$$\omega_{P2} = \frac{1}{R_8 \cdot C_9}$$

After the compensation, the converter will have the following loop gain:

$$T(s) = G_{PWM} \cdot G_{COMP}(s) \cdot G_{VD}(s) = \frac{\frac{1}{V_M} \cdot \omega_I \cdot V_I}{s} \cdot \frac{1+\frac{s}{\omega_{Z1}}}{1+\frac{s}{\omega_{P1}}} \cdot \frac{1+\frac{s}{\omega_{Z2}}}{\cdot 1+\frac{s}{\omega_{P2}}} \cdot \frac{1+\frac{s}{\frac{1}{R_C \cdot C_4}}}{1+s\frac{L_1}{R}+s^2 L_1 C}$$

Where:

G_{PWM} = PWM gain

V_M = 1.0V, ramp peak to valley voltage of SC4609

The design guidelines for the SC4609 applications are as following:

1. Set the loop gain crossover corner frequency ω_C for given switching corner frequency $\omega_S = 2\pi f_S$,
2. Place an integrator at the origin to increase DC and low frequency gains.
3. Select ω_{Z1} and ω_{Z2} such that they are placed near ω_O to damp the peaking and the loop gain has a -20dB/dec rate to go across the 0dB line for obtaining a wide bandwidth.
4. Cancel the zero from C_4's ESR by a compensator pole ω_{P1} ($\omega_{P1} = \omega_{ESR} = 1/(R_C C_4)$).
5. Place a high frequency compensator pole ωp_2 ($\omega p_2 = \pi f_s$) to get the maximum attenuation of the switching ripple and high frequency noise with the adequate phase lag at ω_C.

The compensated loop gain will be as given in Figure 5:

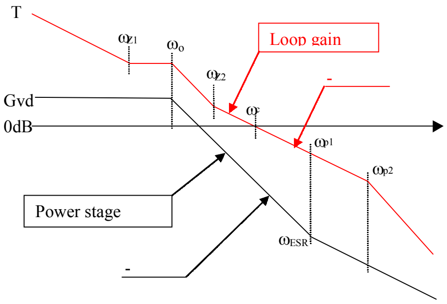


Figure 5. Asymptotic diagrams of power stage and its loop gain

Layout Guidelines

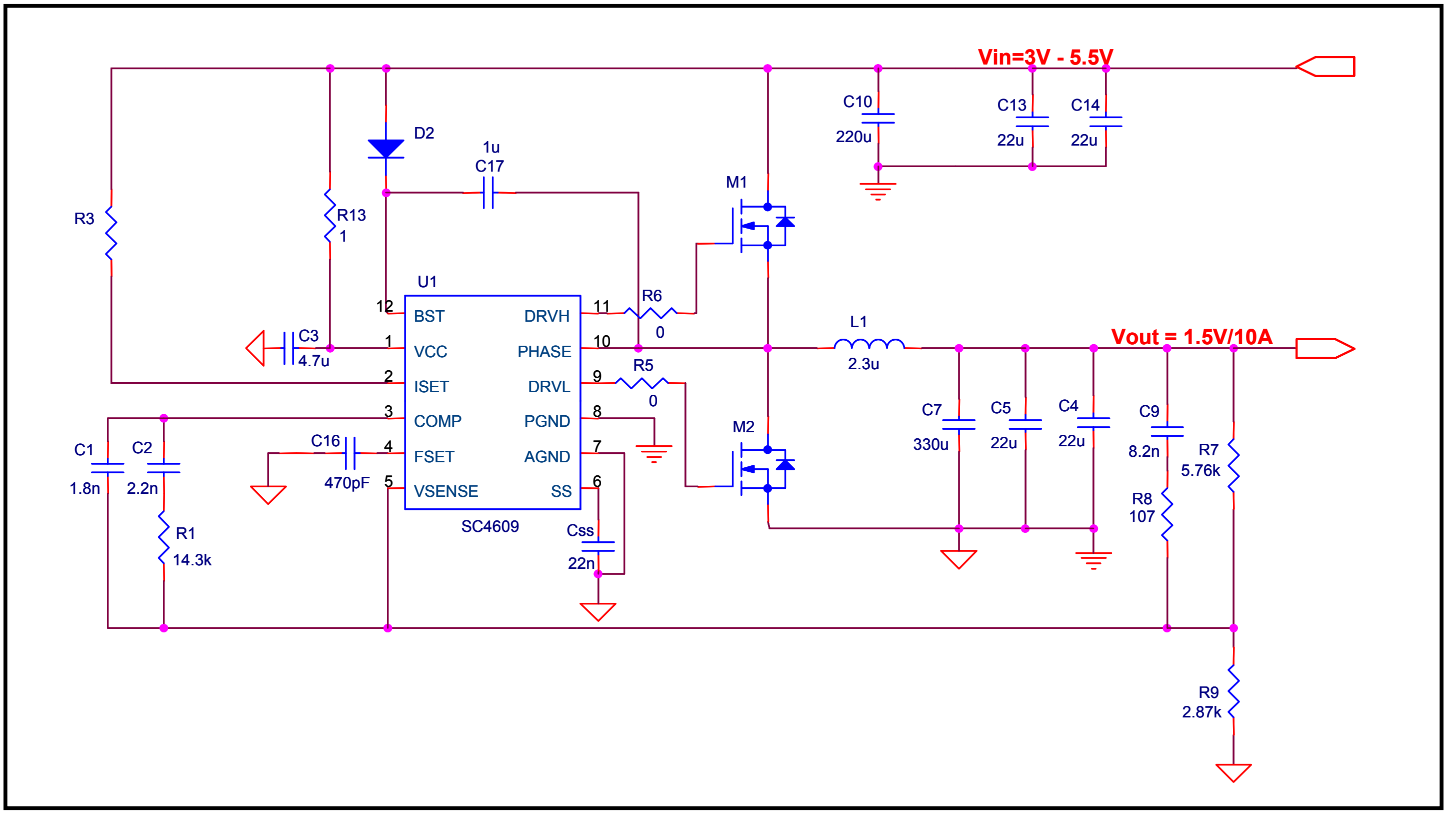
In order to achieve optimal electrical, thermal and noise performance for high frequency converters, special attention must be paid to the PCB layouts. The goal of layout optimization is to identify the high di/dt loops and minimize them. The following guideline should be used to ensure proper functions of the converters.

1. A ground plane is recommended to minimize noises and copper losses, and maximize heat dissipation.
2. Start the PCB layout by placing the power components first. Arrange the power circuit to achieve a clean power flow route. Put all the connections on one side of the PCB with wide copper filled areas if possible.
3. The Vcc bypass capacitor should be placed next to the Vcc and GND pins.
4. The trace connecting the feedback resistors to the output should be short, direct and far away from the noise sources such as switching node and switching components.
5. Minimize the traces between DRVH/DRVL and the gates of the MOSFETs to reduce their impedance to drive the MOSFETs.
6. Minimize the loop including input capacitors, top/bottom MOSFETs. This loop passes high di/dt current. Make sure the trace width is wide enough to reduce copper losses in this loop.
7. ISET and PHASE connections to the top MOSFET for current sensing must use Kelvin connections.
8. Maximize the trace width of the loop connecting the inductor, bottom MOSFET and the output capacitors.

9. Connect the ground of the feedback divider and the compensation components directly to the GND pin of the SC4609 by using a separate ground trace. Then connect this pin to the ground of the output capacitor as close as possible

Application Information (Cont.)

Design Example 1. 3V to1.5V @10A application with SC4609



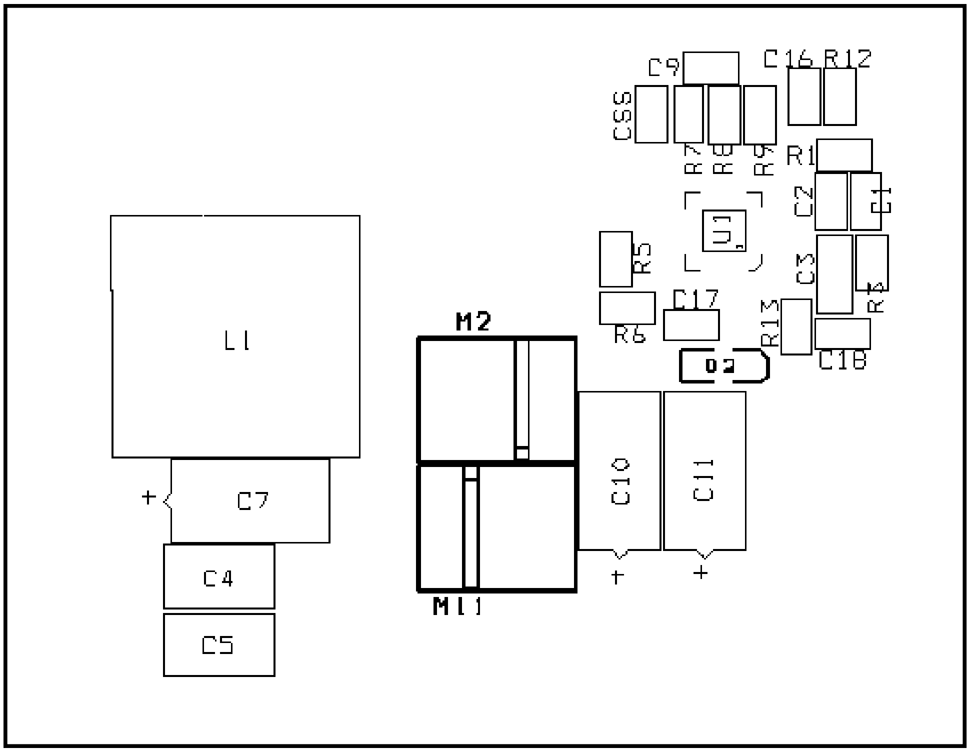
Bill of Materials

Item	Qty	Reference	Value	Part No./Manufacturer
1	1	C1	1.8nF	
2	1	C2	2.2nF	
3	1	C17	1uF	
4	4	C4,C5, C13, C14	22uF, 1206	TDK P/N: C3225X5R0J226M
5	1	C7	330uF, 2870	Sanyo P/N: 6TPB330ML
6	1	C9	8.2nF	
7	1	C16	470pF	
8	1	D2	MBR0520LT1	ON Semi P/N: MBR0520LT1
9	1	L1	2.3uH	Cooper Electronic P/N: HC1-2R3
10	2	M1, M2	Powerpack, SO-8	Vishay P/N: Si7882DP
11	1	R1	14.3K	
12	1	R3	1.33K	
13	1	R7	5.76K	
14	1	R8	107	
15	1	R9	2.87K	
16	1	R13	1	
17	1	C3	4.7uF, 0805	
18	1	C10	220uF, 2870	Sanyo P/N: 6TPB220ML
19	1	Css	22nF	
20	1	U1	SC4609	Semtech P/N: SC4609IMLTRT

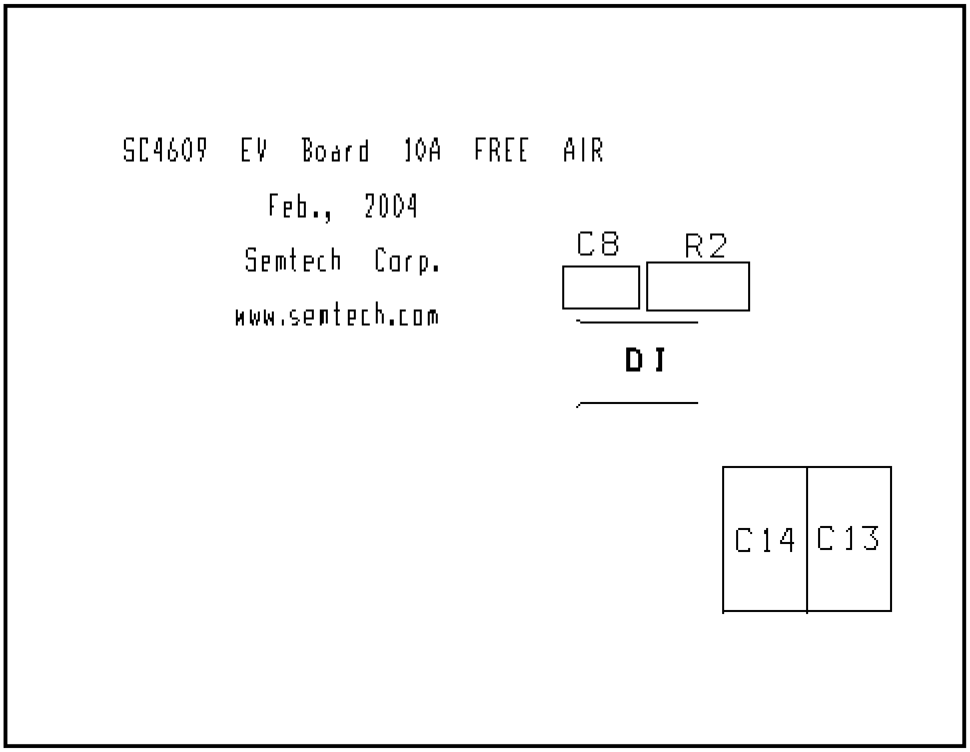
Unless specified, all resistors have 1% precision with 0603 package.
Resistors are +/-1% and all capacitors are +/-20%

PCB Layout

COMPONENT SIDE (TOP)

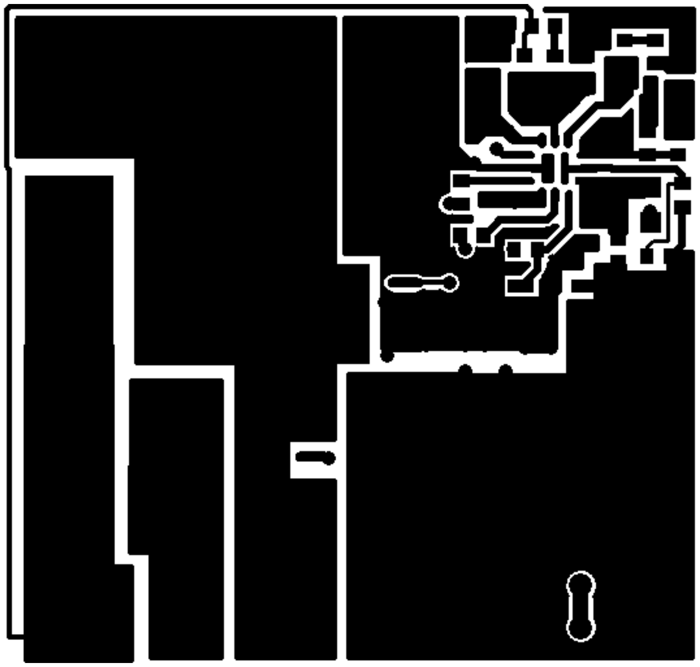


COMPONENT SIDE (BOTTOM)

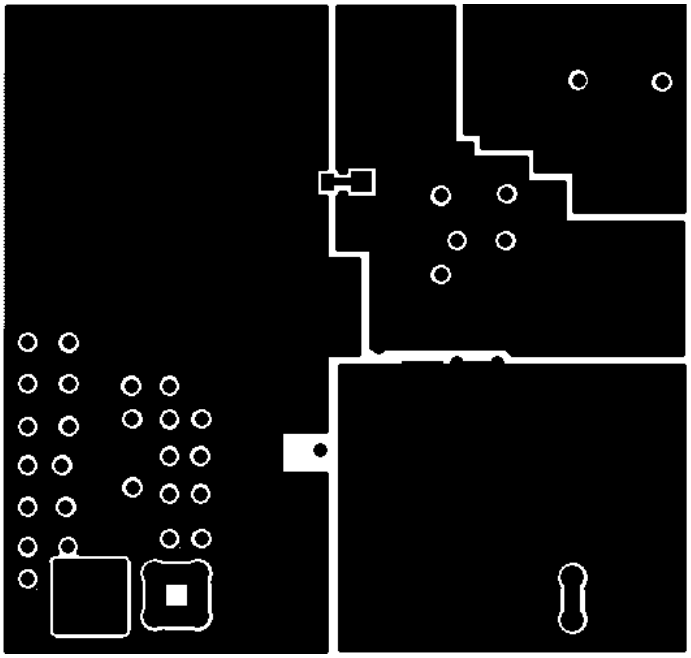


PCB Layout (Cont.)

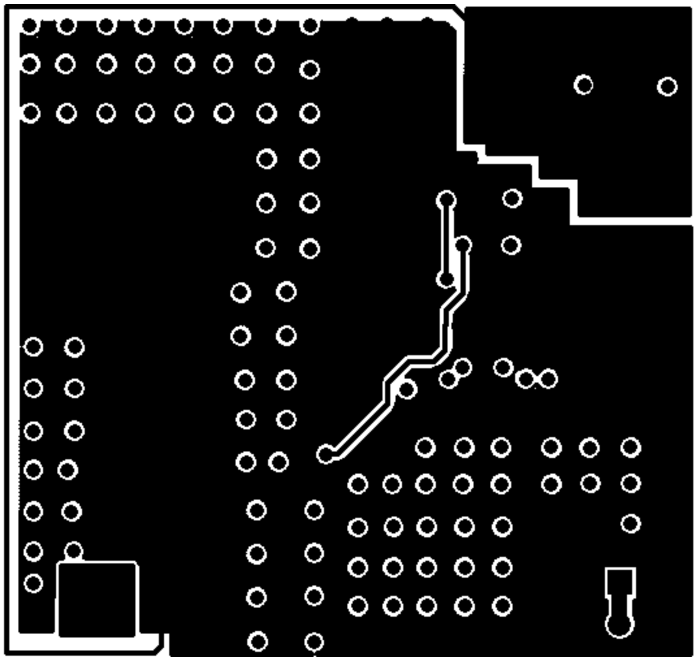
(TOP)



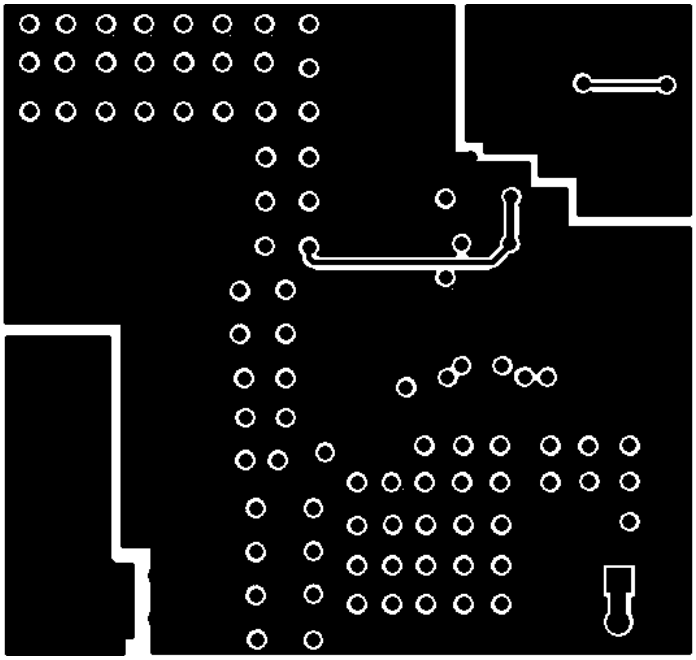
(BOTTOM)



(INTER LAYER 1)

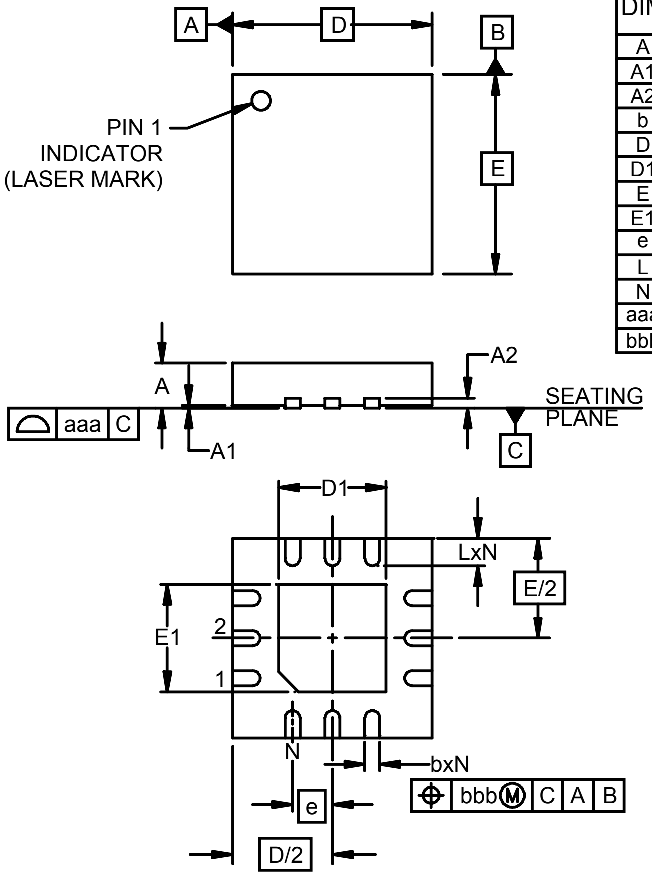


(INTER LAYER 2)



Outline Drawing - MLP-12

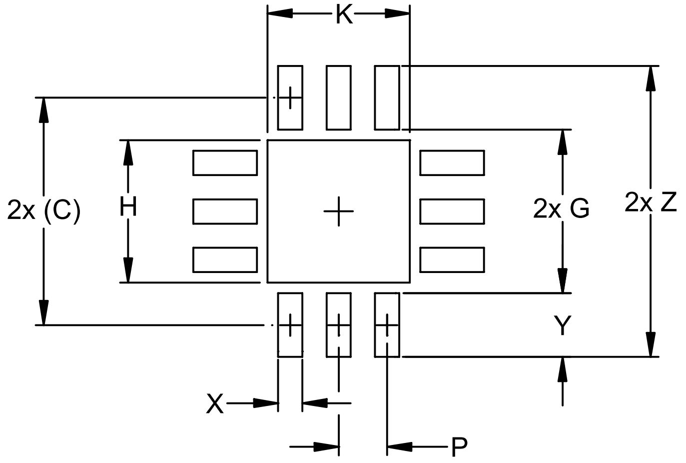
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.040	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.010	.012	.014	0.25	0.30	0.35
D	.153	.157	.161	3.90	4.00	4.10
D1	.074	.085	.089	1.90	2.15	2.25
E	.153	.157	.161	3.90	4.00	4.10
E1	.074	.085	.089	1.90	2.15	2.25
e	.031 BSC			0.80 BSC		
L	.018	.022	.026	0.45	0.55	0.65
N	12			12		
aaa	.003			0.08		
bbb	.004			0.10		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLP-12



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.148)	(3.75)
G	.106	2.70
H	.091	2.30
K	.091	2.30
P	.031	0.80
X	.016	0.40
Y	.041	1.05
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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