SC420

High Speed, Combi-Sense™, Synchronous Power MOSFET Driver for Mobile Applications

POWER MANAGEMENT

Description

The SC420 is a cost effective Dual MOSFET Driver, incorporating Semtech's patented Combi-Sense™ technology, designed for switching High and Low side Power MOSFETs in Step-down Switching regulators. A 20ns max propagation delay from input transition to the gate of the power FET's guarantees operation at high switching frequencies. Internal overlap protection circuit prevents shoot-through from Vin to GND in the main and synchronous MOSFETs.

High current drive capability (2A peak) allows fast switching, thus reducing switching losses at high (up to 1.5MHz) frequencies without causing thermal stress on the driver.

The high voltage CMOS process allows operation up to 27 Volts, making the SC420 suitable for adaptor powered applications. Under-voltage-lockout and over-temperature shutdown features are included for proper and safe operation. The SC420 is offered in a space saving MLP-12 package.

Features

- High efficiency
- Shutdown mode for increased power saving
- Tri-state capability
- Fast rise and fall times (15ns typical with 3000pF load)
- 5V gate drive
- Ultra-low (<20ns) propagation delay (BG going low)
- Adaptive and programmable non-overlapping gate drives provide shoot-through protection
- Floating top drive switches up to 27V
- High frequency (to 1.5 MHz) operation allows use of small inductors and low cost ceramic capacitors
- Under-voltage lockout
- Low quiescent current
- MLP packaging provides superior thermal performance in a small footprint

Applications

- High efficiency portable and notebook computers
- Battery powered applications

Conceptual Application Circuit

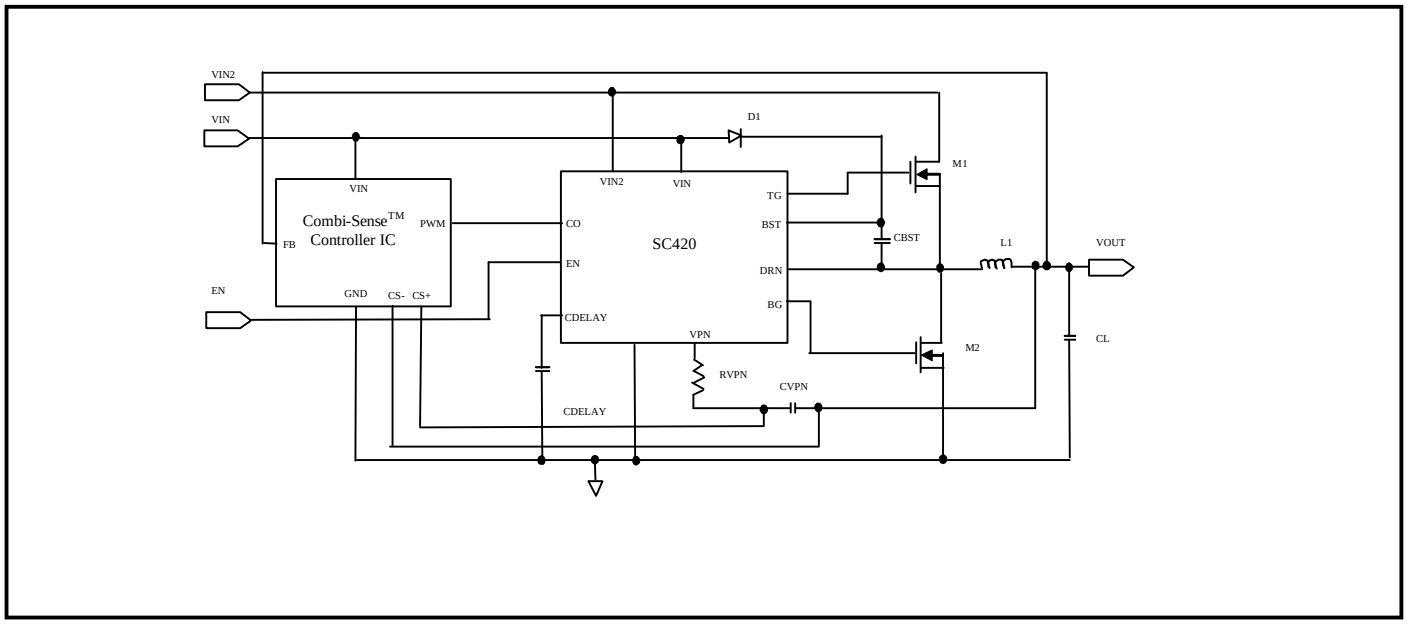


Figure 1

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Conditions	Min	Max	Units
VIN2 Supply Voltage	VIN2			30	V
BST to PGND				40	V
BST to DRN				VIN + 2	V
DRN to PGND		t_{PULSE}<100ns	- 5	34	V
		static	- 2	30	
TG			- 2	BST + 0.3	V
BG			- 0.3	VIN + 0.3	V
VPN to PGND	VPN			30	V
VIN to PGND	VIN			7	V
EN, CO, CDELAY			- 0.3	VIN + 0.3	V
Continuous Power Dissipation	P_D	Tamb = 25 °C,T_J = 125 °C Tcase = 25 °C, T_J = 125°C		0.66 2.56	W
Thermal Resistance Junction to Case	θ_{JC}			3	°C/W
Thermal Resistance Junction to Ambient (1)	θ_{JA}			48	°C/W
Operating Junction Temperature Range	T_J		- 40	125	°C
Storange Temperature Range	T_{STG}		- 65	150	°C
Peak IR Reflow (10-40 sec)	$T_{IRreflow}$			240	°C

Note:
(1) Performance when used according to manufacturing guidelines, refer to Applications Information section for more information
(2) Specification refers to application circuit in Figure 1

Electrical Characteristics

Unless specified: T_A = 25°C; V_{IN} = 5V; 0V ≤ V_{DRN} ≤ 25V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	VIN		4.75	5	6	V
	VIN2				27	V
Quiescent Current, Operating (static)	IQ_{op}	CO = 0V, EN > 2.2V		2.3		mA
Quiescent Current, Tri-state	IQ_{ts}	CO floating		2.3		mA
Quiescent Current, Shutdown	IQ_{sd}	CO = 0V, EN = 0V		0.2	20	µA

(1) Guaranteed by design

Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C; V_{IN} = 5V; 0V ≤ V_{DRN} ≤ 25V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under Voltage Lockout						
Start Threshold (ramping up)	VIN		4.1	4.3	4.55	V
Hysteresis	Vhys		100	200	350	mV
Under-Voltage Lockout Time Delay						
VIN ramping up (1)	$tpdh_{UVLO}$			2		µs
VIN ramping down (1)	tpd_{LUVLO}			2		µs
EN						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
CO						
High Level Input Voltage			2.0			V
Low Level Input Voltage					0.8	V
Tri-state Level		CO floating	1.0		1.9	V
Thermal Shutdown						
Over Temperature Trip Point (1)	T_{OTP}			165		°C
Hysteresis (1)	T_{HYST}			10		°C
High Side Driver (TG)						
Peak Output Current (1)	I_{PKH}			1.3		A
Output Resistance	R_{SRC_TG}	I = 100mA, V_{BST}-V_{DRN} = 5V		3.4		Ω
	R_{SINK_TG}	I = 100mA, V_{BST}-V_{DRN} = 5V		1.1		Ω
Rise Time (1)	tr_{TG}	CL = 3nF, V_{BST} - V_{DRN} = 5V		15	24	ns
Fall Time (1)	tf_{TG}			15	24	ns

(1) Guaranteed by design

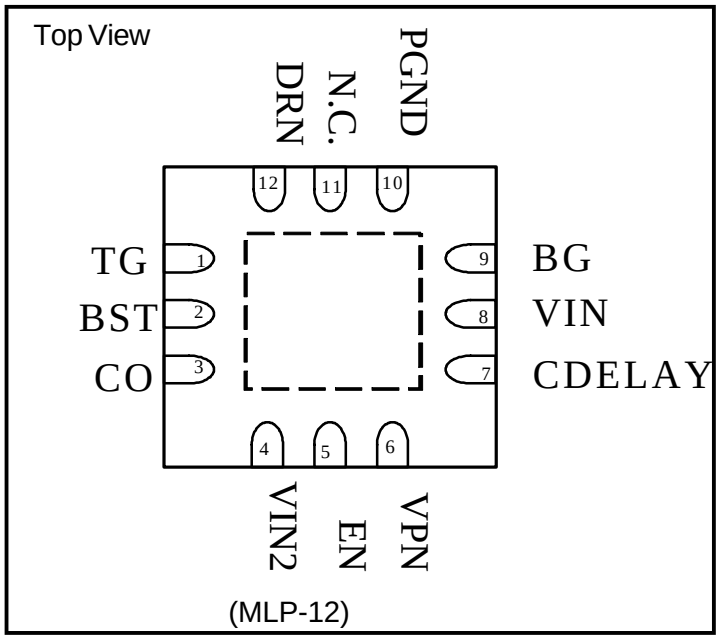
Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C; V_{IN} = 5V; 0V ≤ V_{DRN} ≤ 25V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Propagation Delay, TG Going High (1)	tpdhTG	CTG = 3nF,BG = 0V	20			ns
Propagation Delay, TG Going Low (1)	tpdlTG	CTG = 3nF,DRN = 0V	15			ns
Low-Side Driver (BG)						
Peak Output Current (1)	I_{PKL}			2.0		A
Output Resistance	R_{SRC_BG}	I = 100mA		3.4		Ω
	R_{SINK_BG}	I = 100mA		0.9		Ω
Rise Time (1)	tr_{BG}	C_{BG} = 3nF		15	24	ns
Fall Time (1)	tf_{BG}	C_{BG} = 3nF		10	17	ns
Propagation Delay,BG Going High (1)	$tpdh_{BG}$	C_{BG}=3nF, DRN = 0V		12		ns
Propagation Delay,BG Going Low (1)	$tpdl_{BG}$	C_{BG} = 3nF		15		ns
Shoot-thru Protection (CDELAY)						
Shoot-thru Protection Delay Time (1)	tspd	C_{CDELAY} open		20		ns
Programmed Delay				1		ns/pF
CDELAY charge current	I_{CDELAY}			500		µA
Virtual Phase Node (VPN)						
Output Resistance	R_{SRC_VPN}			65		Ω
	R_{SINK_VPN}			90		
Leakage	I_{LEAK_VPN}				600	nA

(1) Guaranteed by design

Pin Configuration



Ordering Information

Device (1)	Package	Temp Range (T_J)
SC420IMLTR	MLP-12	-40° to 125°C

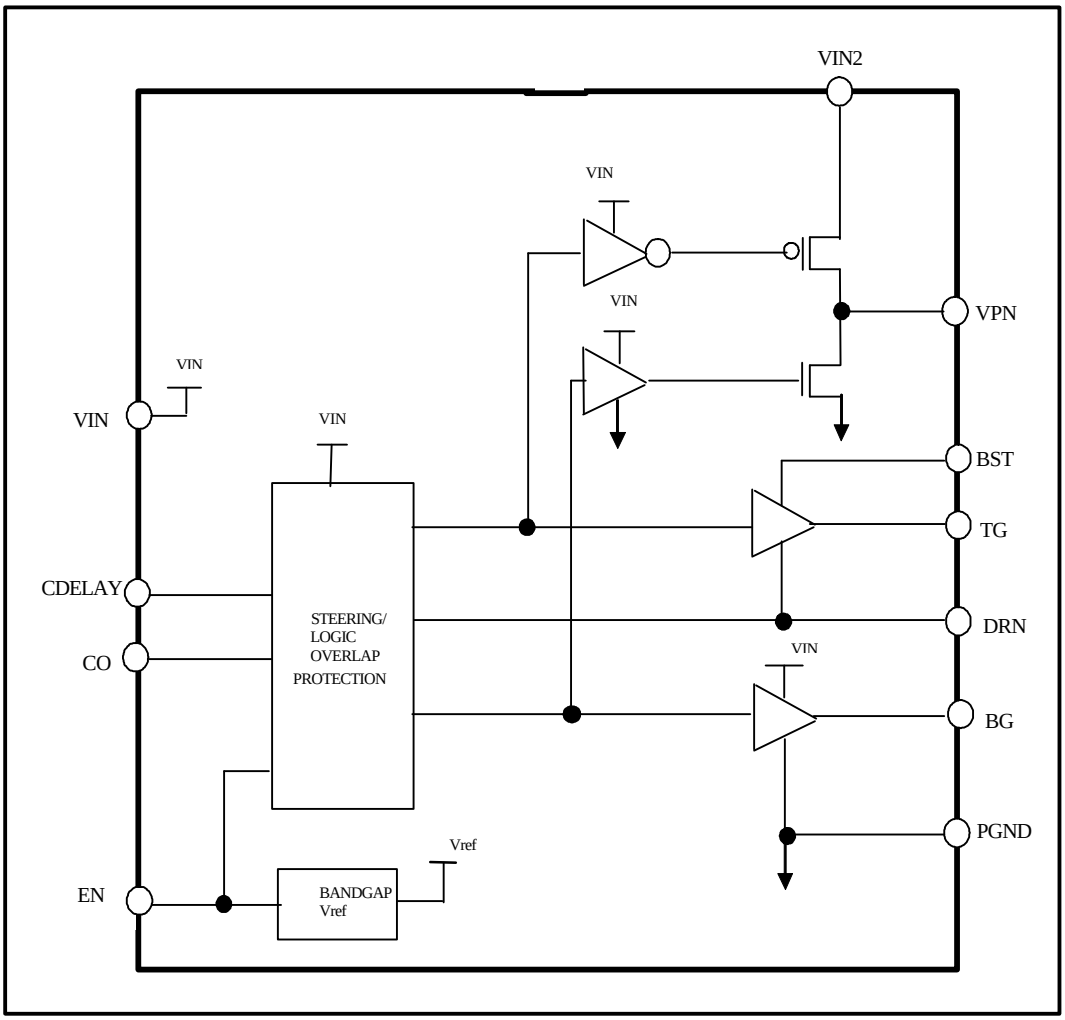
Note:
(1) Only available in tape and reel packaging. A reel contains 3000 devices.

(2) This device is ESD sensitive. Use of standard ESD handling precautions is required.

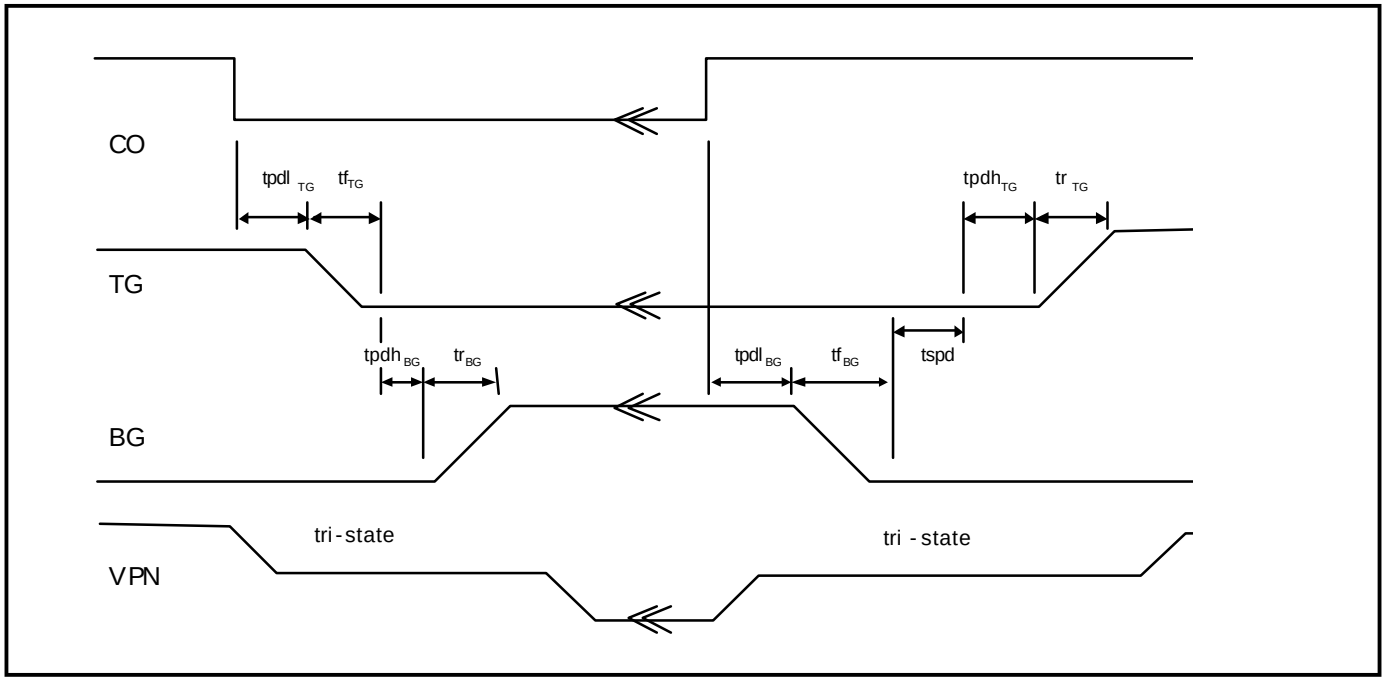
Pin Descriptions

Pin #	Pin Name	Pin Function
1	TG	Output gate drive for the switching (high-side) MOSFET.
2	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1µF and 1µF (ceramic).
3	CO	Logic level PWM input signal to the SC420 supplied by external controller.
4	VIN2	Input power (VBAT) to the DC/DC converter. Used as supply reference for internal Combi-Sense ™ circuitry. Connect as close as possible to Drain of TOP switching MOSFET.
5	EN	Active high logic level input signal. A logic High enables TG and BG switching. A low level disables outputs and reduces quiescent current to IQ_{SD}
6	VPN	Virtual Phase Node. Connect an RC between this pin and the output sense point to Enable Combi-Sense ™ operation.
7	CDELAY	The capacitance connected between this pin and GND sets the additional propagation delay for BG going low to TG going high. Total propagation delay =20ns + 1ns/pF. If no capacitor is connected, the propragation delay = 20ns.
8	VIN	Input supply for the bottom drive and the Logic. A 1µF-10µF Ceramic Capacitor must be connected from this pin to PGND, placed less than 0.5" from SC420.
9	BG	Output drive for the synchronous (bottom) MOSFET.
10	PGND	Ground. Keep this pin close to the synchronous MOSFETs source.
11	N.C.	No Connect
12	DRN	This pin connects to the junction of the switching and synchronous MOSFETs . This pin can be subjected to a -2V minimum relative to PGND without affecting operation.

Block Diagram



Timing Diagram



Applications Information

Combi-Sense (Lossless current sense)

The Combi-Sense is a way to sense the output current on a combination of power devices. There is no sense resistor and the current is sensed on: Top MOSFET, bottom MOSFET and output inductor.

An internal phase node VPN sends a signal which is integrated by the Combi-Sense network. This network consists of a resistor and capacitor in series, connected between VPN and the DRN pins. The resulting signal is large, clean and not duty cycle sensitive. It can be used directly for close loop current mode control and current limit.

Fast Switching Drives

As the switching frequency of PWM controllers is increased to reduce power supply volume and cost, fast rise and fall times are necessary to minimize switching losses (TOP MOSFET) and reduce dead-time (BOTTOM MOSFET) losses. While low Rds_On MOSFET's present a power saving, the MOSFETs die area is larger and the effective input capacitance of the MOSFET is increased. Often a 50% decrease in Rds_On doubles the effective input gate charge, which must be supplied by the driver. The Rds_On power savings can be offset by the switching and dead-time losses with a suboptimum driver. While discrete solution can achieve reasonable drive capability, implementing shoot-through, programmable delay and other housekeeping functions necessary for safe operation can become cumbersome and costly. The SC420 presents a total solution for the high-speed, high power density applications. Wide input supply range of 4.5V-25V allows use in battery powered applications, new high voltage, distributed power supplies.

Shoot Through Protection

The control input (CO) to the SC420 is typically supplied by a PWM controller that regulates the power supply output. The timing diagram demonstrates the sequence of events by which the top and bottom drive signals are applied. The shoot-through protection is implemented by holding the bottom FET off until the voltage at the phase node (intersection of top FET source, the output inductor and the bottom FET drain) has dropped below 1V. This assures that the top FET has turned off and that a direct current path does not exist between the input supply and ground, a shoot-through condition during which both the top and bottom FET's could be on momentarily. The top FET is also prevented from turning on until the bottom FET is off. The top FET turn-on delay is internally set to 20ns (typical) and may be programmably extended by an external capacitor on the Cdelay pin, the delay is increased by 1ns/pf.

The EN (enable) pin may be used to turn both TG and BG drives off. This lowers power consumption by reducing the quiescent current draw of the SC420 to IQsd.

Tri-State

If the CO pin is undriven it will float to an internally defined voltage of 1.4V. This will switch the TG and BG pins low and also tri-states the VPN node.

Over Temperature Shutdown

The SC420 will shutdown by pulling both driver's low if its junction temperature, T_J, exceeds 165°C. The drivers will resume operation when T_J declines below 155°C.

Layout Guidelines

As with any high speed , high current, switching regulator circuit, proper layout is critical in achieving optimum performance of the SC420. The Combi-Sense™ Controller Evaluation board schematic shows a three-phase synchronous design with all surface mountable components.

Tight placement and short, wide traces must be used in layout of The gate drives, DRN, and especially PGND pin. The top gate driver supply voltage is provided by bootstrapping the boost supply and adding it to the phase node (DRN) voltage. Since the bootstrap capacitor supplies the charge to the top gate, it must be less than 0.5in away from the SC420. Ceramic X7R capacitors are a good choice for supply bypassing near the chip.

Supply Voltage

The SC420 can operate from 4.75V to 6V. The V_{IN} pin bypass capacitor must also be less than 0.5in away from the SC420. The ground node of this capacitor, the SC420 PGND pin and the Source of the bottom FET must

Applications Information (Cont.)

be very close to each other, preferably with common PCB copper land with multiple vias to the ground plane (if used). The parallel Schottky (if used) must be physically next to the Bottom FET's drain and source pins. Any trace or lead inductance in these connections will drive current way from the Schottky and allow it to flow through the FET's Body diode, thus reducing efficiency.

Preventing Inadvertent Bottom FET Turn-on

At high VIN2 input voltages, (12V and greater) a fast turn-on of the top FET creates a positive going spike on the Bottom FET's gate through the Miller capacitance, Crss of the bottom FET. The voltage appearing on the gate due to this spike is:

$$V_{SPIKE} = \frac{Vin * Crss}{(Crss + Ciss)}$$

Where Ciss is the input gate capacitance of the bottom FET. This is assuming that the impedance of the drive path is too high compared to the instantaneous impedance of the capacitors, since dV/dT and thus the effective frequency is very high. If the BG pin of the SC420 is very close to the bottom FET, Vspike will be reduced depending on trace inductance, rate of rise of current, etc.

A capacitor may be added from the gate of the Bottom FET to its source, preferably less than 0.5in away. This capacitor will be added to Ciss in the above equation to reduce the effective spike voltage.

The bottom MOSFET must be selected with attention paid to the Crss/Ciss ratio. A low ratio reduces the Miller feedback and thus reduces Vspike. Also MOSFETs with higher Turn-on threshold voltages will conduct at a higher voltage and will not turn on during the spike. A zero ohm bottom FET gate resistor will obviously help keeping the gate voltage low during off time.

Ultimately, slowing down the top FET by adding gate resistance will reduce di/dt which will in turn make the effective impedance of the capacitors higher, thus allowing the BG driver to hold the bottom gate voltage low. It does this at the expense of increased switching times (and switching losses) for the top FET.
The top MOSFET source must be close to the bottom MOSFET drain to prevent ringing and the possibility of the phase node going negative. This frequency is determined by:

$$F_{ring} = \frac{1}{(2\Pi * Sqrt\,(L_{ST} * Coss)} = \frac{1}{2\pi\sqrt{L_{ST} * C_{OSS}}}$$

-Where:

L_{st} = The effective stray inductance of the top FET added to trace inductance of the connection between top FET's source and the bottom FET's drain added to the trace resistance of the bottom FET's ground connection.
C_{OSS} = Drain to source capacitance of bottom FET. If there is a Schottky used, the capacitance of the Schottky is added to this value.

Although this ringing does not pose any power losses due to a fairly high Q, it could cause the phase node to go too far negative, thus causing improper operation, double pulsing or at worst driver damage. On the SC420, the drain node, DRN, can go as far as 2V below ground without affecting operation or sustaining damage.

The ringing is also an EMI nuisance due to its high resonant frequency. Adding a capacitor, typically 1000-2000pf, in parallel with Coss of the bottom FET will often eliminate the EMI issue.

Prevent Driver Overvoltage

The negative voltage spikes on the phase node adds to the bootstrap capacitor voltage, thus increasing the voltage between VBST - VDRN. *This is of special importance if higher boost voltages are used.* If the phase node negative spikes are too large, the voltage on the boost capacitor could exceed device's absolute maximum rating of 7V. To eliminate the effect of the ringing on the boost capacitor voltage, place a 4.7 - 10 Ohm resistor between boost Schottky diode and V_{IN} to filter the negative spikes on DRN Pin. Alternately, a Silicon diode, such as the commonly available 1N4148 can substitute for the Schottky diode and eliminate the need for the series resistor.

Proper layout will guarantee minimum ringing and eliminate the need for external components. Use of surface mount MOSFETs, while increasing thermal resistance, will reduce lead inductance as well as radiated EMI.

Applications Information (Cont.)

Start-up Sequencing

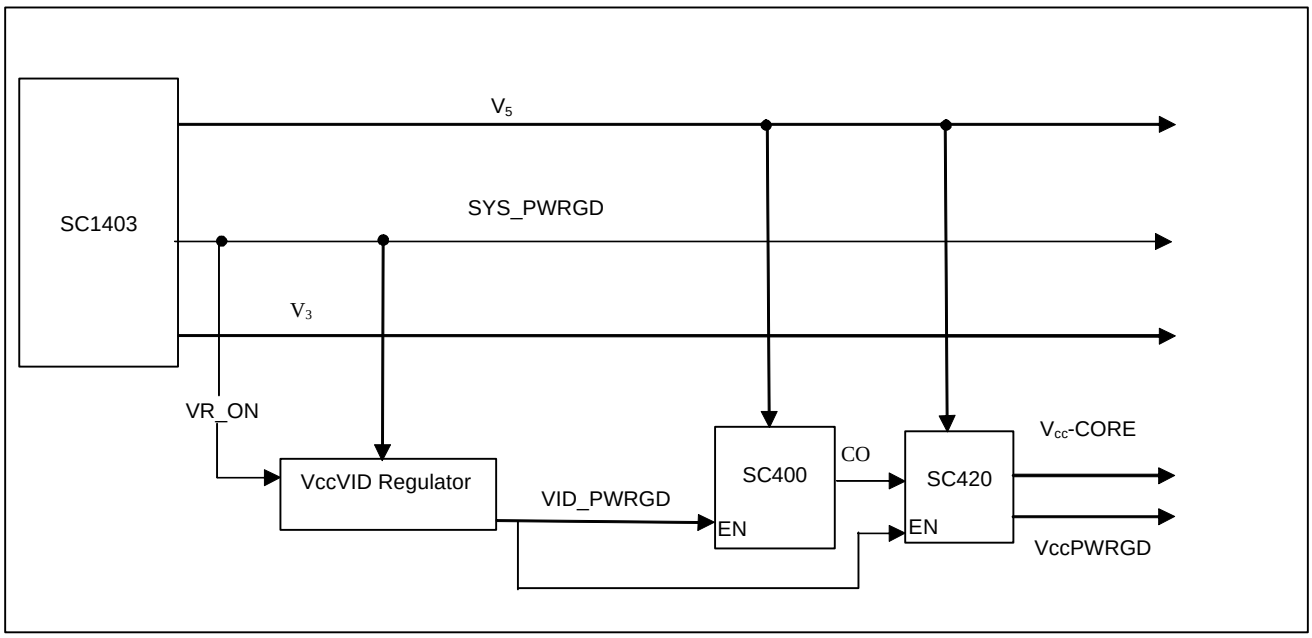
Proper sequencing of the Combi-Sense™ Controller and SC420 driver during both start-up and shut-down is very important. In general, the design must ensure that the driver powers up (during start-up) before the controller does, and that the driver powers down last during shut-down. This ensures that the driver will never puts out gate drive pulses which are not well-controlled, a situation that can lead to MOSFET damage.

In general it is recommended that the Vcc's for the Combi-Sense™ Controller and SC420 be connected to the same (5V) supply. If the EN controls are not used (tied high) then the UVLO settings for the controller and driver will guarantee the proper sequencing (the SC420 maximum UVLO value is guaranteed to be lower than the Combi-Sense™ Controller minimum UVLO value).

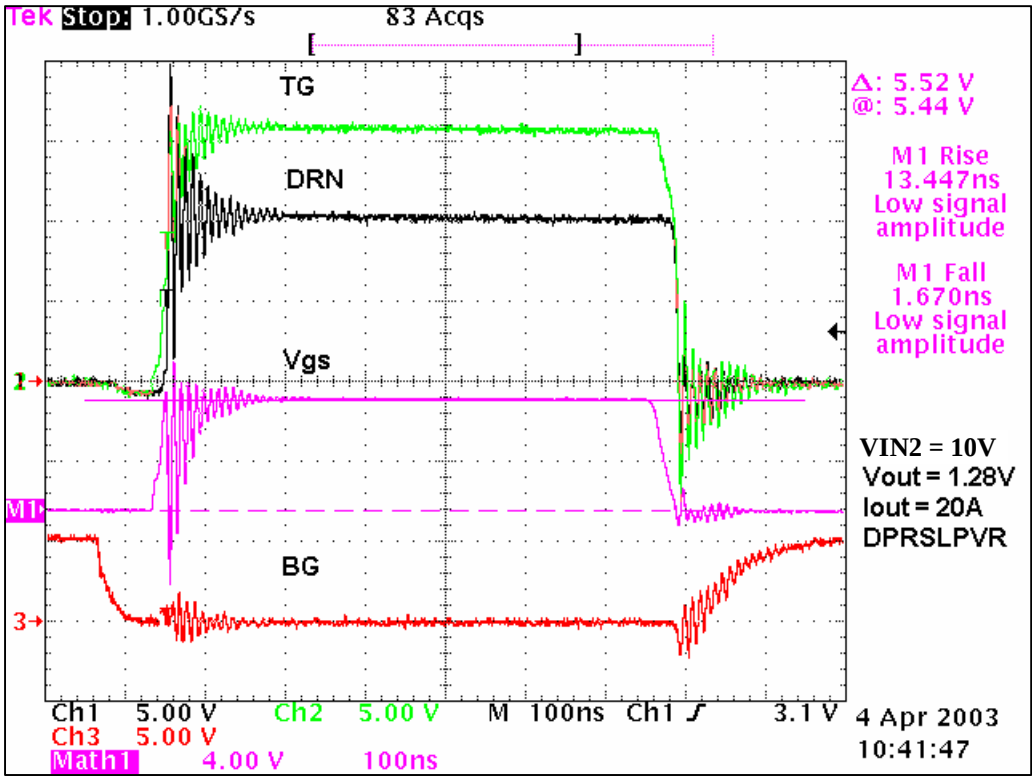
For absolute guarantee of proper sequencing it is recommended that the EN controls be used as shown in the following block diagram. With this arrangement the delayed PWRGD signal from the VccVID regulator is used to enable both ICs. The Soft-Start time established for the controller ensures it will come up well after the SC420. During power-down de-assertion of VID_PWRGD will ensure simultaneous disabling of the Combi-Sense™ Controller and SC420.

Manufacturing Guidelines

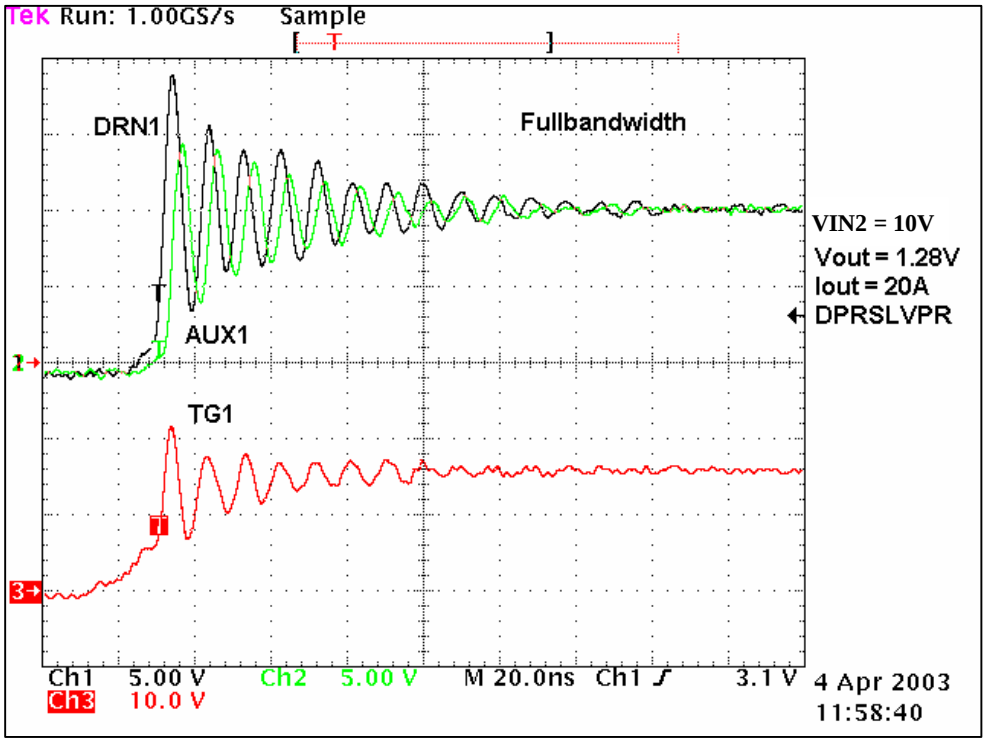
Detailed information on manufacturing and rework of PCBs using the MLP package can be found in the MLP application note "Comprehensive User's Guide - Micro Lead Frame Package" dated April 2002. Please contact your local Semtech representative to obtain a copy of this application note.



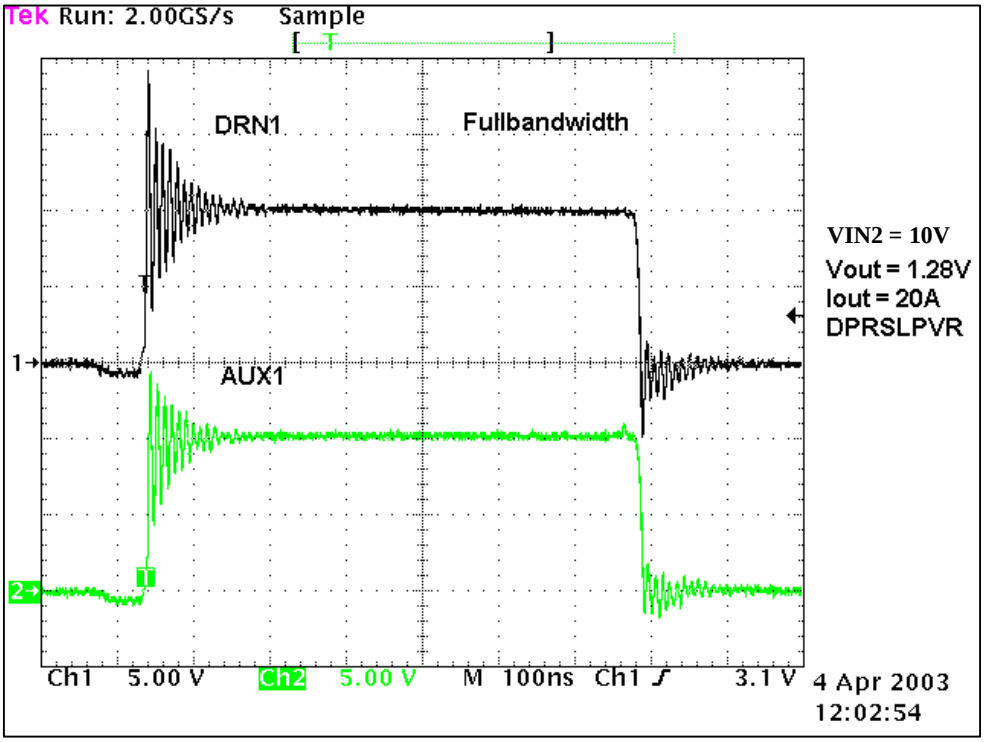
TG, BG, and DRN Waveforms



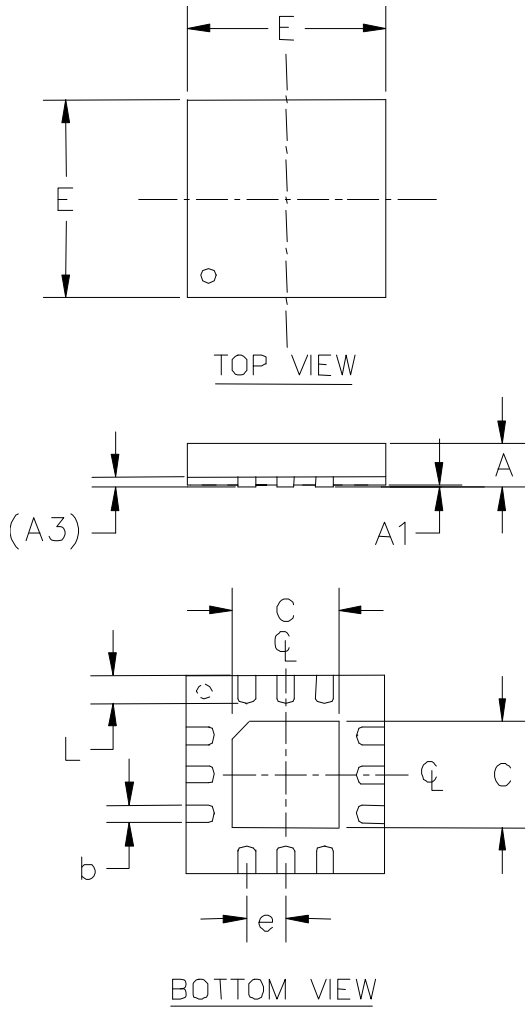
Zoom in on TG, BG, and AUX Rising



DRN and AUX Timing



Outline Drawing - MLP-12



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.032	.039	0.80	1.00	—
A1	0	.002	0	0.05	—
A3	—	.008	—	0.20	REF
b	.011	.016	0.28	0.40	—
C	.079	.088	2.00	2.25	—
E	.157		4.00		NOM
e	.031 BSC		0.80 BSC		—
L	.018	.025	0.45	0.65	—

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