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TELETEXT IC FOR ANALOG AND DIGITAL TV

GENERAL DESCRIPTION

The SAA9042 is a CMOS integrated circuit designed for reception, decoding and display of 625 and 525 line World System Teletext (WST).

It is used in conjunction with a teletext video processor (SAA5235/6 or SAA5191) for data regeneration, and a single-chip 64 K x 4-bit or 256 K x 4-bit dynamic RAM page memory.

The SAA9042 acquires teletext packets defined at levels 1, 2 and 3 in the WST specification and produces a level 1 display.

The device is μC controlled via the standard I^{2}C-bus and is compatible with analog, digital and features TV.

Features

General

- Interfaces with the Philips digital TV chip-set
- Interfaces with analog TV
- Directly interfaces up to 1 Mbit dynamic RAM
- Fully independent acquisition and display timing
- 3 display modes
  - normal
  - 32 kHz (progressive scan)
  - 100 Hz/120 Hz (field doubling)
- I^{2}C controlled
- Single 5 V power supply

Acquisition

- Simultaneous update of up to 8 pages
- Up to 100 page background memory capability
- Software selectable 625/525 line operation
- Full level One Features (FLOF) operation
- TOP compatible
- VPT compatible
- VBI and full channel operation
- Extension packets 26/27/28/29 and 30 fully decoded

Display

- Stable display by slaving from scan-related timing signals
- Automatic selection of six different languages
- Storage of 192 characters (13 x 10 dot matrix)
- Software controlled RGB level removes the need for hardware adjustment
- Up to 27 display rows; 0 to 24 and up to 2 status rows

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

INTEGRATED CIRCUITS
IC02

9397 290 20011

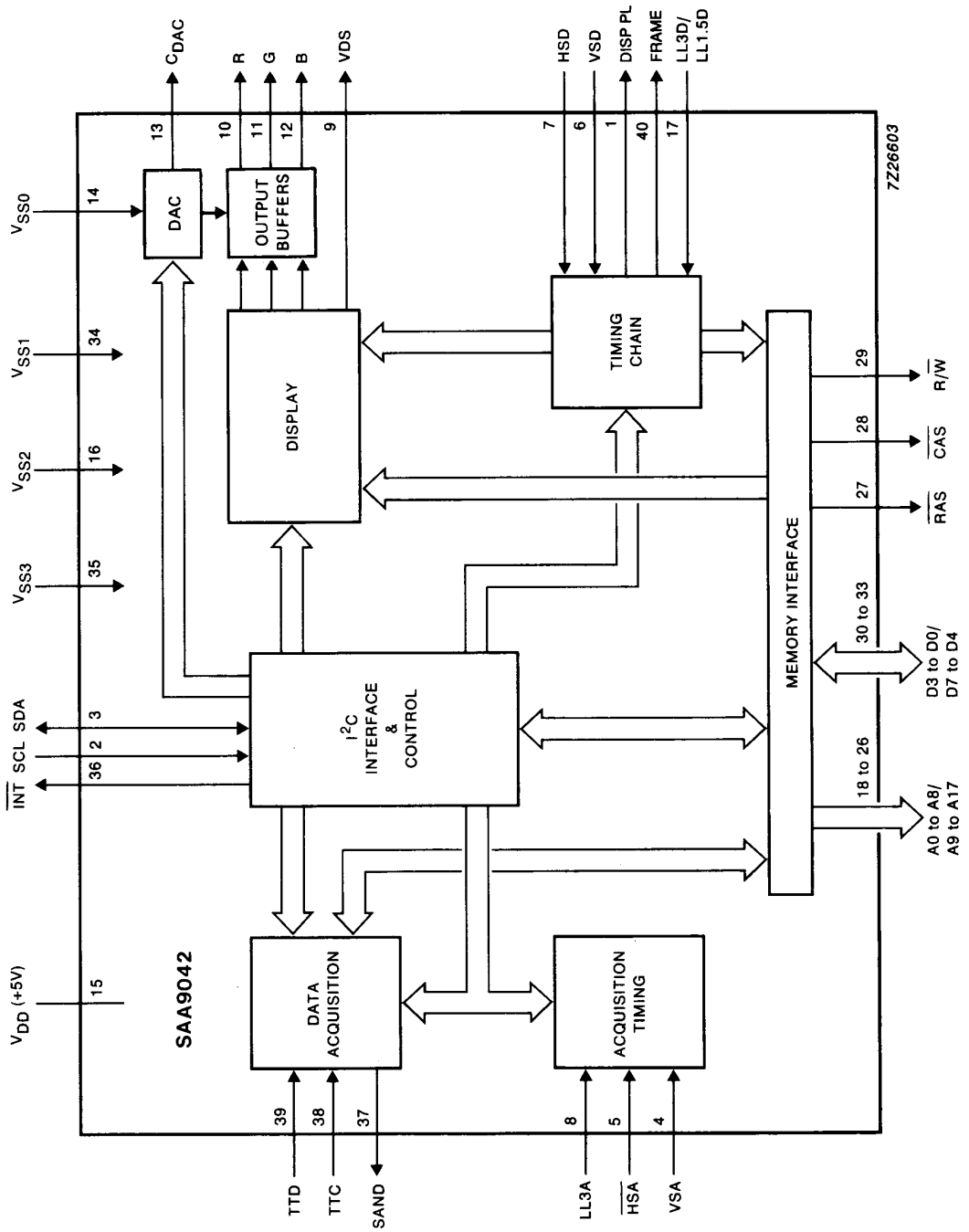


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

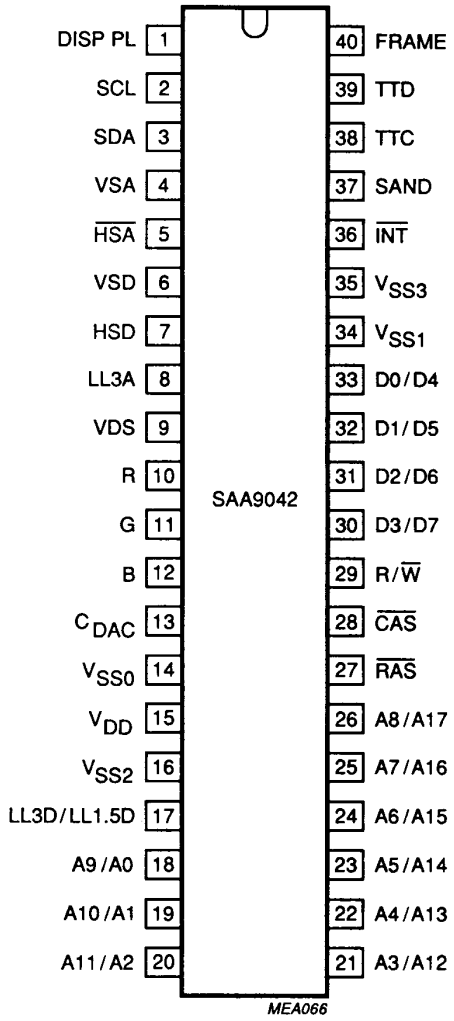


Fig.2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	DISP PL	**Display PL:** a programmable decode from the display-timing chain which can be used as a reference signal in an external PLL in scan-locked applications.
2	SCL	**Serial Clock:** input signal which is the I^2C-bus clock from the microcontroller.
3	SDA	**Serial Data:** is the I^2C-bus data line connected to the microcontroller. It is an input/output function with an open-drain output.
4	VSA	**Vertical Synchronization Acquisition:** vertical synchronization signal from the SAA9051 (VS) or SAA5191 (VCS), derived from the incoming video. This input enables field timing to be established in the acquisition section.
5	$\overline{HSA}$	**Horizontal Synchronization Acquisition:** horizontal synchronization signal derived from the incoming video e.g. burst gate pulse. This active LOW input enables line timing to be established in the acquisition section.
6	VSD	**Vertical Synchronization Display:** synchronization signal indicating the vertical position of the TV picture. This input allows field synchronization of the display section.
7	HSD	**Horizontal Synchronization Display:** synchronization signal indicating the horizontal position of the TV picture. This input allows line synchronization of the TV picture.
8	LL3A	**Line-Locked system clock:** 13.5 MHz system clock input for the acquisition section.
9	VDS	**Video/Data Switch:** push-pull active HIGH 3-state output which controls the switching between text (HIGH) and normal TV (LOW) picture for both normal text and superimposed displays.
10 11 12	R G B	**Red, Green, Blue:** analog 3-state outputs which contain video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
13	C_{DAC}	**DAC output:** DAC output level, requires an external decoupling capacitor not less than 1 μF.
14	V_{SS0}	**Ground:** ground connection for video outputs.
15	V_{DD}	**Power Supply:** + 5 V (typ.).
16	V_{SS2}	**Ground:** ground connection.
17	LL3D/ LL1.5D	**Line-Locked system clock:** 13.5 MHz or 27 MHz system clock input for the display, memory interface and control sections.
18 to 26	A0 to A8/ A9 to A17	**Address:** multiplexed address outputs for the external nibble-wide dynamic RAM (DRAM). With a 64-Kbit (16 K x 4) DRAM the address A8 pin is not used.
27	$\overline{RAS}$	**Row Address Strobe:** active LOW output for the external DRAM.
28	$\overline{CAS}$	**Column Address Strobe:** active LOW output for the external DRAM.
29	R/$\overline{W}$	**Read/Write:** active LOW write enable signal for the external DRAM.

pin no.	mnemonic	description
30 to 33	D3 to D0/ D4 to D7	**Data:** data inputs/outputs to and from the external nibble-wide DRAM.
34	V_{SS1}	**Ground:** ground connection.
35	V_{SS3}	**Ground:** ground connection.
36	$\overline{INT}$	**Interrupt:** open-drain active LOW output which provides an interrupt signal for a microprocessor indicating the arrival of a page or packet in any one of the acquisition channels, change in newsflash/subtitle status or power-on reset.
37	SAND	**Sandcastle:** 3-level output for the SAA5191 or SAA5236 representing the PL/$\overline{CBB}$ signal, derived from the acquisition timing chain.
38	TTC	**Teletext Clock:** input from the SAA5191 or SAA5236 supplied via an external coupling capacitor.
39	TTD	**Teletext Data:** input from the SAA5191 or SAA5236 supplied via an external coupling capacitor, internally clamped to V_{SS} for 4 to 8 μs of each line to maintain the correct DC level.
40	FRAME	**Frame:** output for de-interlacing ciruits. The signal is LOW for even fields and HIGH for odd fields when text but no picture is displayed. It is forced LOW when a TV picture is present.

DEVELOPMENT DATA

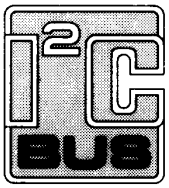
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.5	+ 6.5	V
DC input voltage	V_I	−0.5	V_{DD} + 0.5	V
DC input current	I_I	−20	+ 20	mA
DC output voltage	V_O	−0.5	V_{DD} + 0.5	V
DC output current	I_O	−20	+ 20	mA
DC V_{DD} current	I_{DD}	*	*	mA
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Electrostatic handling**	V_{es}	−1000	+ 1000	V

Notes to the ratings

1. All voltages are with respect to V_{SS}.
2. V_{SSO} is considered as an output.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Value to be fixed.

** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	note 1	V_{DD}	4.5	5.0	5.5	V
Supply current		I_{DD}	–	100	–	mA
Inputs	note 2					
TTD	note 3					
Input voltage						
(peak-to-peak value)		$V_{I(p-p)}$	2.0	–	5.0	V
External coupling capacitor		C_{ext}	–	22	50	nF
Input rise and fall times	notes 4 and 26	t_r, t_f	10	–	80	ns
Input data set-up time	note 5	$t_{SU;DAT}$	40	–	–	ns
Input data hold time	note 5	$t_{HD;DAT}$	40	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	7	–	pF
Clamp start time	note 6	t_{CLon}	3.5	4.0	4.5	μs
Clamp finish time	note 6	t_{CLoff}	7.5	8.0	8.5	μs
Clamp output current	note 7	I_{clamp}	1.0	–	–	mA
TTC	note 8					
Input voltage						
(peak-to-peak value)		$V_{I(p-p)}$	2.0	–	5.0	V
External coupling capacitor		C_{ext}	–	10	10	nF
Peak input current		I_{IM}	−10	–	+ 10	mA
Input peaks relative to 50% duty factor		$\pm V_{IM}$	0.2	–	3.5	V
Input rise and fall times	notes 4 and 26	t_r, t_f	10	–	80	ns
Input capacitance	note 26	C_I	–	7	–	pF
Input clamp voltage		V_{clamp}	1.2	1.4	1.6	V
Clock frequency						
625 line		f_{TTC}	–	6.9375	–	MHz
525 line		f_{TTC}	–	5.7272	–	MHz

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (continued)	note 2					
$\overline{HSA}$	note 9					
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
VSA						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH	note 27	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
LL3A (TTL mode)						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
LL3A cycle time	note 10	t_{CA}	69	74	80	ns
LL3A HIGH time		t_{CAH}	28	–	–	ns
LL3A LOW time		t_{CAL}	28	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−100	–	+ 100	μA
Input capacitance	note 26	C_I	–	–	10	pF
LL3A (AC mode)	13.5 MHz					
Mean voltage level	notes 25 and 26	V_{ACM}	−12	–	+ 12	V
AC voltage (peak-to-peak value)		$V_{AC(p-p)}$	1.0	–	3.0	V
Voltage HIGH w.r.t. mean		V_{ACH}	0.3	–	2.0	V
Voltage LOW w.r.t. mean		V_{ACL}	−2.0	–	−0.3	V
Input mark/space ratio w.r.t. mean t_{ACH}: t_{ACL} or t_{ACL} : t_{ACH}	note 28		30 : 70	–	70 : 30	
Series capacitor		C_S	47	100	220	pF
Input impedance	notes 24 and 26	Z_{ACI}	10	–	–	kΩ
SCL						
Input voltage LOW		V_{IL}	0	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD}	V
Input rise time	notes 4 and 26	t_r	–	–	1	μs
Input fall time	notes 11 and 26	t_f	–	–	300	ns
Input leakage current	note 12; V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance	note 26	C_I	–	–	7	pF
HSD						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	50	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	–10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
VSD						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	–10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
LL3D (TTL mode)						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	10	ns
LL3D cycle time						
13.5 MHz		t_{CA}	69	74	80	ns
27.0 MHz		t_{CA}	35	37	40	ns
LL3D HIGH time						
13.5 MHz		t_{CAH}	28	–	–	ns
27.0 MHz		t_{CAH}	14	–	–	ns
LL3D LOW time						
13.5 MHz		t_{CAL}	28	–	–	ns
27.0 MHz		t_{CAL}	14	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	–100	–	+ 100	μA
Input capacitance	note 26	C_I	–	–	10	pF
LL3D (AC mode)						
Mean voltage level	notes 25 and 26	V_{ACM}	–12	–	+ 12	V
AC voltage (peak-to-peak value)		$V_{AC(p-p)}$	1.0	–	3.0	V
Voltage HIGH w.r.t. mean		V_{ACH}	0.3	–	2.0	V
Voltage LOW w.r.t. mean		V_{ACL}	–2.0	–	–0.3	V
Input mark/space ratio w.r.t. mean t_{ACH}: t_{ACL} or t_{ACL} : t_{ACH}	note 28		30 : 70	–	70 : 30	
Series capacitor		C_S	47	100	220	pF
Input impedance	notes 24 and 26	Z_{ACI}	10	–	–	kΩ
Inputs/Outputs (I/O)	note 13					
SDA (open drain I/O)						
Input voltage LOW		V_{IL}	0	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD}	V

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CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
SDA (open drain I/O) (continued)						
Input rise time	notes 4 and 26	t_r	–	–	1	μs
Input fall time	notes 11 and 26	t_f	–	–	300	ns
Input leakage current	note 12; V_I = 0 to V_{DD}; (with output off)	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	0	–	0.4	V
Output fall time	notes 11 and 26	t_f	–	–	300	ns
Load capacitance		C_L	–	–	400	pF
D3 to D0						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input leakage current	note 12; V_I = 0 to V_{DD}; (with output off)	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V	note 26	t_r, t_f	–	–	10	ns
Load capacitance	note 21	C_L	–	–	100	pF
Outputs	note 13					
SAND	note 22					
Output voltage LOW	I_{OL} = 0.2 mA	V_{OL}	0	–	0.3	V
Output voltage INTERMEDIATE	$\pm I_{OI}$ = 30 μA	V_{OI}	1.3	–	2.7	V
Output voltage HIGH	I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 1.1 V	note 26	t_r, t_f	–	–	400	ns
Output rise time V_{OL} to V_{OH} between 2.9 V and 4.0 V	note 26	t_r, t_f	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 4.0 V and 0.4 V	note 26	t_r, t_f	–	–	50	ns
Load capacitance		C_L	–	–	30	pF

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{INT}$ (open-drain output)						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output leakage current	output off; V_{PU} = 0 to V_{DD}	I_{LO}	−10	–	+ 10	μA
Output fall time	notes 15 and 26	t_f	–	–	50	ns
Load capacitance		C_L	–	–	100	pF
A0 to A8						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V	note 26	t_r, t_f	–	–	10	ns
Load capacitance	note 23	C_L	–	–	100	pF
$\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V	note 26	t_r, t_f	–	–	10	ns
Load capacitance	note 23	C_L	–	–	100	pF
DISP PL, FRAME						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times	notes 16 and 26	t_r, t_f	–	–	200	ns
Load capacitance		C_L	–	–	200	pF
R, G, B (3-state)	note 29					
Output voltage LOW	note 17; I_{OL} = 2.0 mA	V_{OL}	V_{SS0}	–	V_{SS0}+0.2	V
Output voltage HIGH	note 18; I_{OH} = −2 mA	V_{OH}	–	*	–	V
Output rise and fall times between 0.6 V and 1.8 V	notes 4, 17 and 26	t_r, t_f	–	–	10	ns
Load capacitance		C_L	–	–	30	pF
Output capacitance	OFF state; note 26	C_{off}	–	–	10	pF
Output leakage current	OFF state; V_I = 0 to V_{DD}	I_{off}	−10	–	+ 10	μA
VDS (3-state)	note 29					
Output voltage LOW	I_{OL} = 1.0 mA	V_{OL}	0	–	0.2	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	1.1	–	2.8	V
Output rise and fall times	note 26	t_r, t_f	–	–	10	ns
Load capacitance		C_L	–	–	30	pF
Output leakage current	OFF state; V_I = 0 to V_{DD}	I_{off}	−10	–	+ 10	μA

* Adjustable over 0.5 to 1.5 V, via the I^2C-bus.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
TIMING						
I²C-bus	note 20					
SCL clock frequency		f_{SCL}	0	–	100	kHz
Input clock period						
HIGH time		t_{HIGH}	4	–	–	μs
LOW time		t_{LOW}	4	–	–	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop set-up time from clock HIGH		$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop		t_{BUF}	4	–	–	μs
Start hold time		$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock LOW-to-HIGH transition		$t_{SU;STA}$	4	–	–	μs
Memory interface	note 14					
Cycle time		t_{CY}	–	481	–	ns
Transition time		t_T	–	–	10	ns
$\overline{RAS}$ pulse width		$t_{W;RAS}$	120	–	–	ns
$\overline{RAS}$ pre-charge time		$t_{PC;RAS}$	90	–	–	ns
$\overline{CAS}$ hold time		$t_{HD;CAS}$	120	–	–	ns
Page mode cycle time		$t_{CY;PM}$	120	–	–	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time		t_d	25	–	–	ns
$\overline{CAS}$ pulse width		$t_{W;CAS}$	60	–	–	ns
$\overline{CAS}$ pre-charge time		$t_{PC;CAS}$	50	–	–	ns
Row address set-up time		$t_{SU;ROW}$	0	–	–	ns
Row address hold time		$t_{HD;ROW}$	15	–	–	ns
Column address set-up time		$t_{SU;COL}$	0	–	–	ns
Column address hold time		$t_{HD;COL}$	20	–	–	ns
Read command set-up time		$t_{SU;RD}$	0	–	–	ns
Read command hold time referenced to $\overline{CAS}$		$t_{HD;RDC}$	0	–	–	ns
Read command hold time referenced to $\overline{RAS}$		$t_{HD;RDR}$	10	–	–	ns
Access time from $\overline{CAS}$		$t_{ACC;CAS}$	–	–	60	ns

parameter	conditions	symbol	min.	typ.	max.	unit
Write command pulse width		$t_{W;WR}$	50	–	–	ns
Write command hold time		$t_{HD;WR}$	40	–	–	ns
Data-in set-up time		$t_{SU;DATI}$	0	–	–	ns
Data-in hold time		$t_{HD;DATI}$	40	–	–	ns
Access time from $\overline{RAS}$		$t_{ACC;RAS}$	–	–	120	ns
$\overline{RAS}$ hold time after $\overline{CAS}$		$t_{HD;RC}$	60	–	–	ns
$\overline{CAS}$ to $\overline{RAS}$ pre-charge time		$t_{PC;CR}$	20	–	–	ns
Column address hold time referenced to $\overline{RAS}$		$t_{HD;COLR}$	80	–	–	ns
Data-in hold time referenced to $\overline{RAS}$		$t_{HD;DATIR}$	100	–	–	ns

Notes to the characteristics

1. The rise time of V_{DD} from 0 to 4.5 V must be >150 ns to ensure that the internal power-on reset triggers. For this circuit to reset the chip, V_{DD} must be initially <1.0 V or fall to <1.0 V for at least 100 ns. Spikes on V_{DD} are tolerable provided that V_{DD} is not reduced to <2.5 V.
2. All inputs are protected against static charge under normal handling.
3. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor.
4. Rise and fall times are measured between 10% and 90% levels.
5. Teletext input data set-up and hold times are measured with respect to 50% duty factor level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant 2.0$ V, data stable 0 $\leqslant 0.8$ V.
6. Clamp times measured from the line sync reference point, assuming acquisition timing is set correctly.
7. Clamp transistor on, $V_{TTD} - V_{SSI} \leqslant 0.1$ V.
8. The TTC input has an internal clamping diode.
9. HSA is falling edge triggered.
10. Minimum and maximum cycles times are ± 7.1% of the typical value.
11. Fall time is measured between 3.0 V and 1.5 V.
12. Applies even when $V_{DD} = 0$ V.
13. All input/outputs and outputs are protected against static charge under normal handling.
14. For details of memory interface timings to and from external DRAM see Fig. 5 and Fig. 6.

DEVELOPMENT DATA

Notes to the characteristics (continued)

15. Output fall time measured between 4.0 V and 1.0 V levels with a 3.3 kΩ load to 5.0 V.
16. Output rise and fall times measured between 0.8 V and 2.0 V levels.
17. Measured with $V_{SS0} = V_{SS}$ and output voltage (C_{DAC}) = 1.5 V.
18. Measured with $V_{SS0} = V_{SS}$ and output voltage (C_{DAC}) = 0.5 V to 1.5 V.
19. Skew delay time measured at 0.7 V levels.
20. For details of I^2C-bus timings see Fig. 3; timings are referred to V_{IH} = 3.0 V and V_{IL} = 1.5 V.
21. Load capacitance measured with two DRAM data inputs; 50 pF maximum.
22. A current of 1 μA flows out of the SAA5191 or SAA5236 while its SAND input is in the range of 1 V to 3.5 V.
23. Load capacitance measured with eight DRAM data inputs; 80 pF maximum.
24. Through a 200 pF capacitor with a 13.5 MHz sinewave.
25. To be applied via the series capacitor only.
26. This specification point is included because of its importance to the application environment; it is not however guaranteed.
27. When connected to the SAA5191, it is acceptable for the clock frequency to initially attain ⩽ 15 MHz in order to achieve synchronism.
28. When connected to the SAA5191, it is acceptable for the input voltage to attain V_{DD} + 0.9 V. The input current must be restricted as specified in the RATINGS.
29. These outputs can be made 3-state via the I^2C-bus.

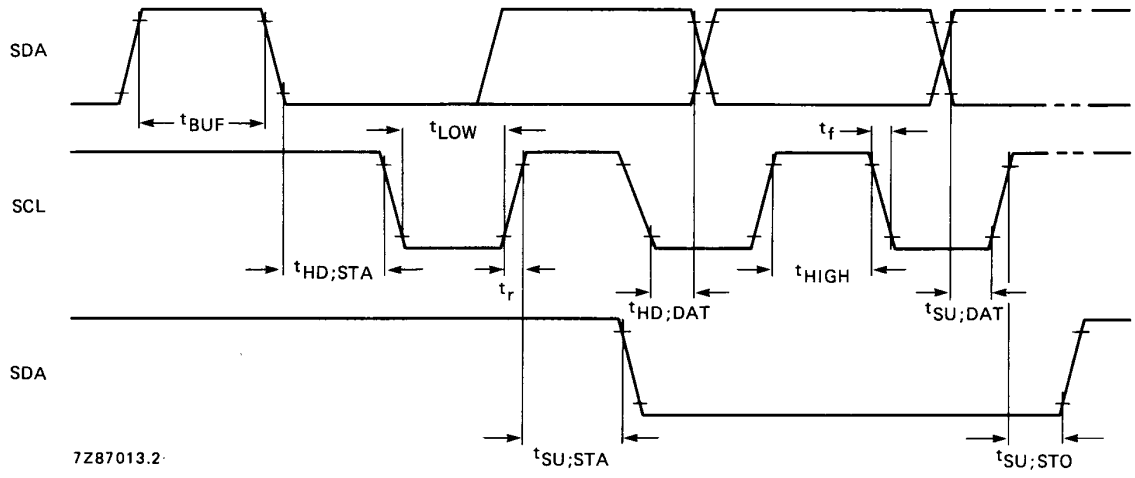


Fig.3 I^2C-bus timing.

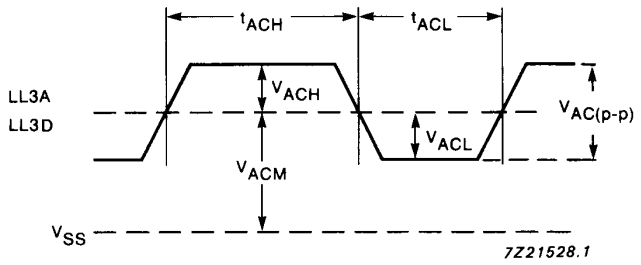


Fig.4 Line-Locked system clock LL3A and LL3D timing diagram.

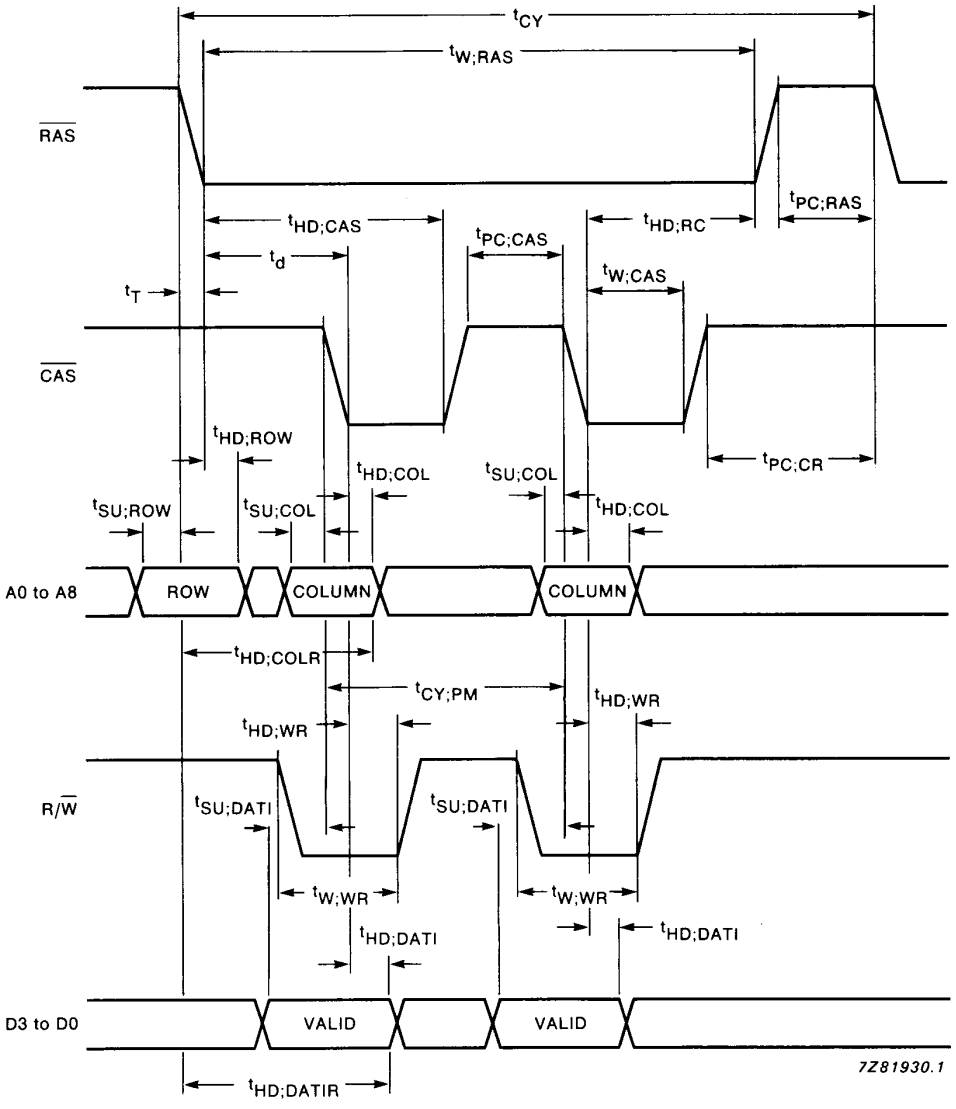


Fig.5 Memory interface timing for write cycle to external DRAM.

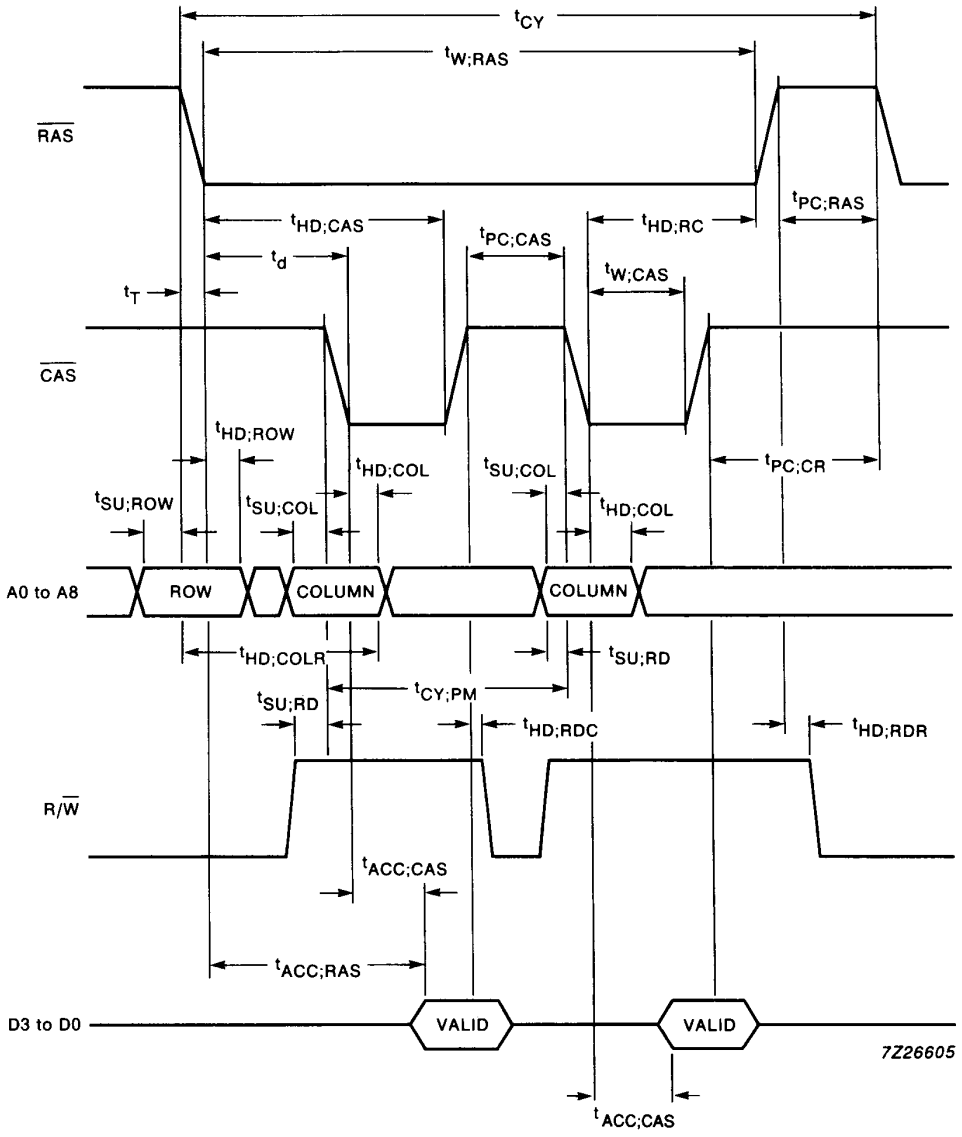


Fig.6 Memory interface timing for read cycle from external DRAM.

DEVELOPMENT DATA

BITS b_4 b_3 b_2 b_1	row	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	10	11	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black			0		é	P	ù		p		$	ï		0	$	$	¤	Á
0 0 0 1	1	alpha-numerics red	graphics red	!		1		A	Q	a		q		£	é	!	1	#	ç	#	À
0 0 1 0	2	alpha-numerics green	graphics green	"		2		B	R	b		r		@	à	"	2	§	i	É	È
0 0 1 1	3	alpha-numerics yellow	graphics yellow	£		3		C	S	c		s		←	ë	ò	3	Ä	á	Ä	ſ
0 1 0 0	4	alpha-numerics blue	graphics blue	$		4		D	T	d		t		½	ê	ì	4	Ö	é	Ö	Ï
0 1 0 1	5	alpha-numerics magenta	graphics magenta	%		5		E	U	e		u		→	ù	%	5	Ü	í	Å	Ó
0 1 1 0	6	alpha-numerics cyan	graphics cyan	&		6		F	V	f		v		↑	î	&	6	^	ó	Ü	Ò
0 1 1 1	7	alpha-numerics white**	graphics white	'		7		G	W	g		w		#	#	'	7	_	ú	_	Ú
1 0 0 0	8	flash	conceal display	(		8		H	X	h		x		—	è	(	8	°	¿	é	æ
1 0 0 1	9	steady**	contiguous graphics**	)		9		I	Y	i		y		¼	â	)	9	ä	ü	ä	Æ
1 0 1 0	10	end box**	separated graphics	*		:		J	Z	j		z		‖	ô	*	:	ö	ñ	ö	ð
1 0 1 1	11	start box	ESC*	+		;		K	°	k		à		¾	û	+	;	ü	è	å	Đ
1 1 0 0	12	normal height**	black background**	,		<		L	ç	l		ò		÷	ç	,	<	ß	à	ü	ø
1 1 0 1	13	double height	new background	−		=		M	→	m		è				−	=	ä	Ä	¤	Ø
1 1 1 0	14	double width	hold graphics	.		>		N	↑	n		ì				.	>	ö	Ö	¤	þ
1 1 1 1	15	double size	release graphics**	/		?		O	#	o						/	?	·	ç	Ñ	Þ

7Z26604

*These control characters are reserved for compatability with other data codes.
**These control characters are presumed before each row begins.

Fig.7 SAA9042A West European character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.2

(1) Where PHCB are the page Header Control Bits.
Other combinations of PHCB default to English.

Fig.8 SAA9042A West European national option sets.

DEVELOPMENT DATA

APPLICATION INFORMATION

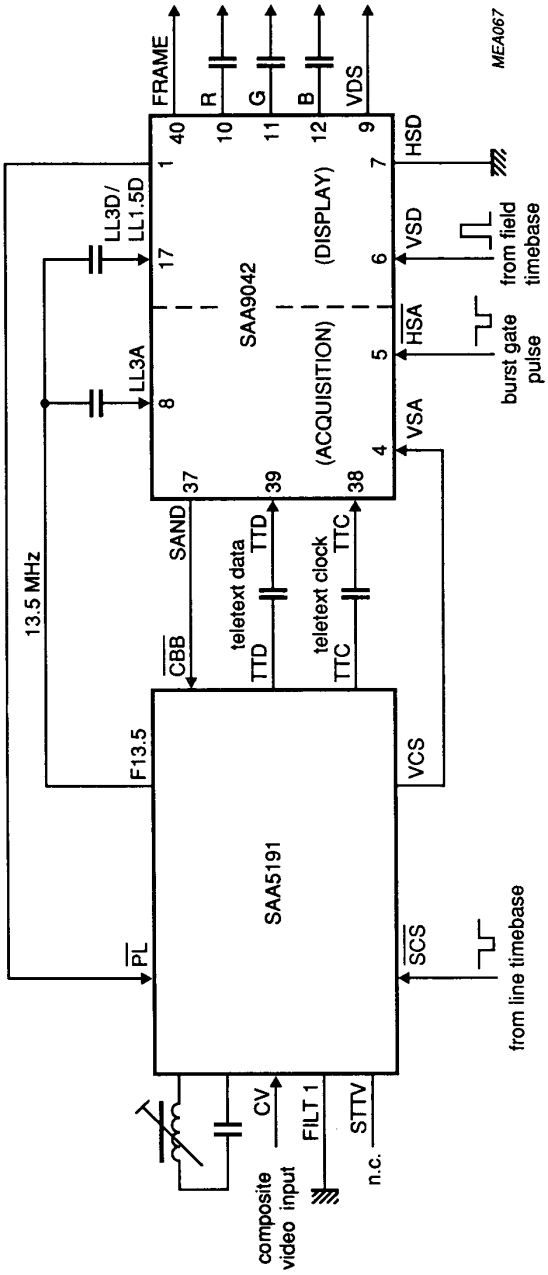


Fig.9 Synchronization of SAA9042 in analog TV (slave sync mode).

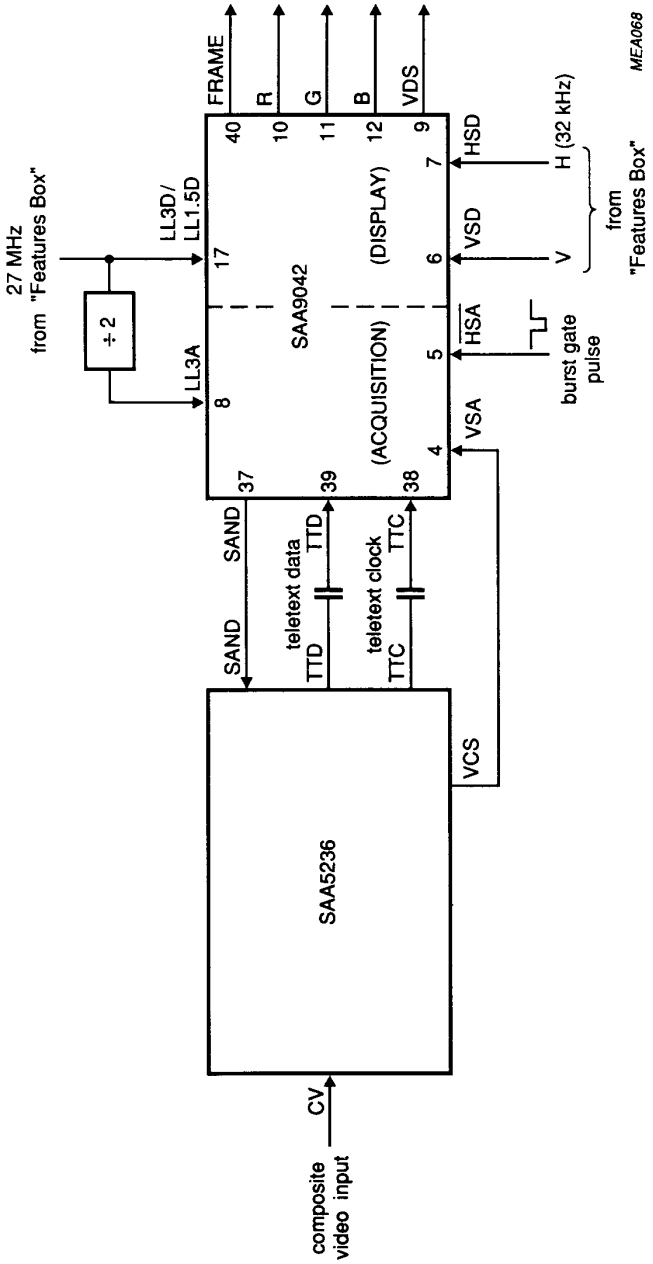


Fig.10 Synchronization of SAA9042 in analog TV with 2 x H features.

APPLICATION INFORMATION (continued)

DEVELOPMENT DATA

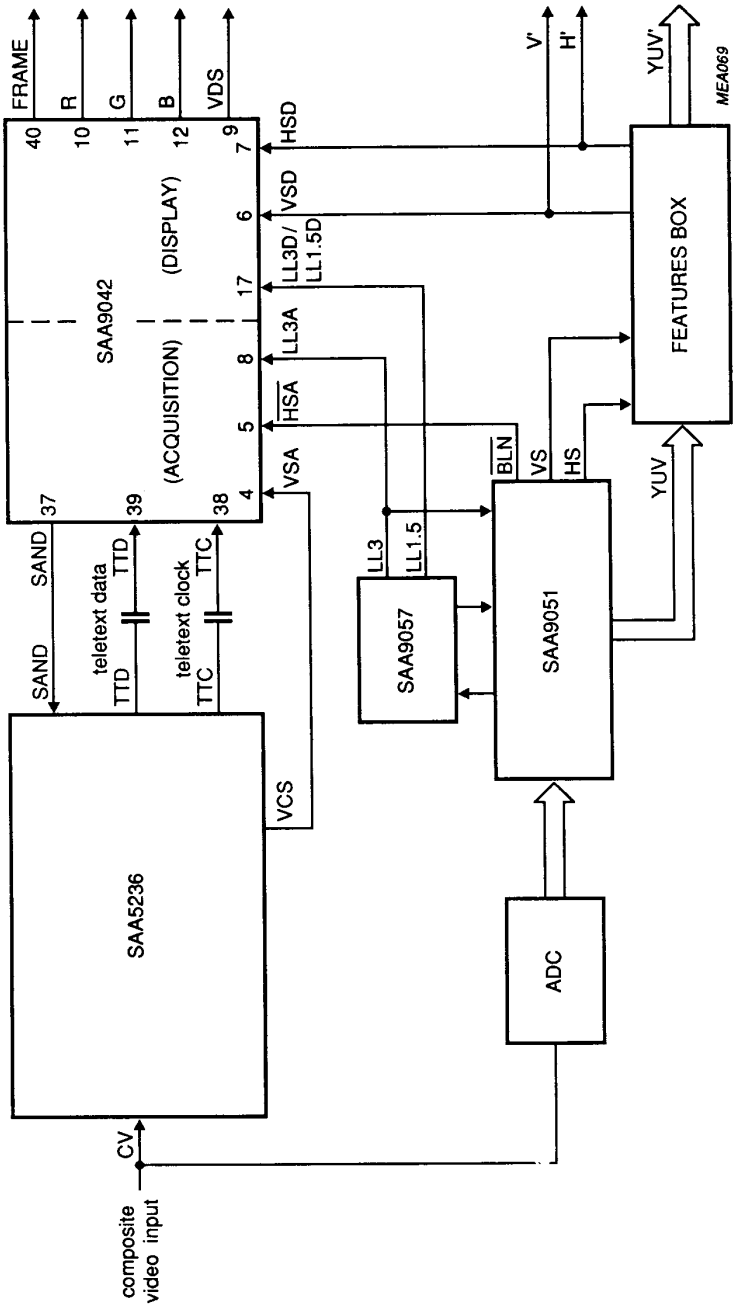
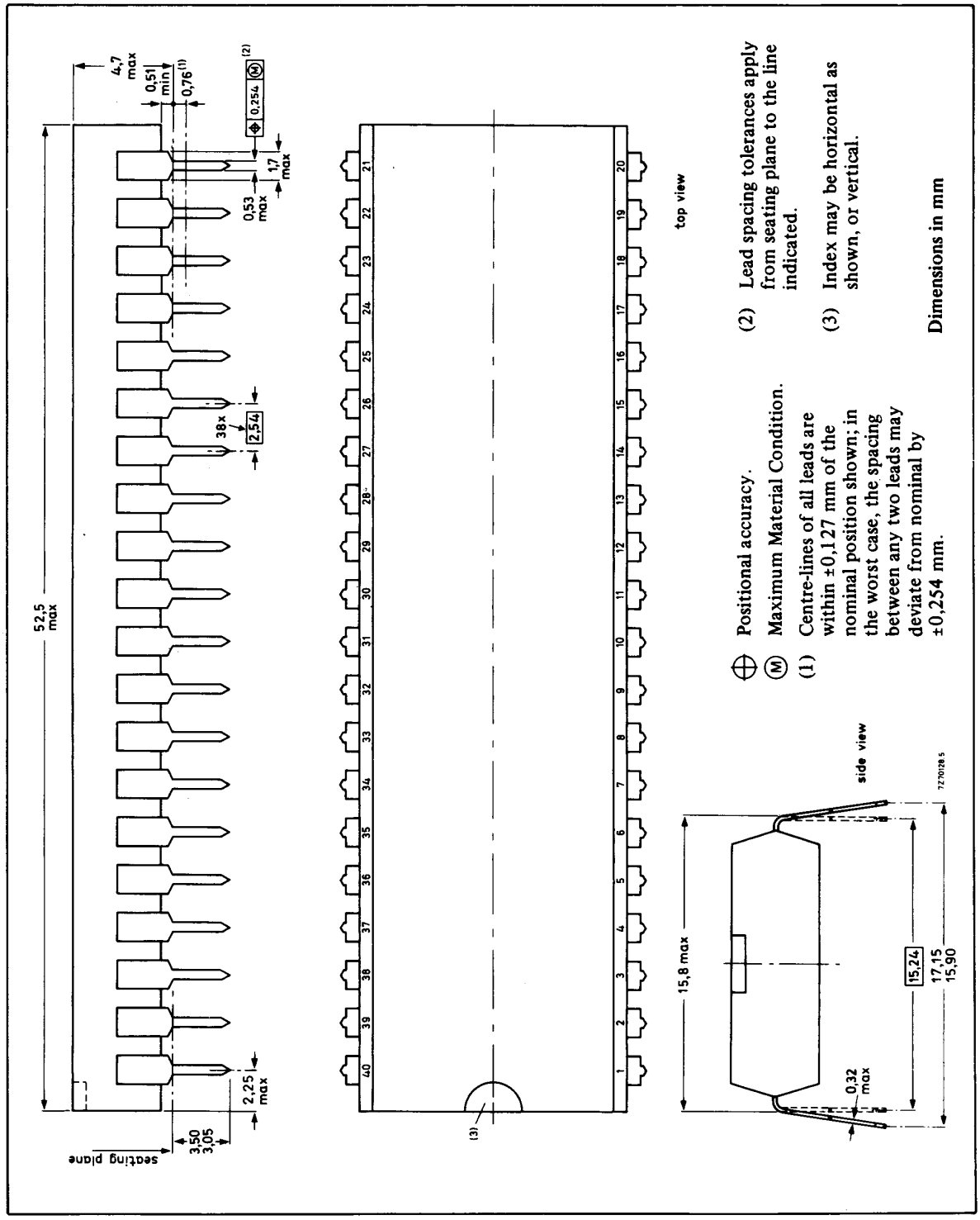


Fig.11 Synchronization of SAA9042 in digital TV with 2 x H features.

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.