S6B0796

240 SEG / COM DRIVER FOR STN LCD

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Ver. 1.0

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S6B0796 Specification Revision History		
Version	**Content**	**Date**
0.0	● Original	June.1999
0.1	● p6, p16 revision	August.1999
1.0	● p4 Introduction revision.	January. 2000

CONTENTS

INTRODUCTION

The S6B0796 is a 240-outputs segment/common driver LSI for graphic dot-matrix liquid crystal display systems. It is fabricated by low power CMOS high voltage process technology. This device consists of 240-bits bi-directional shift register, 240-bits data latch and 240-bits driver. In case of segment mode, the data input is selected 4bit parallel input mode and 8bit parallel input mode by a mode (MD) pin. In case of common mode, data input/output pins are bi-directional, four data shift directions are pin-selectable.

FEATURES

Both Segment Mode and Common Mode

- Supply voltage for LC driver: +15.0 to +32.0V
- Number of LC driver outputs: 240
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.4V to +5.5V
- CMOS silicon gate process (P-type Silicon Substrate)
- Package: 268-pin TCP (Tape Carrier Package) or Gold bumped chip

Segment Mode

- Shift clock frequency: 20MHz (Max) (Vdd=+5V±10%)
  12MHz (Max) (Vdd=+2.4V to +4.5V)
- Adopts a data bus system
- 4- / 8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select, causes the internal clock to be stopped by automatically counting 240 of input data
- Line latch circuit reset function when DISPOFFB active

Common Mode

- Shift clock frequency: 4.0MHz (Max) (vdd=+2.4V to +5.5V)
- Built-in 240-bits bi-directional shift register (divisible into 120-bits ×2)
- Available in a single mode (240-bits shift register)
  or in a dual mode (120-bits shift register ×2)
- Shift register circuit reset function when DISPOFFB active

BLOCK DIAGRAM

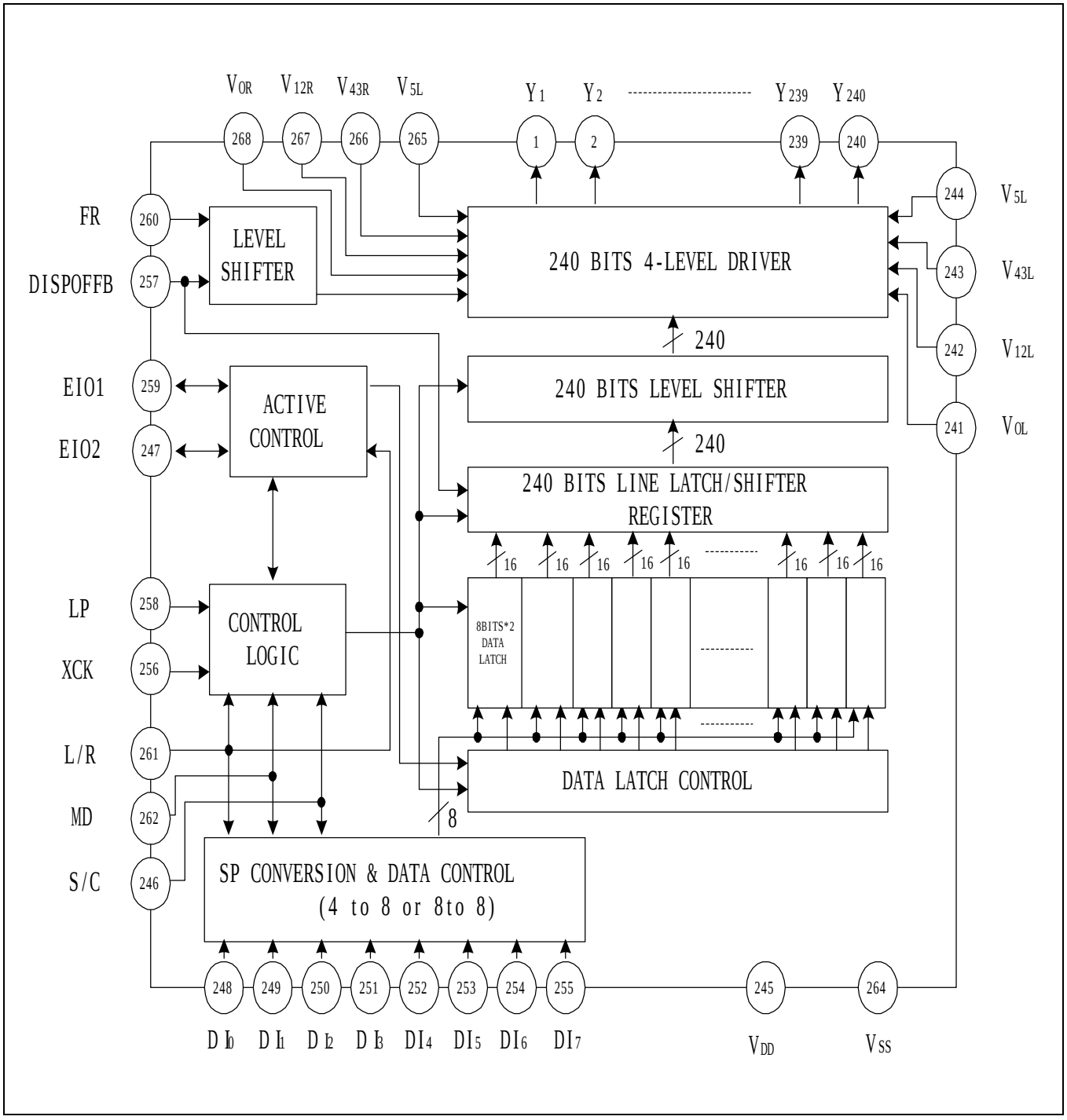


Figure 1. Block Diagram

PAD CONFIGURATION

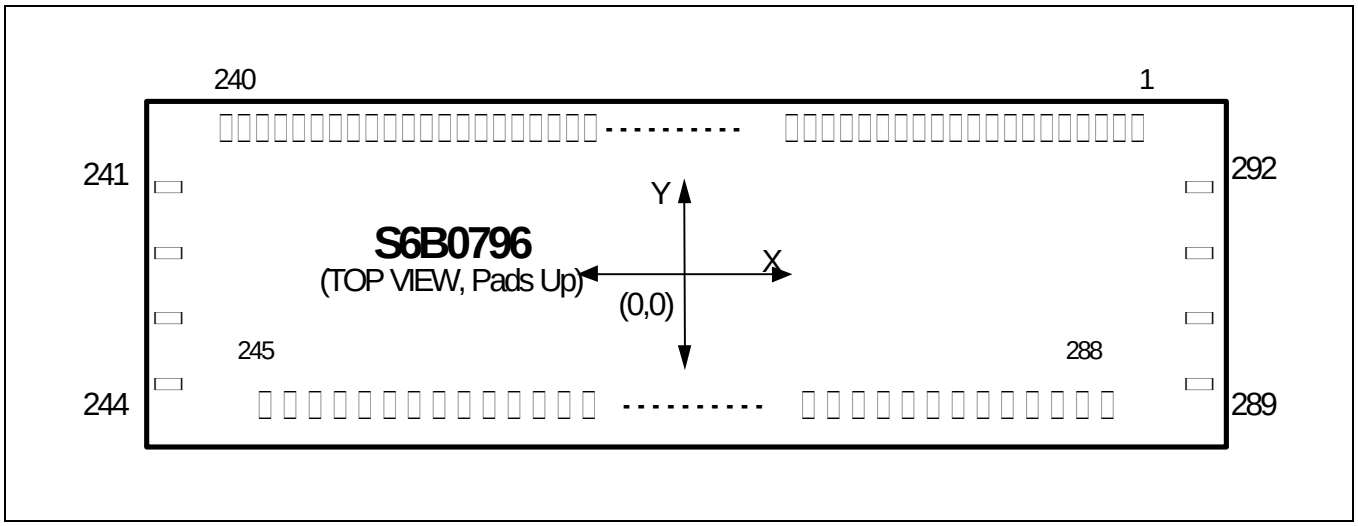


Figure 2. S6B0796 Chip Configuration

Table 1. S6B0796 Pad Dimensions

Item	Pad NO.	Size		Unit
		X	Y	
Chip size	-	16200	1100	mm
Pad pitch	1 to 240 241 to 292	65 (Min.) 260 (Min.)		
Bumped pad size	1 to 240	43	108	
	241 to 244 289 to 292	76	73	
	245 to 288	58	76	
Bumped pad height	1 to 292	14 (Typ.)		

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: ㎜]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	Y1	7767.5	395	51	Y51	4517.5	395	101	Y101	1267.5	395
2	Y2	7702.5	395	52	Y52	4452.5	395	102	Y102	1202.5	395
3	Y3	7637.5	395	53	Y53	4387.5	395	103	Y103	1137.5	395
4	Y4	7572.5	395	54	Y54	4322.5	395	104	Y104	1072.5	395
5	Y5	7507.5	395	55	Y55	4257.5	395	105	Y105	1007.5	395
6	Y6	7442.5	395	56	Y56	4192.5	395	106	Y106	942.5	395
7	Y7	7377.5	395	57	Y57	4127.5	395	107	Y107	877.5	395
8	Y8	7312.5	395	58	Y58	4062.5	395	108	Y108	812.5	395
9	Y9	7247.5	395	59	Y59	3997.5	395	109	Y109	747.5	395
10	Y10	7182.5	395	60	Y60	3932.5	395	110	Y110	682.5	395
11	Y11	7117.5	395	61	Y61	3867.5	395	111	Y111	617.5	395
12	Y12	7052.5	395	62	Y62	3802.5	395	112	Y112	552.5	395
13	Y13	6987.5	395	63	Y63	3737.5	395	113	Y113	487.5	395
14	Y14	6922.5	395	64	Y64	3672.5	395	114	Y114	422.5	395
15	Y15	6857.5	395	65	Y65	3607.5	395	115	Y115	357.5	395
16	Y16	6792.5	395	66	Y66	3542.5	395	116	Y116	292.5	395
17	Y17	6727.5	395	67	Y67	3477.5	395	117	Y117	227.5	395
18	Y18	6662.5	395	68	Y68	3412.5	395	118	Y118	162.5	395
19	Y19	6597.5	395	69	Y69	3347.5	395	119	Y119	97.5	395
20	Y20	6532.5	395	70	Y70	3282.5	395	120	Y120	32.5	395
21	Y21	6467.5	395	71	Y71	3217.5	395	121	Y121	-32.5	395
22	Y22	6402.5	395	72	Y72	3152.5	395	122	Y122	-97.5	395
23	Y23	6337.5	395	73	Y73	3087.5	395	123	Y123	-162.5	395
24	Y24	6272.5	395	74	Y74	3022.5	395	124	Y124	-227.5	395
25	Y25	6207.5	395	75	Y75	2957.5	395	125	Y125	-292.5	395
26	Y26	6142.5	395	76	Y76	2892.5	395	126	Y126	-357.5	395
27	Y27	6077.5	395	77	Y77	2827.5	395	127	Y127	-422.5	395
28	Y28	6012.5	395	78	Y78	2762.5	395	128	Y128	-487.5	395
29	Y29	5947.5	395	79	Y79	2697.5	395	129	Y129	-552.5	395
30	Y30	5882.5	395	80	Y80	2632.5	395	130	Y130	-617.5	395
31	Y31	5817.5	395	81	Y81	2567.5	395	131	Y131	-682.5	395
32	Y32	5752.5	395	82	Y82	2502.5	395	132	Y132	-747.5	395
33	Y33	5687.5	395	83	Y83	2437.5	395	133	Y133	-812.5	395
34	Y34	5622.5	395	84	Y84	2372.5	395	134	Y134	-877.5	395
35	Y35	5557.5	395	85	Y85	2307.5	395	135	Y135	-942.5	395
36	Y36	5492.5	395	86	Y86	2242.5	395	136	Y136	-1007.5	395
37	Y37	5427.5	395	87	Y87	2177.5	395	137	Y137	-1072.5	395
38	Y38	5362.5	395	88	Y88	2112.5	395	138	Y138	-1137.5	395
39	Y39	5297.5	395	89	Y89	2047.5	395	139	Y139	-1202.5	395
40	Y40	5232.5	395	90	Y90	1982.5	395	140	Y140	-1267.5	395
41	Y41	5167.5	395	91	Y91	1917.5	395	141	Y141	-1332.5	395
42	Y42	5102.5	395	92	Y92	1852.5	395	142	Y142	-1397.5	395
43	Y43	5037.5	395	93	Y93	1787.5	395	143	Y143	-1462.5	395
44	Y44	4972.5	395	94	Y94	1722.5	395	144	Y144	-1527.5	395
45	Y45	4907.5	395	95	Y95	1657.5	395	145	Y145	-1592.5	395
46	Y46	4842.5	395	96	Y96	1592.5	395	146	Y146	-1657.5	395
47	Y47	4777.5	395	97	Y97	1527.5	395	147	Y147	-1722.5	395
48	Y48	4712.5	395	98	Y98	1462.5	395	148	Y148	-1787.5	395
49	Y49	4647.5	395	99	Y99	1397.5	395	149	Y149	-1852.5	395
50	Y50	4582.5	395	100	Y100	1332.5	395	150	Y150	-1917.5	395

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
151	Y151	-1982.5	395	201	Y201	-5232.5	395	251	DUMMY	-5900	-419
152	Y152	-2047.5	395	202	Y202	-5297.5	395	252	VDD	-5640	-419
153	Y153	-2112.5	395	203	Y203	-5362.5	395	253	VDD	-5380	-419
154	Y154	-2177.5	395	204	Y204	-5427.5	395	254	VDD	-5120	-419
155	Y155	-2242.5	395	205	Y205	-5492.5	395	255	VDD	-4860	-419
156	Y156	-2307.5	395	206	Y206	-5557.5	395	256	VDD	-4600	-419
157	Y157	-2372.5	395	207	Y207	-5622.5	395	257	SC	-4340	-419
158	Y158	-2437.5	395	208	Y208	-5687.5	395	258	EIO2	-4080	-419
159	Y159	-2502.5	395	209	Y209	-5752.5	395	259	DI0	-3820	-419
160	Y160	-2567.5	395	210	Y210	-5817.5	395	260	DI1	-3560	-419
161	Y161	-2632.5	395	211	Y211	-5882.5	395	261	DI2	-3300	-419
162	Y162	-2697.5	395	212	Y212	-5947.5	395	262	DI3	-3040	-419
163	Y163	-2762.5	395	213	Y213	-6012.5	395	263	DI4	-2780	-419
164	Y164	-2827.5	395	214	Y214	-6077.5	395	264	DI5	-2520	-419
165	Y165	-2892.5	395	215	Y215	-6142.5	395	265	DI6	-2260	-419
166	Y166	-2957.5	395	216	Y216	-6207.5	395	266	DI7	-2000	-419
167	Y167	-3022.5	395	217	Y217	-6272.5	395	267	XCK	1770	-419
168	Y168	-3087.5	395	218	Y218	-6337.5	395	268	DISPOFFB	2030	-419
169	Y169	-3152.5	395	219	Y219	-6402.5	395	269	LP	2290	-419
170	Y170	-3217.5	395	220	Y220	-6467.5	395	270	EIO1	2550	-419
171	Y171	-3282.5	395	221	Y221	-6532.5	395	271	FR	2810	-419
172	Y172	-3347.5	395	222	Y222	-6597.5	395	272	LR	3070	-419
173	Y173	-3412.5	395	223	Y223	-6662.5	395	273	MD	3330	-419
174	Y174	-3477.5	395	224	Y224	-6727.5	395	274	NC	3590	-419
175	Y175	-3542.5	395	225	Y225	-6792.5	395	275	VSS	3850	-419
176	Y176	-3607.5	395	226	Y226	-6857.5	395	276	VSS	4110	-419
177	Y177	-3672.5	395	227	Y227	-6922.5	395	277	VSS	4370	-419
178	Y178	-3737.5	395	228	Y228	-6987.5	395	278	VSS	4630	-419
179	Y179	-3802.5	395	229	Y229	-7052.5	395	279	VSS	4890	-419
180	Y180	-3867.5	395	230	Y230	-7117.5	395	280	VSS	5150	-419
181	Y181	-3932.5	395	231	Y231	-7182.5	395	281	DUMMY	5410	-419
182	Y182	-3997.5	395	232	Y232	-7247.5	395	282	DUMMY	5670	-419
183	Y183	-4062.5	395	233	Y233	-7312.5	395	283	DUMMY	5930	-419
184	Y184	-4127.5	395	234	Y234	-7377.5	395	284	DUMMY	6190	-419
185	Y185	-4192.5	395	235	Y235	-7442.5	395	285	DUMMY	6450	-419
186	Y186	-4257.5	395	236	Y236	-7507.5	395	286	DUMMY	6710	-419
187	Y187	-4322.5	395	237	Y237	-7572.5	395	287	DUMMY	6970	-419
188	Y188	-4387.5	395	238	Y238	-7637.5	395	288	DUMMY	7230	-419
189	Y189	-4452.5	395	239	Y239	-7702.5	395	289	V5R	7969	-348.5
190	Y190	-4517.5	395	240	Y240	-7767.5	395	290	V43R	7969	-127.5
191	Y191	-4582.5	395	241	V0L	-7969	344.5	291	V12R	7969	93.5
192	Y192	-4647.5	395	242	V12L	-7969	93.5	292	V0R	7969	344.5
193	Y193	-4712.5	395	243	V43L	-7969	-127.5				
194	Y194	-4777.5	395	244	V5L	-7969	-348.5				
195	Y195	-4842.5	395	245	DUMMY	-7460	-419				
196	Y196	-4907.5	395	246	DUMMY	-7200	-419				
197	Y197	-4972.5	395	247	DUMMY	-6940	-419				
198	Y198	-5037.5	395	248	DUMMY	-6680	-419				
199	Y199	-5102.5	395	249	DUMMY	-6420	-419				
200	Y200	-5167.5	395	250	DUMMY	-6160	-419				

PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1 to 240	Y_1 – Y_{240}	O	LC driver output
241, 292	V_{0L}, V_{0R}	-	Power supply for LC driver
242, 291	V_{12L}, V_{12R}	-	Power supply for LC driver
243, 290	V_{43L}, V_{43R}	-	Power supply for LC driver
244, 289	V_{5L}, V_{5R}	-	Power supply for LC driver
272	L/R	I	Display data shift direction selection
252 to 256	V_{DD}	-	Power supply for logic system(+2.4 to +5.5V)
257	S/C	I	Segment mode/common mode selection
258	EIO_2	I/O	Input/output for chip select or data of shift register
259 to 265	DI_0 – DI_6	I	Display data input for segment mode
266	DI_7	I	Display data input for segment mode/Dual mode data input
267	XCK	I	Display data shift clock input for segment mode
268	DISPOFFB	I	Control input for deselect output level
269	LP	I	Latch pulse input/shift clock input for shift register
270	EIO_1	I/O	Input/output for chip select or data of shift register
271	FR	I	AC-converting signal input for LC driver waveform
273	MD	I	Mode selection input
275 to 280	V_{SS}	-	Ground(0V)

Table 3 Pin Description

FUNCTIONAL DESCRIPTION

BLOCK FUNCTION

. Active Control
In case of segment mode, controls the selection or deselection of the chip. Following a LP signal, and after the chip select signal is input, a select signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected. In case of common mode, controls the input/output data of bidirectional pins.

. SP Conversion & Data Control
In case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bits parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

. Data Latch Control
In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.

. Data Latch
In case of segment mode, latches the data on the data bus. The latched state of each LC driver output pin is controlled by the control logic and the data latch control, 240 bits of data are read in 30 sets of 8 bits.

. Line Latch / Shift Register
In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block. In case of common mode, shifts data from the data input pin on the falling edge of the LP signal.

. Level Shifter
The logic voltage signal is level-shifted to the LC driver voltage level, and output to the driver block.

. 4-level Driver
Driver the LC driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_5) based on the S/C, FR and DISPOFFB signals.

. Control logic
Controls the operation of each block. In case of segment mode, when a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 240 bits of data are read in, and the chip is deselected. In case of common mode, controls the direction of data shift.

PIN FUNCTION

Segment mode

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.4 to +5.5V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{12R} , V_{12L} V_{43R} , V_{43L} V_{5R} , V_{5L}	Power supply pin for LC driver voltage bias. . Normally, the bias voltage used is set by a resistor divider. . Ensure that voltage are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$. . To further reduce the difference between the output waveforms of LC driver output pins Y_1 and Y_{160}, externally connect V_{iR} and V_{iL} (I = 0, 12, 43, 5)
DI_0 – DI_7	Input pin for display data . In 4-bit parallel input mode, input data into the 4 pins DI_0 – DI_3. Connect DI_4 – DI_7 to V_{SS} or V_{DD}. . In 8-bit parallel input mode, input data into the 8 pins DI_0 – DI_7.
XCK	Clock input pin for taking display data . Data is read on the falling edge of the clock pulse.
LP	Latch pulse input pin for display data . Data is latched on the falling edge of the clock pulse.
L/R	Direction selection pin for reading display data . When set to V_{SS} level “L”, data is read sequentially from Y_{240} to Y_1. . When set to V_{DD} level H”, data is read sequentially from Y_1 to Y_{240}.
DISPOFFB	Control input pin for output deselect level . The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. . When set to V_{SS} level “L”, the LC drive output pins (Y_1 - Y_{240}) are set to level V_5. . While set to “L”, the contents of the line latch are reset, but read the display data in the data latch regardless of condition of DISPOFFB. When the DISPOFFB function is canceled, the driver outputs deselect level (V_{12} or V_{43}), then outputs the contents of the data latch on the next. Falling edge of the LP. That time, if DISPOFFB removal time can not keep regulation what is shown AC characteristics (page 21), can not output the reading data correctly.

FR	AC signal input for LC driving waveform . The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. . Normally, inputs a frame inversion signal. . The LC driver output pin's output voltage level can be set using the line latch output signal and the FR signal. Table of truth values is shown in table 4.
MD	Mode selection pin . When set to V_{SS} level "L", 8-bit parallel input mode is set. . When set to V_{DD} level "H", 4-bit parallel input mode is set. . The relationship between the display data and driver output pins is shown in table 5.
S/C	Segment mode/common mode selection pin . When set to V_{DD} level 'H", segment mode is set.
EIO_1 **EIO_2**	Input / output pin for chip selection . When L/R input is at V_{SS} level 'L", EIO_1 is set for output, and EIO_2 is set for input. . When L/R input is at V_{DD} level 'H", EIO_1 is set for input, and EIO_2 is set for output. . During output. set to "H" while LP*XCLKB is 'H" and after 240-bits of data have been read, set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". . During input, after the LP signal is input, the chip is selected while EI is set to "L". After 240-bits of data have been read, the chip is deselected.
$Y_1 – Y_{240}$	LC driver output pins . Corresponding directly to each bit of the data latch, one level(V_0, V_{12}, V_{43}, or V_5) is selected and output. Table of truth values is shown in table 4.

Common Mode

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.4 to +5.5V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{12R} , V_{12L} V_{43R} , V_{43L} V_{5R} , V_{5L}	Power supply pin for LC driver voltage bias. . Normally, the bias voltage used is set by a resistor divider. . Ensure that voltage are set such that $V_{SS}<V_{43}<V_{12}<V_0$. . To further reduce the difference between the output waveforms of LC driver output pins Y_1 and Y_{240}, externally connect V_{iR} and V_{iL}(i=0, 12, 43, 5)
EIO_1	Bidirectional shift register shift data input/output pin . Output pin when L/R is at V_{SS} level “L”, input pin when L/R is at V_{DD} level “H”. . When EIO1 is used as input pin, it will be pull-down. . When EIO1 is used as output pin, it won’t be pull-down.
EIO_2	Bidirectional shift register shift data input/output pin . Input pin when L/R is at V_{SS} level “L”, output pin when L/R is at V_{DD} level “H”. . When EIO_2 is used as input pin, it will be pull-down. . When EIO_2 is used as output pin, it won’t be pull-down.
LP	Bidirectional shift register shift clock pulse input pin . Data is shifted on the falling edge of the clock pulse.
L/R	Bidirectional shift register shift direction selection pin . Data is shifted from Y_{240} to Y_1 when set to V_{SS} to level “L”, and data is shifted from Y_1 to Y_{240} when set to V_{DD} level “H”.

DISPOFFB	Control input pin for output deselect level . The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. . When set to V_{SS} level "L", the LC drive output pins(Y_1-Y_{240}) are set to level V_5. . While set to "L", the contents of the shift resister are reset not reading data. When the DISPOFFB function is canceled, the driver outputs deselect Level(V_{12} or V_{43}), and the shift data is reading on the falling edge of the LP. That time, if DISPOFFB removal time can not keep regulation what is shown AC characteristics (page 26), the shift data is not reading correctly.
FR	AC signal input for LC driving waveform . The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. . Normally, input a frame inversion signal. . The LC driver output pin's output voltage level can be set using the shift register output signal and the FR signal. Table of truth values is shown in table 4.
MD	Mode selection pin . When set to V_{SS} level "L", Single mode operation is selected, when set to V_{DD} level "H", Dual mode operation is selected.
DI_7	Dual Mode data input pin . According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used as Dual mode, DI_7 will be pull-down. When the chip is used as Single mode, DI_7 won't be pull-down.
S/C	Segment mode/common mode selection pin . When set to V_{SS} level 'L", common mode is set.
DI_0 – DI_6	Not used . Connect DI_0 – DI_6 to V_{SS} or V_{DD}. Avoiding floating.
XCK	Not used . XCK is pull-down in common mode, so connect to V_{SS} or open.
Y_1 – Y_{240}	LC driver output pins . Corresponding directly to each bit of the shift register, one level(V_0, V_{12}, V_{43}, or V_5) is selected and output. Table of truth values is shown in table 4.

FUNCTIONAL OPERATIONS

TRUTH TABLE (Table 4)

Segment Mode

FR	Latch data	DISPOFFB	Driver output voltage level (Y_1 – Y_{240})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
x	x	L	V_5

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H : V_{DD} (+2.4V to +5.5V), L : V_{SS}(0V), x : Don't care

Common Mode

FR	Latch data	DISPOFFB	Driver output voltage level (Y_1 – Y_{240})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
x	x	L	V_5

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H : V_{DD} (+2.4V to +5.5V), L : V_{SS}(0V), x : Don't care

NOTE : There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD driver, please supply regular voltage which assigned by specification for each power pin. That time 'Don't care" should be fixed to 'H" or "L ", avoiding floating.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND DRIVER OUTPUT PINS (Table 5)

Segment Mode

(a) 4-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Figure of clock						
					1st	2nd	3rd	..	58th	59th	60th
H	L	Output	Input	DI_0	Y237	Y233	Y229	..	Y9	Y5	Y1
				DI_1	Y238	Y234	Y230	..	Y10	Y6	Y2
				DI_2	Y239	Y235	Y231	..	Y11	Y7	Y3
				DI_3	Y240	Y236	Y232	..	Y12	Y8	Y4
H	H	Input	Output	DI_0	Y4	Y8	Y12	..	Y232	Y236	Y240
				DI_1	Y3	Y7	Y11	..	Y231	Y235	Y239
				DI_2	Y2	Y6	Y10	..	Y230	Y234	Y238
				DI_3	Y1	Y5	Y9	..	Y229	Y233	Y237

(a) 8-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Figure of clock						
					1st	2nd	3rd	..	28th	29th	30th
L	L	Output	Input	DI_0	Y233	Y225	Y217	..	Y17	Y9	Y1
				DI_1	Y234	Y226	Y218	..	Y18	Y10	Y2
				DI_2	Y235	Y227	Y219	..	Y19	Y11	Y3
				DI_3	Y236	Y228	Y220	..	Y20	Y12	Y4
				DI_4	Y237	Y229	Y221	..	Y21	Y13	Y5
				DI_5	Y238	Y230	Y222	..	Y22	Y14	Y6
				DI_6	Y239	Y231	Y223	..	Y23	Y15	Y7
				DI_7	Y240	Y232	Y224	..	Y24	Y16	Y8
L	H	Input	Output	DI_0	Y8	Y16	Y24	..	Y224	Y232	Y240
				DI_1	Y7	Y15	Y23	..	Y223	Y231	Y239
				DI_2	Y6	Y14	Y22	..	Y222	Y230	Y238
				DI_3	Y5	Y13	Y21	..	Y221	Y229	Y237
				DI_4	Y4	Y12	Y20	..	Y220	Y228	Y236
				DI_5	Y3	Y11	Y19	..	Y219	Y227	Y235
				DI_6	Y2	Y10	Y18	..	Y218	Y226	Y234
				DI_7	Y1	Y9	Y17	..	Y217	Y225	Y233

Table 5 (Continued)

Common Mode

MD	L/R	Data transfer direction	EIO1	EIO2	DI7
L (Single)	L(shift to left)	$Y_{240} \rightarrow Y_1$	Output	Input	X
	H(shift to right)	$Y_1 \rightarrow Y_{240}$	Input	Output	X
H (Dual)	L(shift to left)	$Y_{240} \rightarrow Y_{121}$ $Y_{120} \rightarrow Y_1$	Output	Input	Input
	H(shift to right)	$Y_1 \rightarrow Y_{120}$ $Y_{121} \rightarrow Y_{240}$	Input	Output	Input

Here, L : V_{SS}(0V), H : V_{DD}(+2.4V to +5.5V), X : Don't care

NOTE: "Don't care" should be fixed to "H" or "L", avoid floating.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 °C Referenced to V_{SS}(0V)	V_{DD}	-0.3 to +6.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	-0.3 to +35	V
	V_{12}		V_{12L}, V_{12R}	-0.3 to V_0+0.3	V
	V_{43}		V_{43L}, V_{43R}	-0.3 to V_0+0.3	V
	V_5		V_{5L}, V_{5R}	-0.3 to V_0+0.3	V
Input voltage	V_1		DI_0 –DI_7, XCK, LP, L/R, MD, S/C, EIO_1, EIO_2, DISPOFFB	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}			-45 to 125	°C

RECOMMENDED OPERATING CONDITIONS

Table 7. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	Referenced to V_{SS}(0V)	V_{DD}	+2.4		+5.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	+15		+32	V
Operating temperature	T_{OPR}			-20		+85	°C

NOTE: Ensure that voltage are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$

DC CHARACTERISTICS

DC CHARACTERISTICS(Table 8)

Segment Mode

(V_{SS}=V_5=0V, V_{DD}=+2.4 to 5.5V, V_0=+15 to +32V, Ta=-20~85°C)

Parameter	Symbol	Conditions		Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}			DI_0 -DI_7, XCK, LP, L/R, FR, MD, S/C,EIO_1, EIO_2, DISPOFFB	0.8V_{DD}			V
	V_{IL}						0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4mA		EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA					+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}		DI_0 -DI_7, XCK, LP, L/R, FR, MD, S/C,EIO_1, EIO_2, DISPOFFB			+10	uA
	I_{LIL}	V_I=V_{SS}					-10	uA
Output resistance	R_{ON}	|ΔV_{ON}| =0.5V	V_0=+30V	Y_1- Y_{240}		1.5	2.0	kΩ
			V_0=+20V			2.0	2.5	
Stand-by current	I_{STB}	*1		V_{SS}			75.0	uA
Consumed current(1) (Deselection)	I_{DD1}	*2		V_{DD}			2.0	mA
Consumed current(2) (Selection)	I_{DD2}	*3		V_{DD}			12.0	mA
Consumed current	I_0	*4		V_0			1.5	mA

NOTES: *1 V_{DD}=+5V, V_0=+32V, V_I=V_{SS}

*2 V_{DD}=+5V, V_0=+32V, f_{XCK}=20MHz, No-load, EI=V_{DD}
The input data is turned over by data taking clock (4-bit parallel input mode)

*3 V_{DD}=+5V, V_0=+32V, f_{XCK}=20MHz, No-load, EI=V_{SS}
The input data is turned over by data taking clock (4-bit parallel input mode)

*4 V_{DD}=+5V, V_0=+32V, f_{XCK}=20MHz, f_{LP}=25.6 kHz, f_{FR}=80Hz, No-load
The input data is turned over by data taking clock (4-bit parallel input mode)

Table 8 (Continued)

Common Mode

(V_{SS}=V_5=0V, V_{DD}=+2.4 to 5.5V, V_0=+15 to +32V, Ta=-20~85°C)

Parameter	Symbol	Conditions		Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}			DI_0 -DI_7, XCK, LP, L/R, FR, MD, S/C,EIO_1, EIO_2, DISPOFFB	0.8V_{DD}			V
	V_{IL}						0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4mA		EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA					+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}		DI_0 –DI_6, LP, L/R, FR, MD, S/C, DISPOFFB			+10	uA
	I_{LIL}	V_I=V_{SS}		DI_0 -DI_7, XCK, LP, L/R, FR, MD, S/C,EIO_1, EIO_2, DISPOFFB			-10	uA
Output resistance	R_{ON}	|Δ_{ON}| =0.5V	V_0=+30V	Y_1 – Y_{240}		1.5	2.0	kΩ
			V_0=+20V			2.0	2.5	
Input pull-down current	I_{PD}	V_I=V_{DD}		XCK, EIO_1, EIO_2, DI_7			100.0	uA
Stand-by current	I_{STB}	*1		V_{SS}			75.0	uA
Consumed current(1)	I_{DD}	*2		V_{DD}			120.0	uA
Consumed current(2)	I_0	*2		V_0			240.0	uA

NOTES: *1 V_{DD}=+5V, V_0=+32V, V_I=V_{SS}

*2 V_{DD}=+5V, V_0=+32V, f_{LP}=25.6kHz, f_{FR}=80Hz
case of 1/320 duty operation, No-load

AC CHARACTERISTICS

SEGMENT MODE AC CHARACTERISTICS(Table 9)

Segment Mode 1

(V_{SS}=V_5=0V, V_{DD}=+4.5 to +5.5V, V_0=+15 to +32V, Ta=-20~85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	T_{WCK}	T_R, T_F≤10 ns	50			ns
Shift clock "H" pulse width	T_{WCKH}		15			ns
Shift clock "L" pulse width	T_{WCKL}		15			ns
Data setup time	T_{DS}		10			ns
Data hold time	T_{DH}		12			ns
Latch pulse "H" pulse width	T_{WLPH}		15			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		30			ns
Latch pulse rise to shift clock rise time	T_{LS}		25			ns
Latch pulse fall to shift clock fall time	T_{LH}		25			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		10			ns
DISPOFFB removal time	T_{SD}		100			ns
DISPOFFB "L" pulse width	T_{WDL}		1.2			us
Output delay time (1)	T_D	C_L=15pF			30	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L=15pF			1.2	us
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	us

NOTES: *1 Take the cascade connection into consideration.

*2 (T_{WCK} – T_{WCKH} – T_{WCKL}) / 2 is maximum in the case of high speed operation.

Table 9 (Continued)

Segment Mode 2

(V_{SS}=V_5=0V, V_{DD}=+3.0V to +4.5V, V_0=+15 to +32V, Ta=-20~85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	T_{WCK}	T_R, T_F≤10 ns	66			ns
Shift clock "H" pulse width	T_{WCKH}		23			ns
Shift clock "L" pulse width	T_{WCKL}		23			ns
Data setup time	T_{DS}		15			ns
Data hold time	T_{DH}		23			ns
Latch pulse "H" pulse width	T_{WLPH}		30			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		50			ns
Latch pulse rise to shift clock rise time	T_{LS}		30			ns
Latch pulse fall to shift clock fall time	T_{LH}		30			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		15			ns
DISPOFFB removal time	T_{SD}		100			ns
DISPOFFB "L" pulse width	T_{WDL}		1.2			us
Output delay time (1)	T_D	C_L=15pF			41	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L=15pF			1.2	us
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	us

NOTES: *1 Take the cascade connection into consideration.

*2 (T_{WCK} – T_{WCKH} – T_{WCKL}) / 2 is maximum in the case of high speed operation.

Table 9 (Continued)

Segment Mode 3

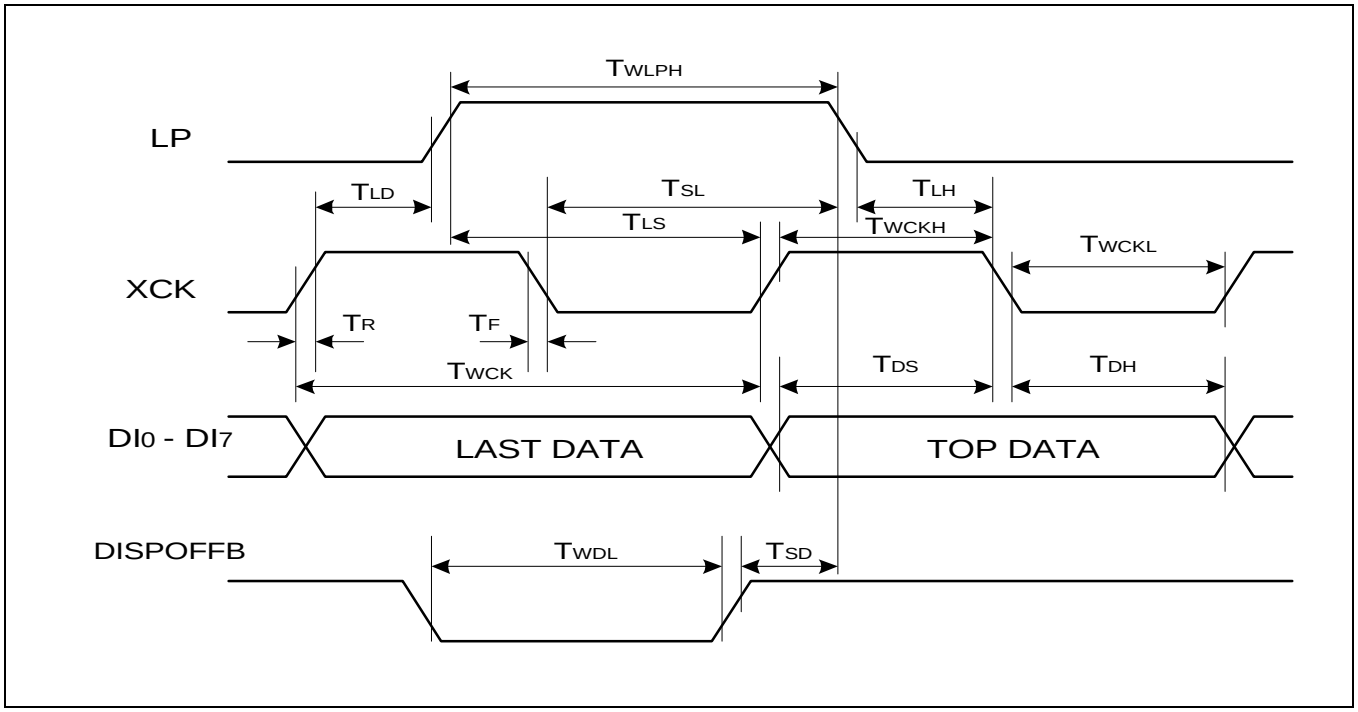
(V_{SS}=V_5=0V, V_{DD}=+2.4V to +3.0, V_0=+15 to +32V, Ta=-20~85°C)

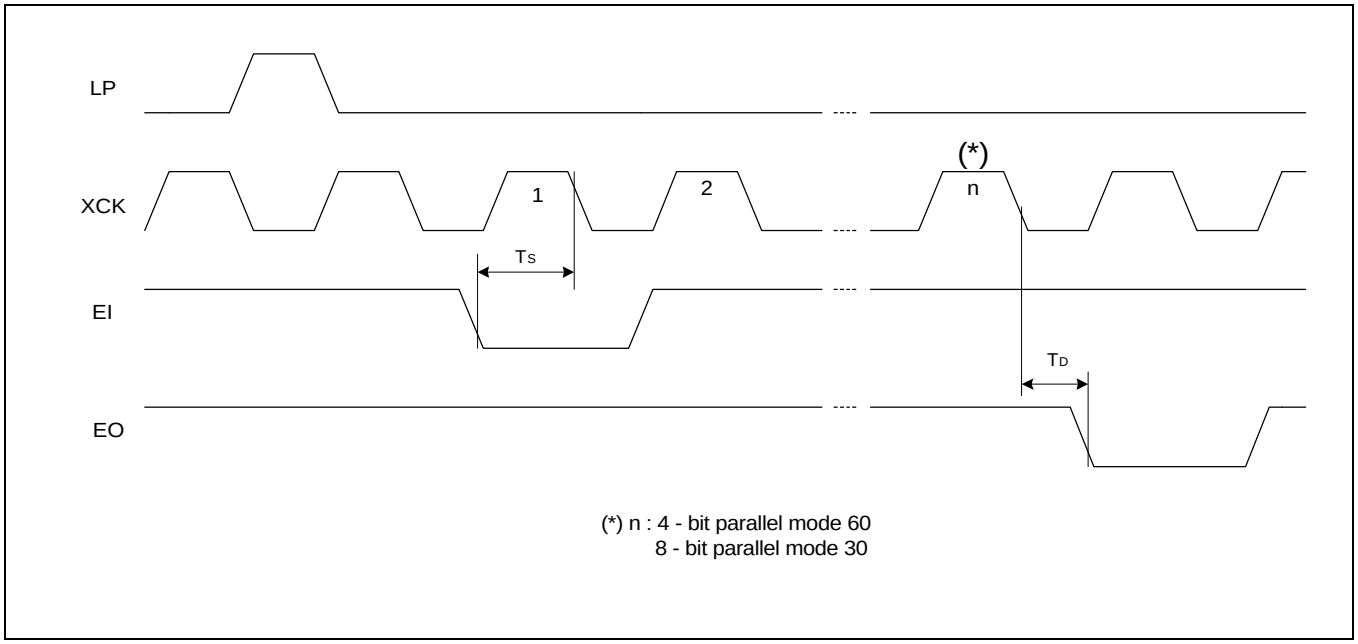
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	T_{WCK}	T_R, T_F≤10 ns	82			ns
Shift clock "H" pulse width	T_{WCKH}		28			ns
Shift clock "L" pulse width	T_{WCKL}		28			ns
Data setup time	T_{DS}		20			ns
Data hold time	T_{DH}		23			ns
Latch pulse "H" pulse width	T_{WLPH}		30			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		65			ns
Latch pulse rise to shift clock rise time	T_{LS}		30			ns
Latch pulse fall to shift clock fall time	T_{LH}		30			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		15			ns
DISPOFFB removal time	T_{SD}		100			ns
DISPOFFB "L" pulse width	T_{WDL}		1.2			us
Output delay time (1)	T_D	C_L=15pF			57	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L=15pF			1.2	us
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	us

NOTES: *1 Take the cascade connection into consideration.

*2 (T_{WCK} – T_{WCKH} – T_{WCKL}) / 2 is maximum in the case of high speed operation.

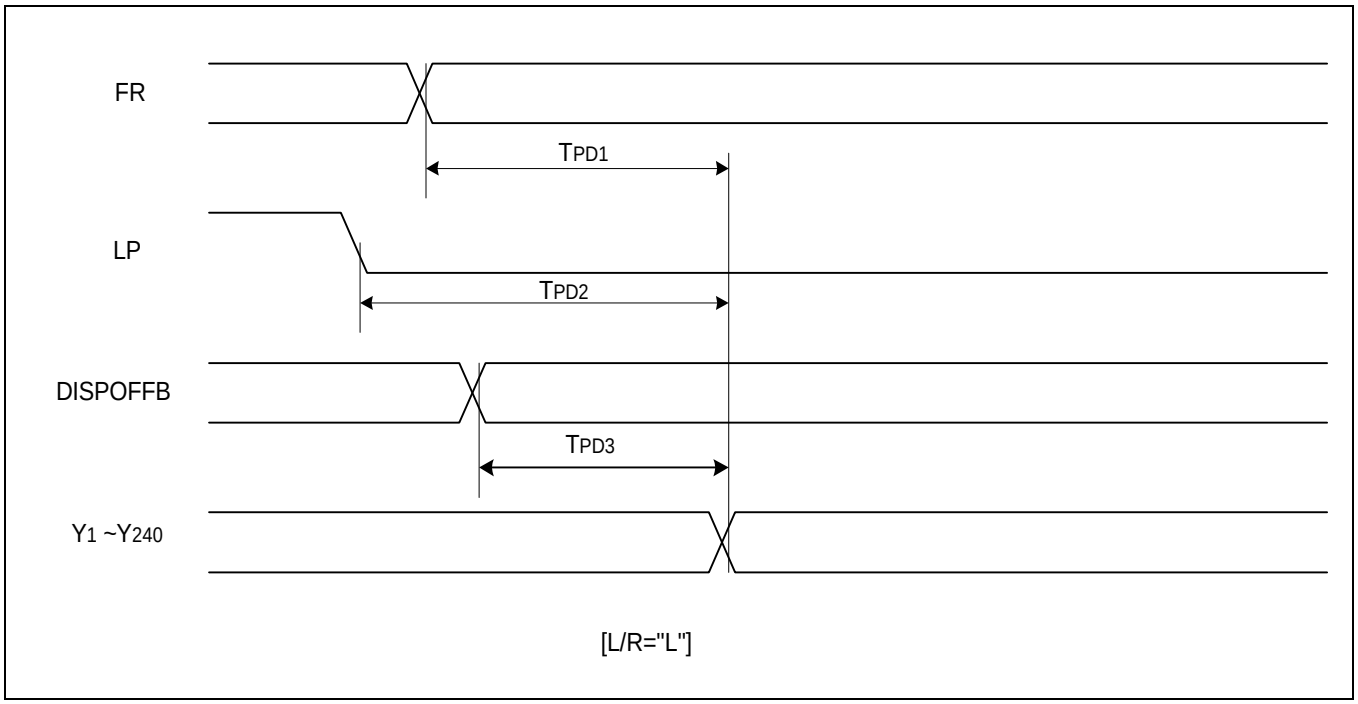
Timing Characteristics of Segment Mode (Figure 3)





(*) n : 4 - bit parallel mode 60
8 - bit parallel mode 30

Figure 3. (Continued)



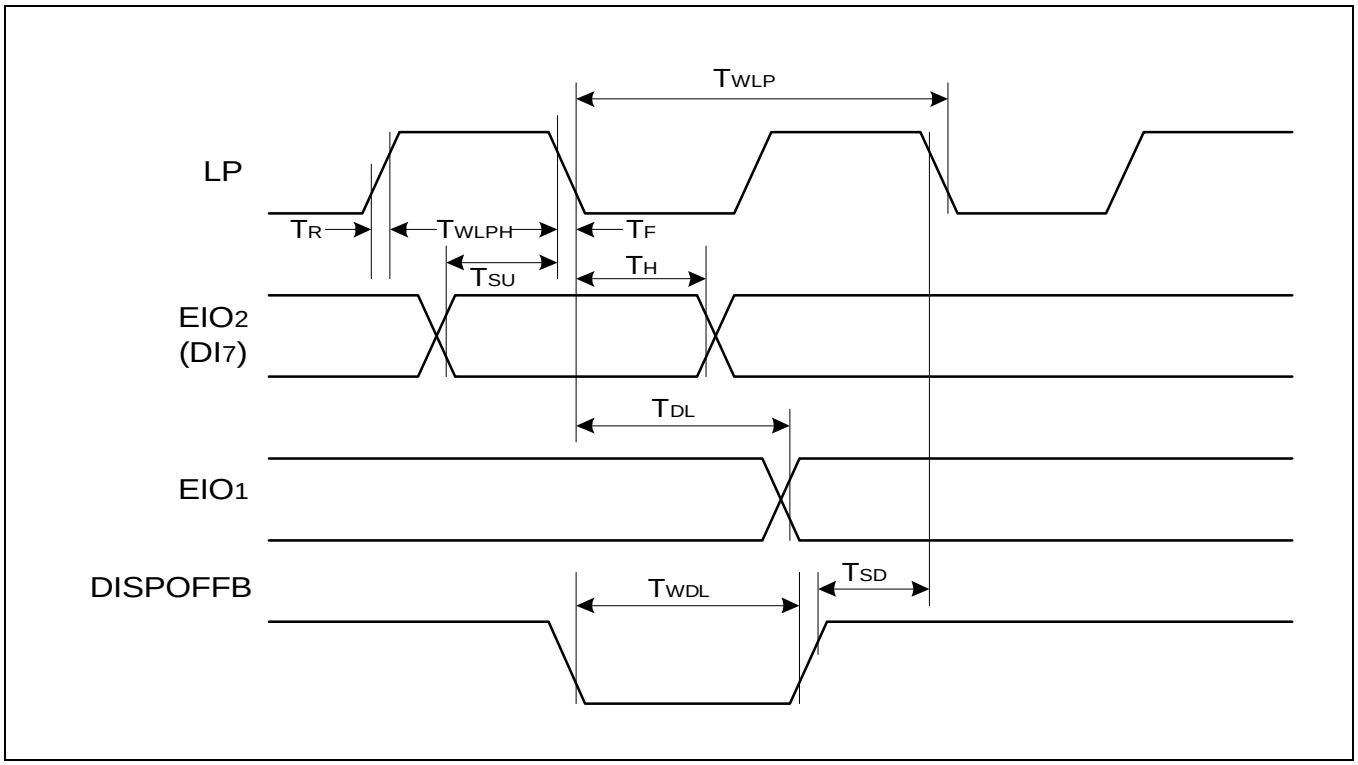
COMMON MODE AC CHARACTERISTICS (Table 10)

Common Mode

(V_{SS}=V_5=0V, V_{DD}=+2.4V to +4.5V, V_0=+15 to +32V, Ta=-20~85°C)

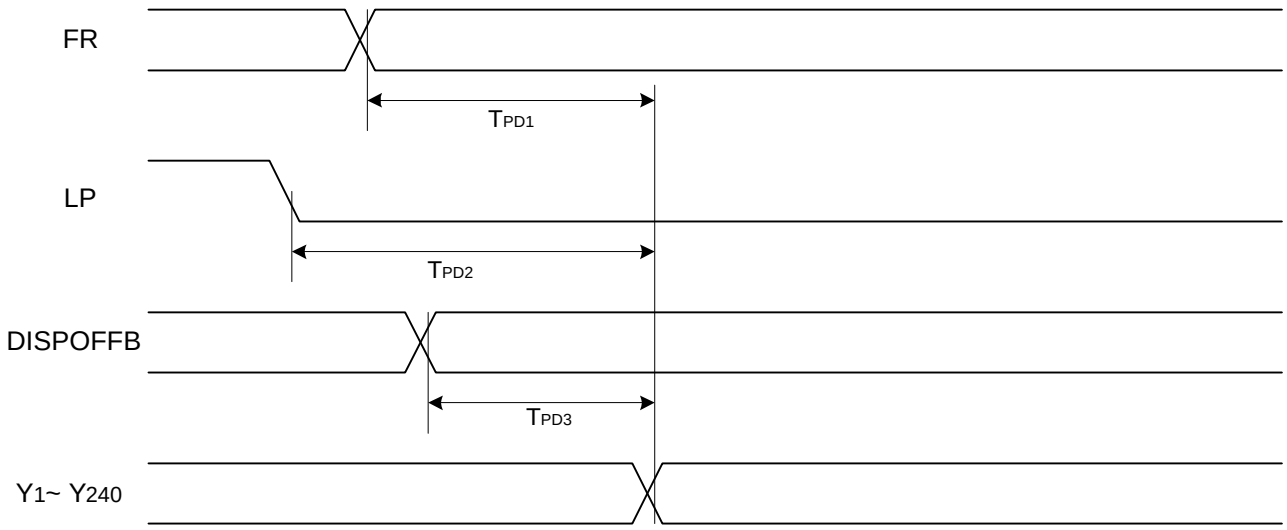
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	T_{WLP}	T_R, T_F≤20ns	250			ns
Shift clock "H" pulse width	T_{WLPH}	V_{DD}=+5.0V±10%	15			ns
		V_{DD}=+2.5V~+4.5V	30			ns
Data setup time	T_{SU}		30			ns
Data hold time	T_H		50			ns
Input signal rise time	T_R				50	ns
Input signal fall time	T_F				50	ns
DISPOFFB removal time	T_{SD}		100			ns
DISPOFFB 'L" pulse width	T_{WDL}		1.2			us
Output delay time (1)	T_{DL}	CL=15pF			200	ns
Output delay time (2)	T_{PD1},T_{PD2}	CL=15pF			1.2	us
Output delay time (3)	T_{PD3}	CL=15pF			1.2	us

Timing Characteristics of Common Mode (Figure 4)



SAMSUNG ELECTRONICS

Figure 4. (Continued)



[L/R="L"]

PRECAUTION

. PRECAUTION WHEN CONNECTING OR DISCONNECTING THE POWER

This LSI has a high-voltage LC driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC driver power supply while the logic system power supply is floating. The detail is as follows.

. When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC driver power.

. We recommend you connecting the serial resistor (50~100Ω) or fuse to the LC drive power V_0 of the system as a current limiter. And set up the suitable of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LC driver power supply after resetting logic condition of this LSI inside on DISPOFFB function. After that, cancel the DISPOFFB function after the LC driver power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V_5 on DISPOFFB function. After that, disconnect the logic system power after disconnecting the LC drive power. When connecting the power supply, show the following recommend sequence.

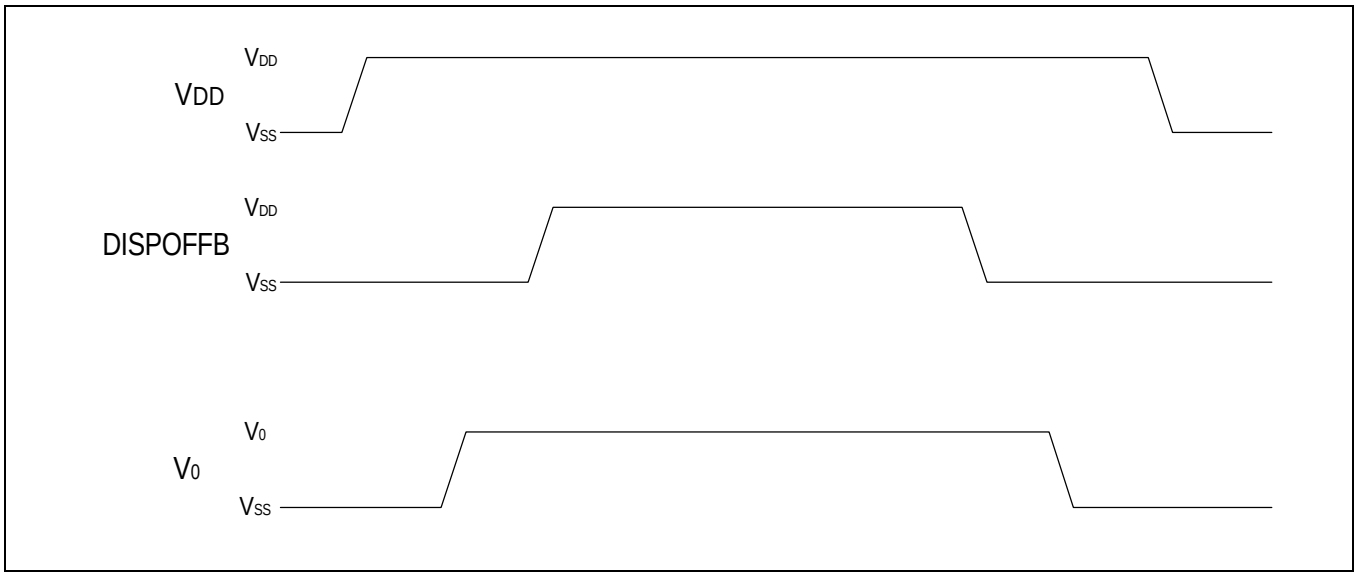


Figure 5.

CONNECTION EXAMPLES OF PLURAL SEGMENT DRIVERS

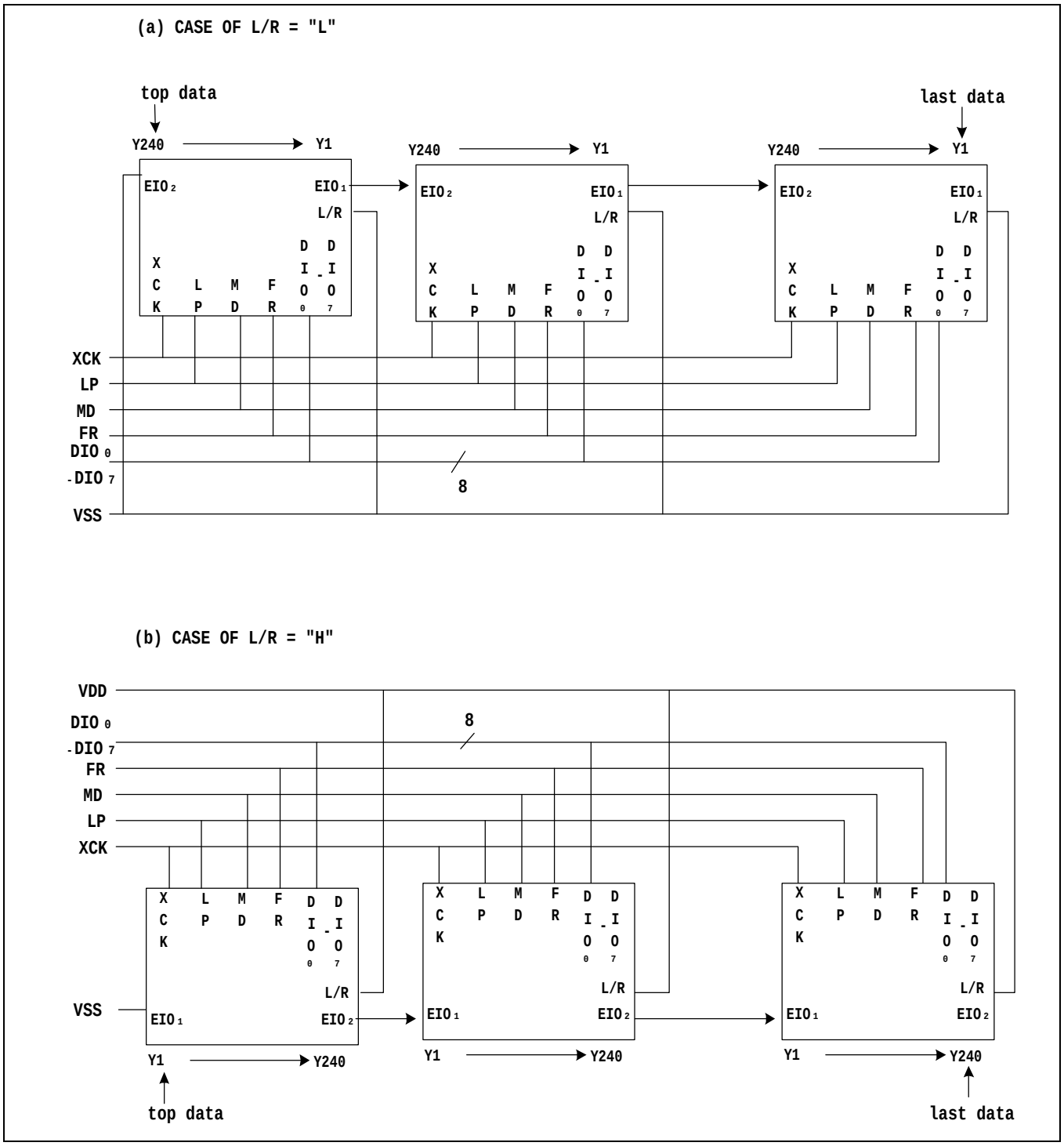


Figure 6.

TIMING CHART OF 4-DEVICE CASECADE CONNECTION OF SEGMENT DRIVERS

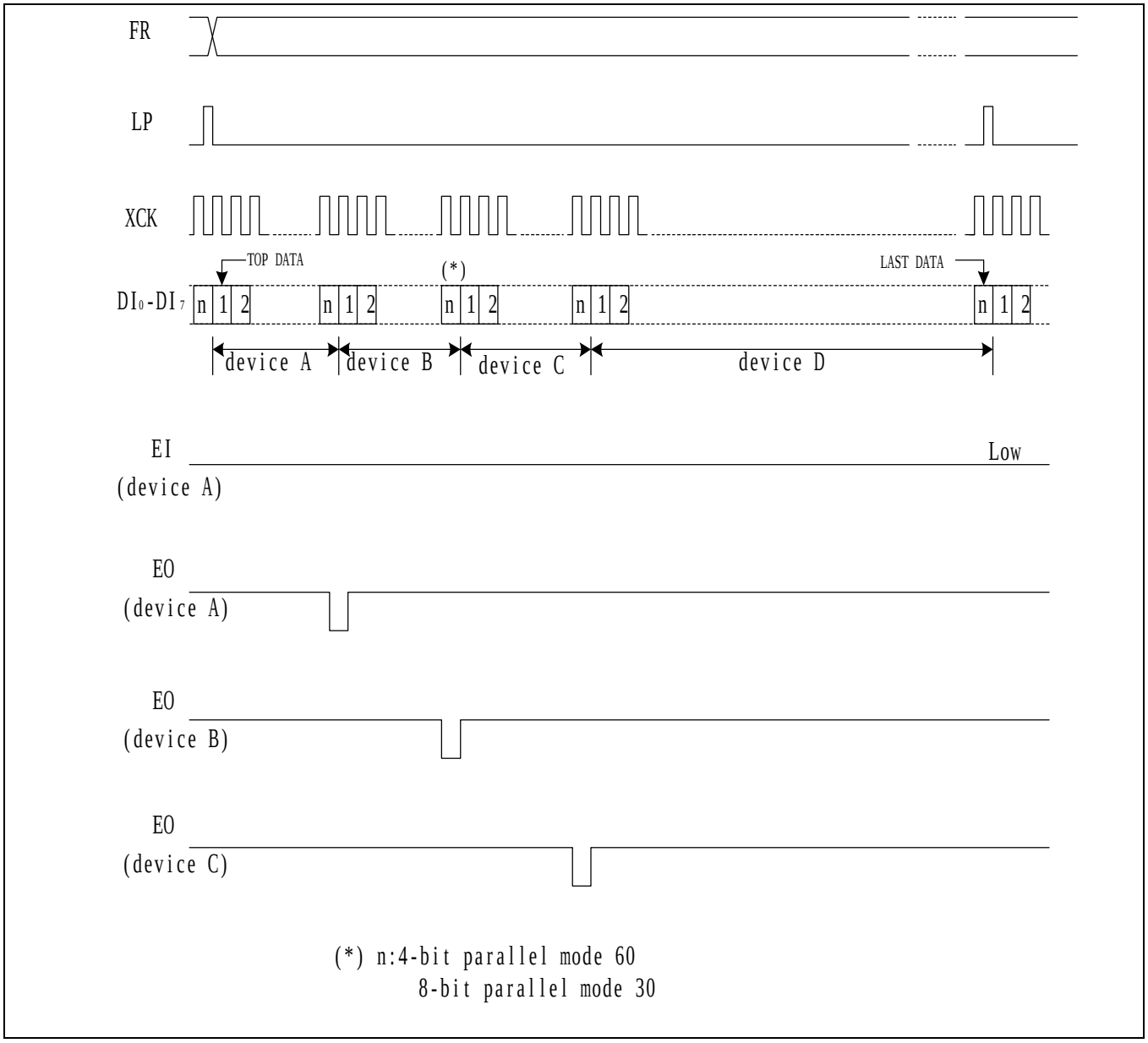


Figure 7.

CONNECTION EXAMPLES OF PLURAL COMMON DRIVERS

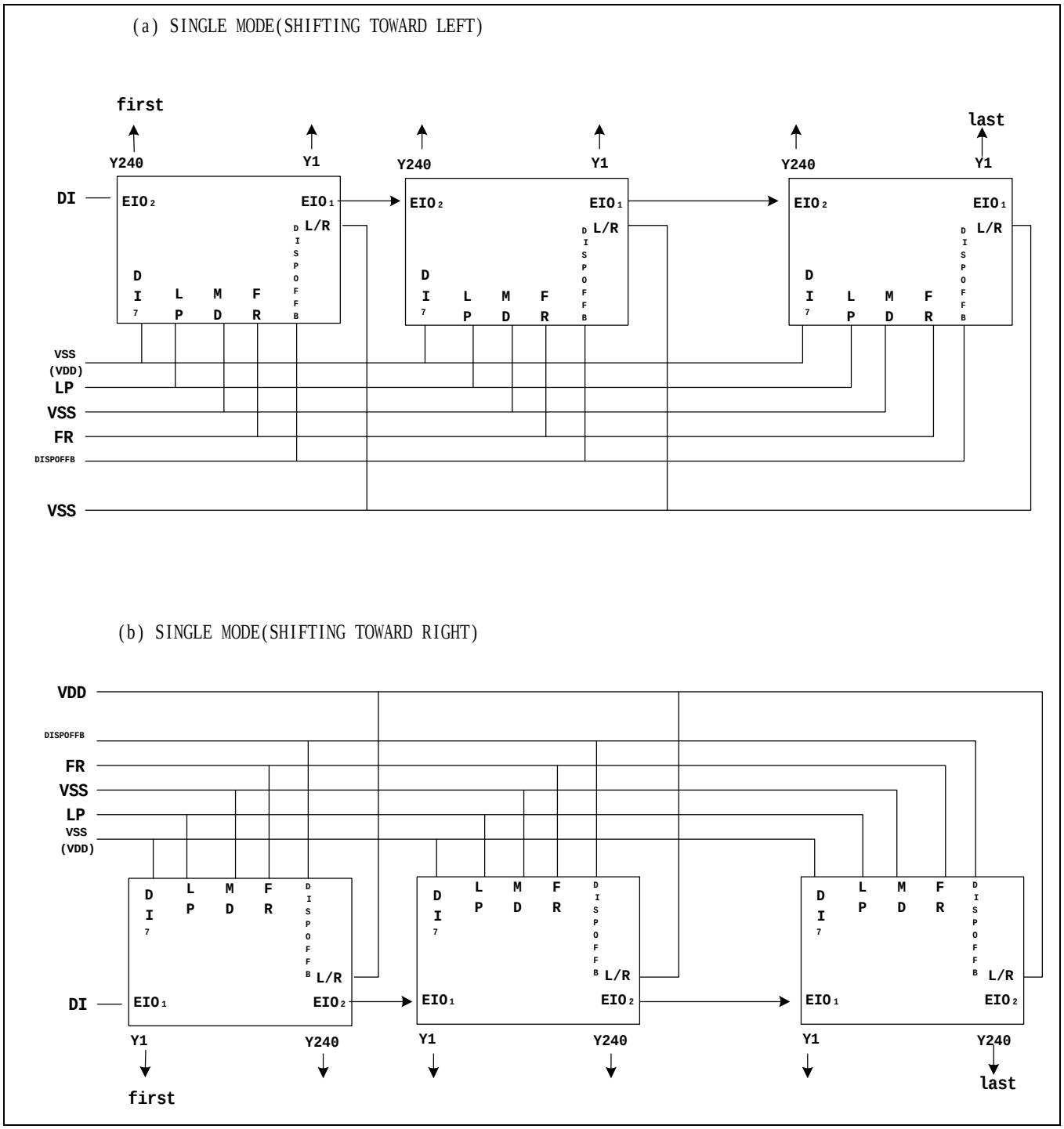
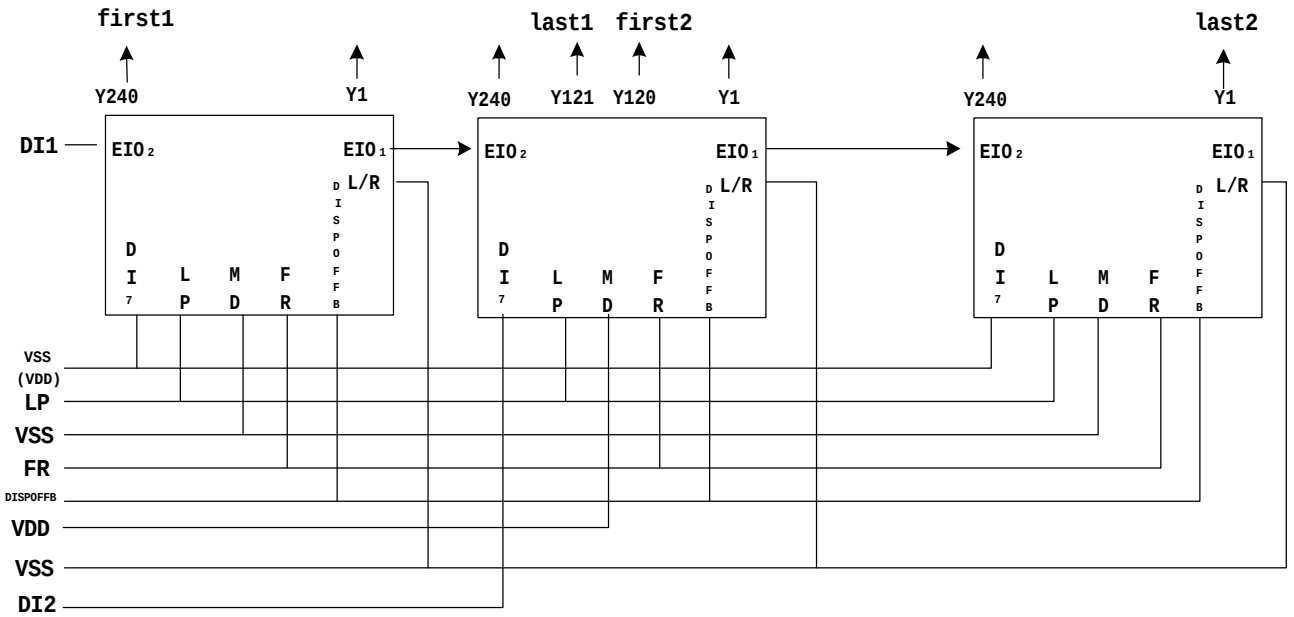


Figure 8.

(c) DUAL MODE(SHIFTING TOWARD LEFT)



(d) DUAL MODE(SHIFTING TOWARD RIGHT)

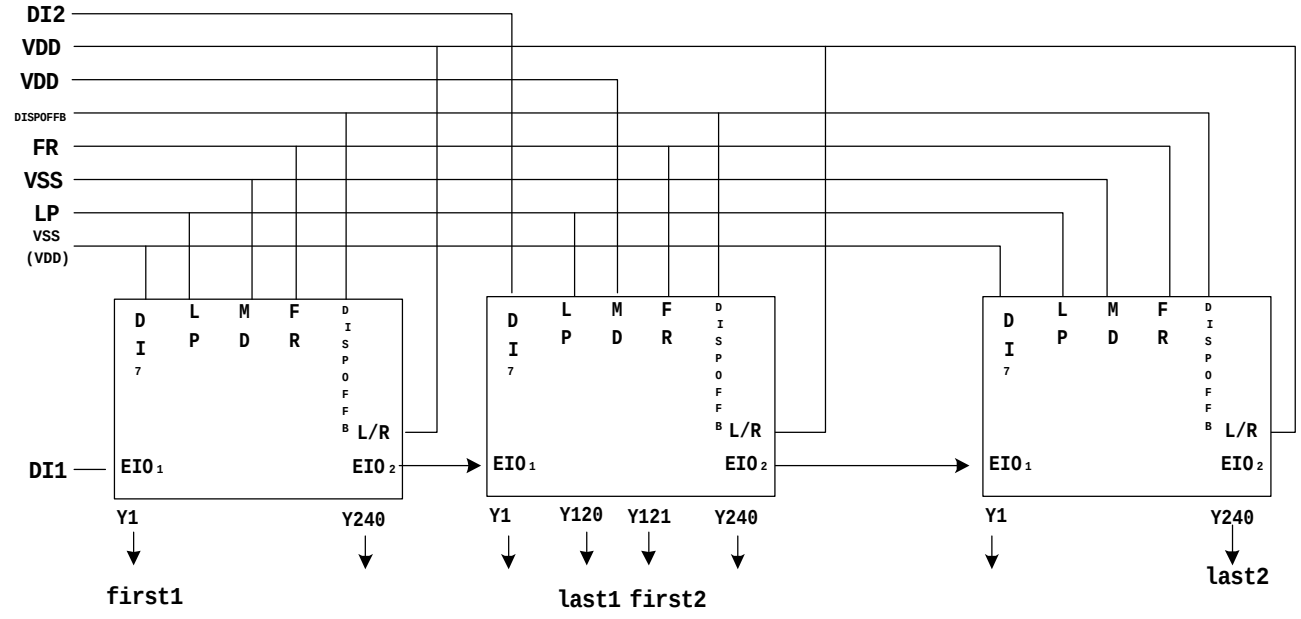


Figure 9.