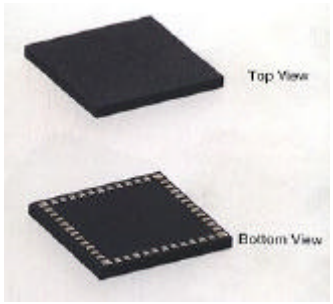
INTRODUCTION

S1M8662A is CDMA/PCS/GPS Triple Mode IF/ baseband IC which is divided into three main parts - IF frequency processing, basband processing , and digital interface. The receiver IC (S1M8662A)and transmitter IC (S1M8657) are provided as a KIT.
S1M8662A is a receiver IC, installed with a Rx AGC, Baseband Converter, Baseband analog filter, and A-D Converter. It can send a digital baseband signal to the digital baseband IC.

S1M8662A is fabricated on the Samsung's 0.5um high-speed, high frequency BICMOS processing and can achieve superior high frequency and low power digital operations.
Its operating voltage is 2.7 to 3.3V, and operating temperature -30 to +85°C .

32-BCC++-5.0×5.0



FEATURES

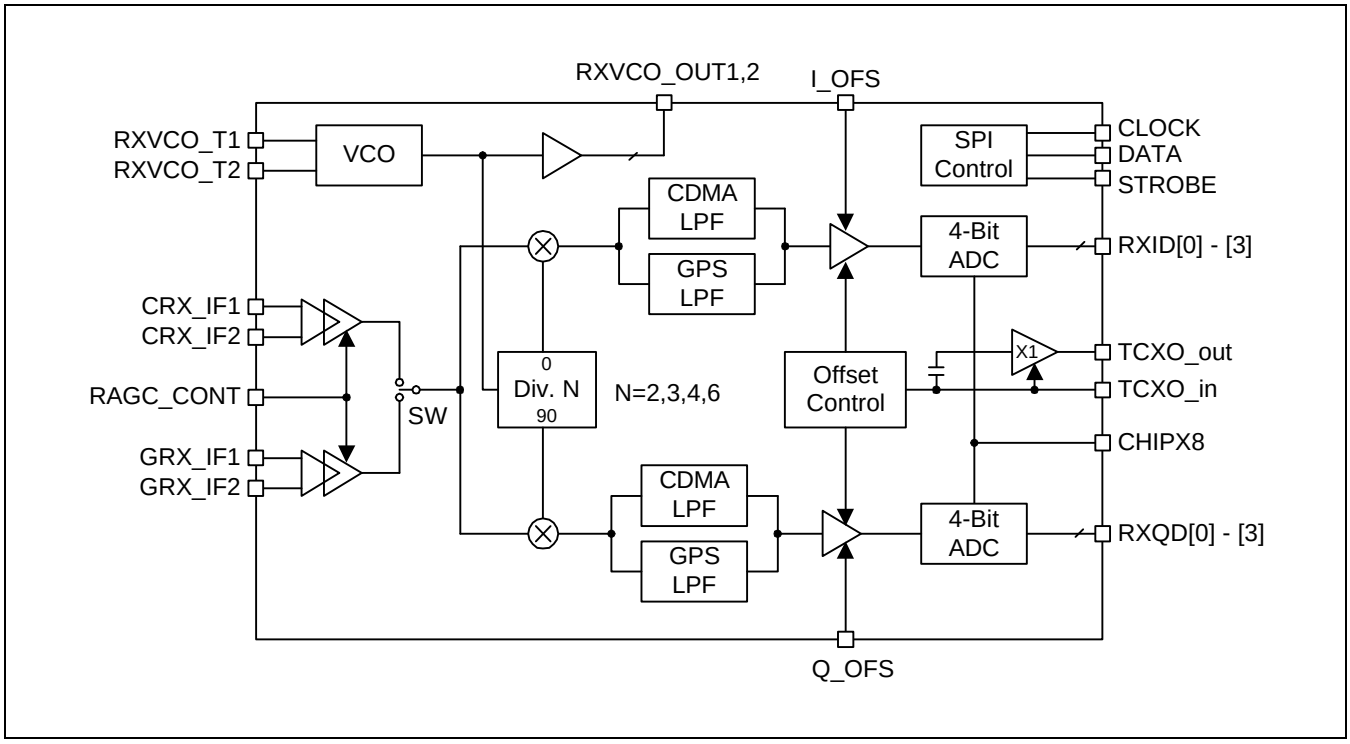
- Cellular CDMA/PCS/GPS Triple Mode
- AGC input signal range : 90dB
- QPSK Baseband Converter
- Built-in I ,Q Baseband signal extractor LPF
- Built-in 4-bit ADC for converting I and Q CDMA analog baseband signals to digital baseband signals
- Built-in VCO for baseband conversion
- Built-in Modem PDM control circuit to compensate the I and Q offsets
- Built-in TCXO output ON/OFF
- 3-Line Serial Port Interface (SPI)
- Operating Voltage : 2.7 to 3.3V
- 32BCC++(5mm * 5mm * 0.8mm) Package

ORDERING INFORMATION

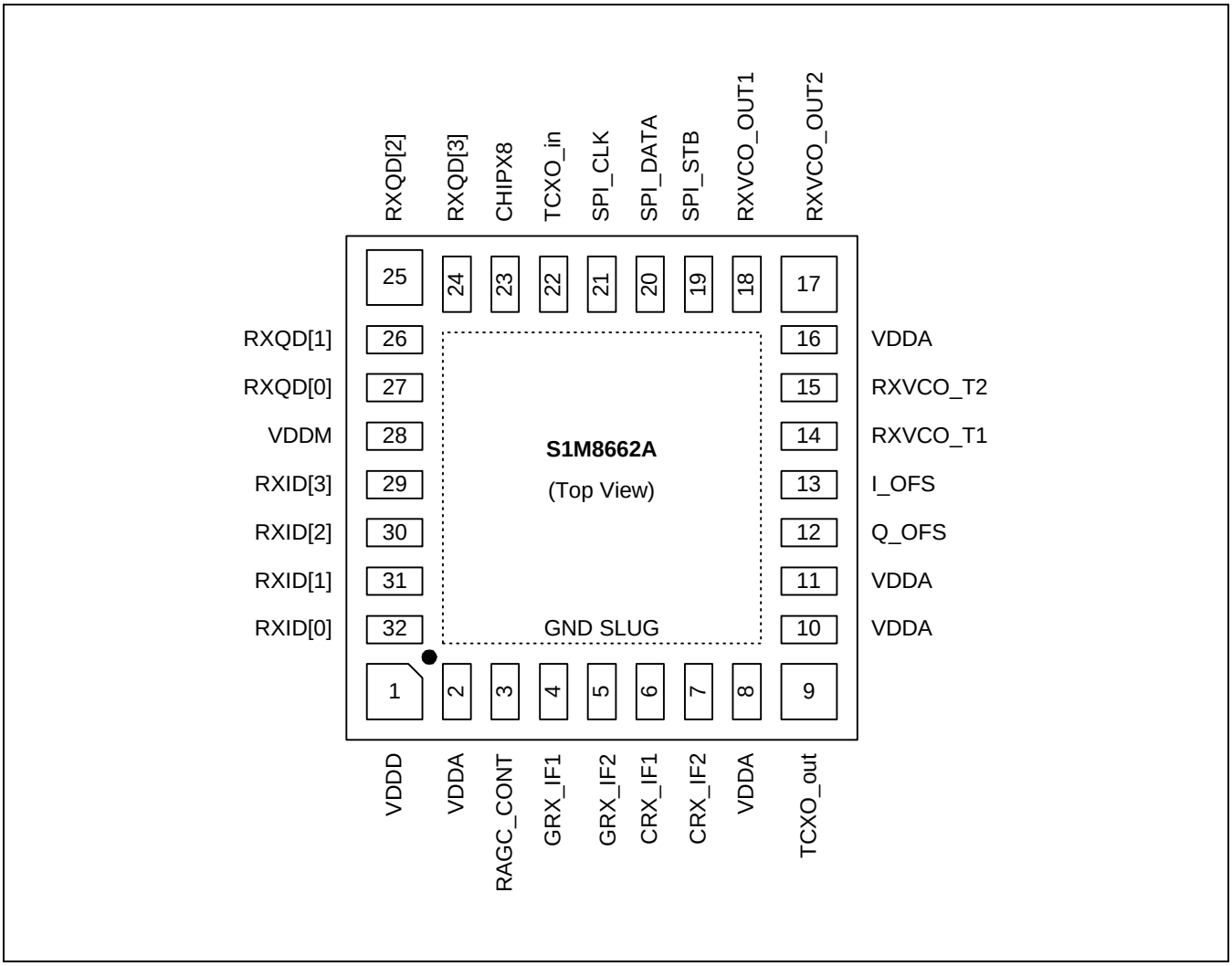
Device	Package	Operating Temperature
++ S1M8662AX01-F0T0	32-BCC++-5.0×5.0	-30 to +85°C

++ : Under Development

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	VDDD	P	Power for the digital logic.
2	VDDA	P	Power input terminal for the analog circuit.
3	RAGC_CONT	AI	AGC gain control input. The input voltage is allowed up to VDDA. It remains at High impedance during SLEEP.
4 5	GRX_IF1 GRX_IF2	AI	GPS IF input terminals, which have an input impedance of about 865W; generally, the GPS IF SAW filter is connected to them. When these terminals are not used, they remain at High impedance.
6 7	CRX_IF1 CRX_IF2	AI	CDMA IF input terminals, which have an input impedance of about 865Ω; generally, the CDMA IF SAW filter is connected to them. When these terminals are not used, they remain at High impedance.
8	VDDA	P	Power input terminal for the analog circuit.
9	TCXO_out	DO	TCXO Clock output. division ratio : 1
10	VDDA	P	Power input terminal for the analog circuit.
11	VDDA	P	Power input terminal for the analog circuit.
12 13	Q_OFS I_OFS	AI	Control DC input for removing the DC offset generated in the S1M8662A and system during CDMA and GPS Mode. The control DC is generated in the modem in PDM form, passes through the R-C filter and is converted to DC, which is sent to this input terminal.
14 15	RXVCO_T1 RXVCO_T2	AI	Very sensitive terminal, which is connected to the oscillation L-C resonance circuit. Their impedance are about 2kΩ
16	VDDA	P	Power input terminal for the analog circuit.
17 18	RXVCO_OUT1 RXVCO_OUT2	AO	Output for the PLL, able to output about -12dBm. When this is not used, it remains at high impedance.
19	SPI_STB	DI	3-Line serial control. Strobe input port. If this pin is opened, it remains at Low.
20	SPI_DATA	BI	3-Line serial control. DATA input/output port. If this pin is opened, it remains at Low.
21	SPI_CLK	DI	3-Line serial control. CLOCK input/output port. If this pin is opened, it remains at Low.
22	TCXO_in	AI/DI	Reference frequency input terminal connected to the VCTCXO output. When this pin stops, only DC bias is delivered to maintain the DC charge value of the capacitor connected externally
23	CHIPx8	DI	CHIPx8 Clock input port. CDMA/GPS ADC sampling clock from the MSM.

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
24 25 26 27	RXQD3 RXQD2 RXQD1 RXQD0	DO	Q Channel 4-bit A-D Converter's digital outputs, which are connected to the modem data input pins. These data are synchronized at CHIP×8's rising edge and output. Because they are valid at the falling edge, the data are latched at the falling edge in the modem.
28	VDDM	DI	Power source for a logic circuit ,related to the digital input /output, connected to an external digital logic such as the modem.
29 30 31 32	RXQD3 RXQD2 RXQD1 RXQD0	DO	I Channel 4-bit A-D Converter's digital outputs, which are connected to the modem data input pins. These data are synchronized at CHIP×8's rising edge and output. Because they are valid at the falling edge, the data are latched at the falling edge in the modem.

Table 1. S1M8660A and S1M8662A Function & Control Content Comparison

Function / Mode Control	S1M8660A	S1M8662A
Operation Modes		
CDMA (Cellular CDMA, PCS)	•	•
AMPS (FM)	•	
Global Positioning System (GPS)	•	•
IF AGC 90dB Range		
CDMA (Cellular CDMA, PCS)	•	•
AMPS (FM)	•	
Global Positioning System (GPS)	•	•
IF to Analog Baseband Quadrature Down-Conversion		
CDMA (Cellular CDMA, PCS)	•	•
AMPS (FM)	•	
Global Positioning System (GPS)	•	•
Low Pass Baseband I/Q Filtering with Mode Specific Performance		
CDMA (Cellular CDMA, PCS)	•	•
AMPS (FM)	•	
Global Positioning System (GPS)	•	•
4-bit I/Q Analog to Digital Converters, Parallel Outputs		
CDMA (Cellular CDMA, PCS)	•	•
Global Positioning System (GPS)	•	•
8-bit I/Q Analog to Digital Converters, Serial Outputs		
AMPS (FM)	•	
Rx Slotting Operation for Saving Current Consumption	•	•
Clock Generation		
TCXO/N Output	•	Δ (N=1)
Configurable CHIPx8 as Input or Output	•	Δ (Input)
VCO for Generation the Rx IF LO	•	•
Analog Baseband Amplifiers with I/Q Offset Controls	•	•

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value
Power supply	V_{CC}	-0.5 to 3.6V
Storage temperature	T_{STG}	-55 to +125°C
Operating temperature	T_{OPR}	-30 to +85°C
Storage temperature	HBM	TBD
Electrostatic discharge rating	MM	TBD

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value
Power supply	V_{DDA}, V_{DDD}	2.7 to 3.3V
	V_{DDM}	2.4 to 3.3V
Ambient operating temperature	Ta	-30 to +85°C

ELECTRICAL CHARACTERISTICS

Electrical Characteristics(V_{CC} = 3.3V, Ta = 25°C)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Units
Current consumption	CDMA idle mode	I_{CRX}	-	23	30	mA
Current consumption	CDMA sleep mode	I_{CSLP}	-	300	650	uA
Current consumption	CDMA slot mode	I_{CSLT}	-	5	7	mA
Current consumption	GPS idle mode	I_{GPS}	-	24	31	mA
Logic high input		V_{IH}	V_{DDM}-0.4	-	-	V
Logic low input		V_{IL}	-	-	0.4	V
Logic high output		V_{OH}	V_{DDM}-0.4	-	-	V
Logic low output		V_{OL}	-	-	0.4	V
Digital input capacitance		C_{DI}	-	-	5	pF
Digital output load capacitance		C_{DOL}	-	-	10	pF
TCXO input impedance	Attach C = 2pF	Z_{TCXO}	10	-	-	kΩ
VCO input resistance	IF VCO differential	R_{VCO}	-	2.0	-	kΩ
VCO input capacitance	IF VCO differential	C_{VCO}	-	-	2	pF

AC Characteristics

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
CDMA Performance						
Input sensitivity	Maximum AGC gain. Control input signal so that output corresponding to 3LSB is output from ADC.	VCSEN	-102	-	-	dBm
Maximum input signal	Minimum AGC gain. Control input signal so that output corresponding to 3LSB is output from ADC.	VCMAX	-	-	-12	dBm
AGC gain slope	PDM 3.3V Mode	GS LOPE	43	50	57	dB/V
AGC gain error over temperature	-30 to +85°C.	GVAR	-3	-	3	dB
IF input frequency range	Cin < 2pF	Fin	-	-	250	MHz
IF input Impedance		Zin	0.8	1.0	1.2	kΩ
Noise figure	Input power = -102dBm	NFmin	-	-	7	dB
	Input power = -75dBm	NFmid	-	-	20	dB
	Input power = -25dBm	NFmax	-	-	72	dB
IIP3	AGC gain Max.	IIP3max	-53	-	-	dBm
	AGC gain Min.	IIP3min	-10	-	-	dBm
Spurious contents	ADC generated harmonic frequency component. Two signals in the in-band are each mixed with signals which will allow ADC to produce -7dB output signals. The harmonic and non-harmonic components of the ADC output signals between 1kHz to 20MHz are extracted and added. The AGC control voltage is controlled so that ADC output is full scale when the input signal is -80dBm.	TSpur	-	-	-25	dBc
Spurious content related to jammer	In-band spurious peak value produced by IMD based on 2 jammer signals. One in-band signal(@50kHz,0.5*F/S) and two jammers(@900kHz, 22dB*F/S and @1.7MHz, 21dB*F/S)are simultaneously input. AGC control voltage is controlled so that ADC output is F/S when the input signal is -80dBm.	Jspur	-	-	-18.4	dBc

AC Characteristics (Continued)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Single-tone jammer desense	Overall gain reduction due to one jammer. The in-band signal at -97dBm (control the AGC control voltage to 0.5*F/S)and the jammer signal at 900kHz and -57dBm are simultaneously input.	Jdsen	-	-	1.0	dB
Residual Sideband	$RSB = 20\log\sqrt{\frac{1+k^2+2k\cos q}{1+k^2-2k\cos q}}$ *k* : Linear Gain Mismatch *q* : Phase Mismatch in Deg.	RSB	22			dB
Offset gain slope	Amount of code change of the voltage ADC output at the I/Q offset control	GOFS	-	250	-	%FS/V
Offset adjust input impedance	-	Zoff	100	-	-	kΩ
Out-band attenuation	≥ 900kHz	ATC9	46	-	-	dB
	≥ 1.2MHz	ATC12	48	-	-	dB
Gain flatness	Amount of gain change along I and Q paths between 1kHz to 615kHz	Gft	-1		1	dB
IF VCO pertormance						
VCO and buffered output Frequency range	VCO external time constant and PLL value	Fvco	-	170	500	MHz
VCO phase noise	Tank LC's Q value should be above 20. Measure @100kHz away from the mid-frequency.	Pvco	-	-	104	dBc/Hz
RXVCO_OUT output power	Select a VCO buffer output value reduced by -2dB. Connect output load to 50Ω.	Ovco	-15	-	-	dBm

AC Characteristics (Continued)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
GPS Performance						
Input sensitivity	Maximum AGC gain. Control input signal so that ADC outputs 0.5*F/S.	VCSEN	-102	-	-	dBm
Maximum input signal	Minimum AGC gain Control input signal so that ADC outputs 0.5*F/S.	VCMAX	-	-	-12	dBm
AGC gain slope	PDM 3.3V Mode	GSLOPE	43	50	57	dB/V
AGC gain error over temperature	-30°C to +85°C.	GVAR	-3	-	3	dB
IF input frequency range	Cin < 2pF	Fin	-	-	250	MHz
IF input Impedance		Zin	0.8	1.0	1.2	kΩ
Noise figure	Input power = -98dBm	NFmin	-	-	7	dB
	Input power = -75dBm	NFmid	-	-	12	dB
	Input power = -25dBm	NFmax	-	-	58	dB
IIP3	AGC gain Max.	IIP3max	-53	-	-	dBm
	AGC gain Min.	IIP3min	-25	-	-	dBm
Offset gain slope	Amount of code change of the voltage ADC output at the I/Q offset control	GOFS		250		%FS/V
Offset adjust input impedance	-	Zoff	100	-	-	kΩ
Out-band attenuation	≥ 1.3MHz	ATC13	46	-	-	dB
	≥ 1.7MHz	ATC17	48	-	-	dB
Residual Sideband	$RSB = 20\log\sqrt{\frac{1+k^2+2k\cos q}{1+k^2-2k\cos q}}$ k : Linear Gain Mismatch q : Phase Mismatch in Deg.	RSB	22	-	-	dB
Gain flatness	Amount of gain change along I and Q paths between 1kHz to 800kHz	Gft	-1.5	-	1.5	dB

TIMING DIAGRAMS

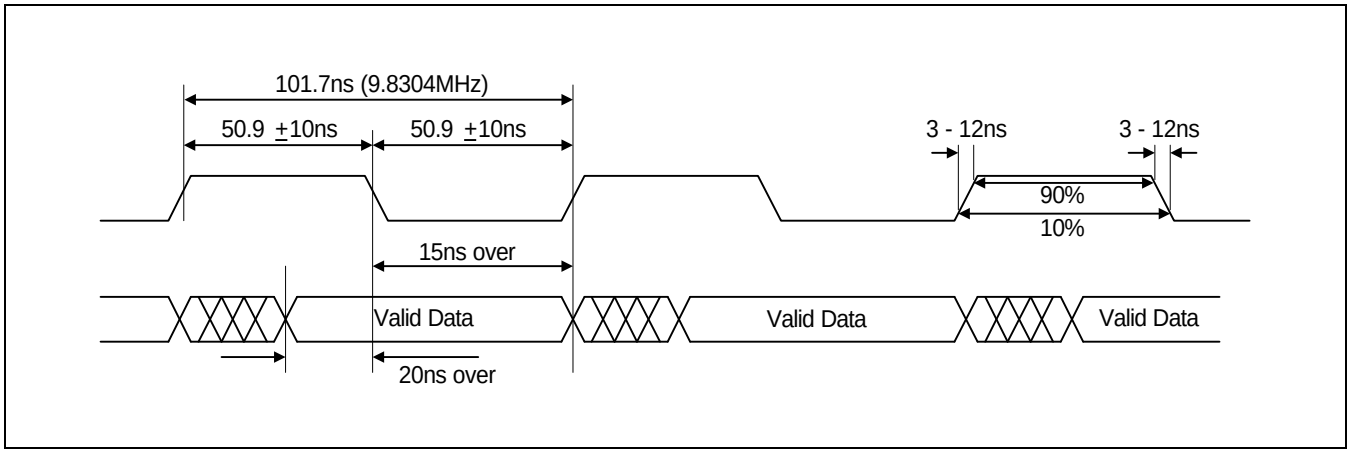


Figure 1. CDMA Receive ADC Timing

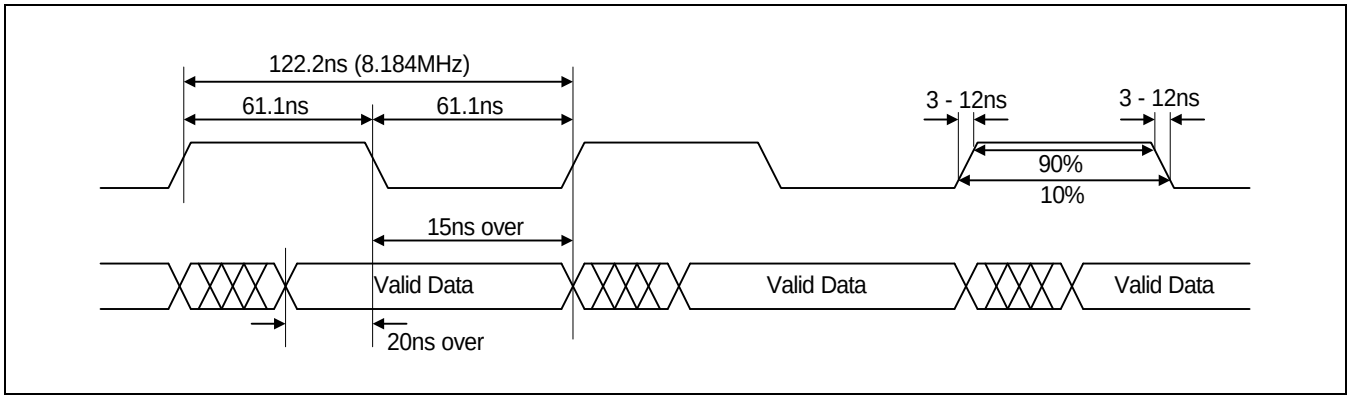


Figure 2. GPS Receive ADC Timing

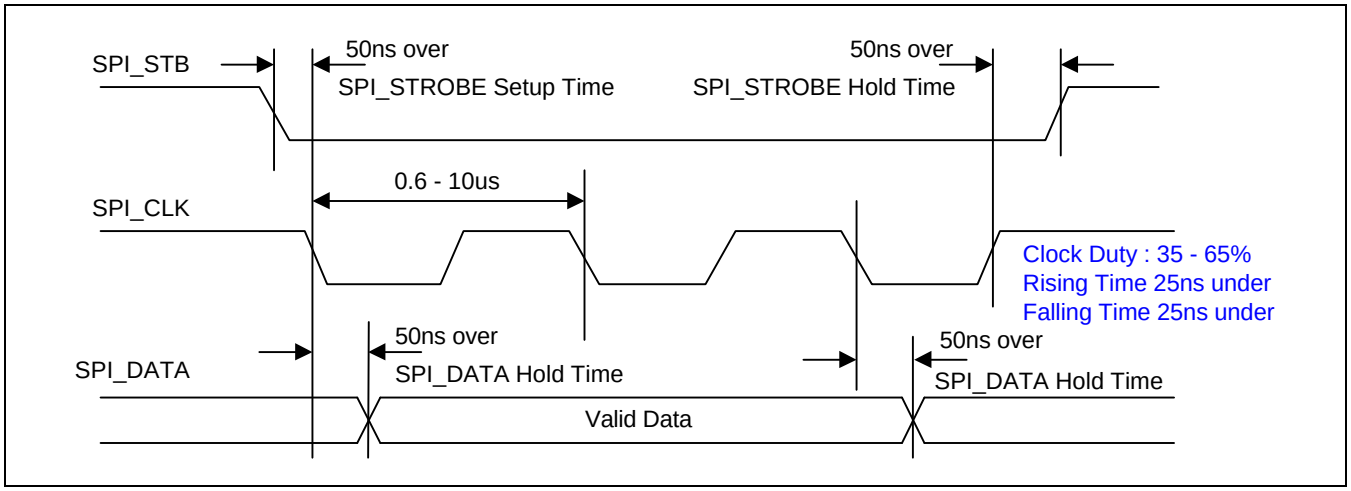


Figure 3. 3-Line Serial Port Interface Timing

FUNCTIONAL DESCRIPTION

S1M8662A is a CDMA/GPS receive-only baseband analog IC, located between the RF mid-frequency processing terminal and baseband processing terminal. The RF analog mid-frequency signal terminal(IF SAW filter output), directly connected to the S1M8662A mid-frequency input pin, converts and processes the baseband signal and sends the corresponding digital signal to the modem IC. Baseband analog processing uses QPSK modulation, LPF, and A-D converter and the modem IC performs digital CDMA /GPS baseband modulation on the digitalized analog baseband signal it receives. An on-chip VCO creates a multiple frequency(x2, x3, x4, x6) LO signal.

S1M8662A uses a 0.5um BiCMOS, equipped with high-frequency bipolar and low power standardized CMOS logic, to operate safely in the low power range, consisting of power voltage between 2.7 to 3.3V and operating temperature between -30 to +85°C.

CDMA Receive Signal Path

The receive circuit of S1M8662A has the Rx AGC, an automatic gain controller, and baseband LPF and output terminal with the A-D converter, and VCO and mixer etc. The input signal is received as a differential signal, which is modulated to 1.23 MHz spread-spectrum for CDMA. The mid-frequency is 220.38MHz for Korea-PCS, 1.23MHz for US-PCS, and 85.38MHz for cellular; they are set based on the time constants of the components involved with the external VCO and external Rx PLL. Rx AGC , connected to both the IF SAW filter and matching component in the RF-IF converter output located in the RF block, amplifies or reduces according to the signal size. It takes its orders from the modem chip when it sets the appropriate receive level as required by the CDMA system. Gain is controlled by applying a DC voltage to the RAGC_CONT pin. The applied DC is produced when the PDM signal, generated as a control signal in the modem, passes through the R-C filter. The control band of this AGC is approx. 90dB. The QPSK Baseband modulator separates and modulates the IF signal sent by the AGC using I(In-phase) and Q(Quad-phase) baseband signal. Essentially, two signals, I-LO and Q-LO (Local oscillator), are mixed with AGC's IF output signals, respectively. The LO(local oscillator) signal is generated by the internal oscillating components, externally connected tank coil, and Varactor, and the externally independent PLL device is used to generate its exact oscillation mid-frequency.

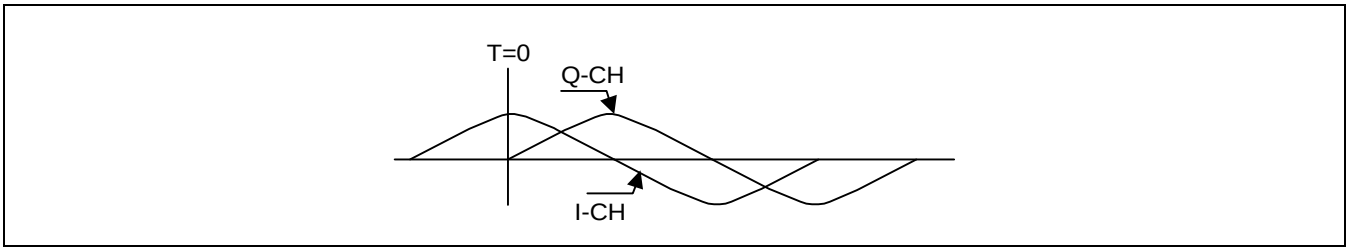


Figure 4. Received I/Q Phase in S1M8662A

Defining of the I-Phase and Q-Phase receive path is very important to its design. The polarities of these paths are also important to digital baseband modulation. Therefore, the output of the QPSK baseband modulation determines the I and Q phases; I-phase is defined as the phase leading the Q-phase by exactly 90°, but it simpler to think of I as Cosin and Q as Sin. The figure related to this is shown in Figure 5. This definition is valid only when the QPSK IF input signal is higher than the IF mid-frequency. The baseband signal, output by the QPSK modulator, includes various other unnecessary surrounding band noises, which are removed by the use of the LPF(Low-Pass-Filter).

Ultimately, I and Q filtered signals are converted to digital signals by the 4-bit A-D converter and sent to the modem. The A-D converter used is a parallel output type and its outputs are synchronized at the CHIP×8 rising edge. The modem chip captures the data on the CHIP×8 falling edge. The CHIP×8 clock used in the A-D converter received to MSM.

GPS Rx Signal Path

The difference of the S1M8662A from the S1M8656A is that S1M8662A provides GPS receiving operation. While GPS receiving path shares function blocks with CDMA modes, it needs independent AGC and lowpass filter.

GPS IF signal from GPS RF-IF mixer is applied to S1M8662A via GPS SAW filter. GPS IF is differential input pins.

The operation of I/Q demodulator is the same in CDMA modes and the phase relation of I/Q signal of the output is the same as depicted in Figure 5.

GPS lowpass filter of S1M8662A has its cut off frequency at around 800kHz.

A-D converter, as output of GPS path, is the 4bit parallel converter which is the same one used in CDMA path. But the sampling frequency is different from that of CDMA mode. And in operating in GPS mode, sampling clock of A-D converter should be supplied from the modem.

TCXO Clock Generator

In S1M8656A and S1M8660A, the output of TCXO is divided by 1, 2, and 4 and then clocked out. But in S1M8662A the output of TCXO is just amplified and clocked out. So, there is no SPI control which controls the division ratio of TCXO clock. In this product, the TCXO_in pin can input both TCXO signal (TCXO_sig) and TCXO control (TCXO_cont) at the same time.

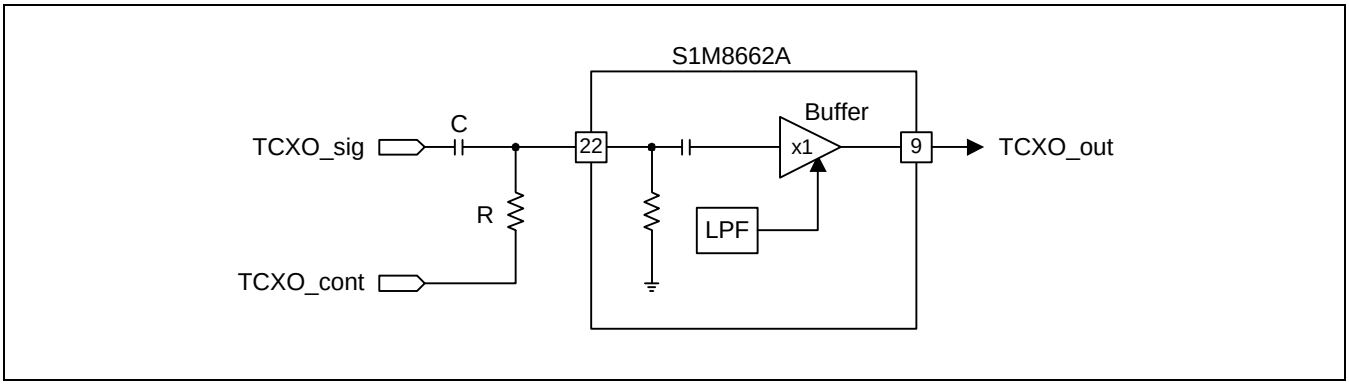


Figure 5. TCXO Clock Generating

If TCXO_cont pin is held low or high-impedance (floating), TCXO_out keeps high, and on the contrary, if TCXO_cont pin is held high, TCXO_out outputs TCXO clock. If TCXO_cont pin is low or high-impedance (floating), S1M8662A can be pin to pin compatible with IFR3500 of Qualcomm.

RX VOLTAGE CONTROLLED OSCILLATOR(VCO)

S1M8662A includes the Rx LO block having the VCO and quad-phase generator. The quad-phase generator outputs I-phase and Q-phase clocks with 1/2, 1/3, 1/4 or 1/6 the VCO frequency and sends them to the QPSK modulator. The VCO buffer is used when the VCO output is sent to the external RX PLL. Although the allowable VCO frequency is determined based on an external time constant, it can only range between approx. 100MHz to 500MHz, suggesting that the maximum input IF frequency is 250MHz.

Serial Port Interface(SPI)

S1M8662A is equipped with the Serial I/F. All internal functions can be controlled through a common bus using an external controller. S1M8662A is designed to be completely compatible with MSM series of Qualcomm. Here, the modem is the master and S1M8662A the slave.

Each pin which uses the SPI bus has the following common functions.

- The STB(STROBE) for the serial bus start signal is used to initialize serial data transmission.
- Serial BUS DATA is used for the bi-direction data input /output at serial data transmission. Because it is an open drain type pin, it requires the pull-up resistance of approx. 8kΩ.
- Serial BUS CLK is used to synchronize the data input/output at serial data transmission.

Serial Port Interface Operation

The modem, the master, controls slaves such as S1M8662A using the SPI bus.
The STB falling edge indicates the start of the serial I/F data transmission. The STB becomes high to mark the end of the data transmission.
(Data sent after the STB turns high are not valid.)
Serial line data is captured and stored as soon as the BBA or the MODEM places the clock on the falling edge.
The SPI 3-line must remain high for at least 1-clock cycle in order to sent new data.
The MSB always outputs the data line data.
After 9-clocks, which is required to send data, the data line driver opens the data line, at which time the data line becomes high because of the external pull-up resistance.

Serial Data Transfer format

S1M8662A and S1M8657 are all slave devices with the SPI bus. What differentiate them from one another is their different device IDs. Each company has its own characteristic SPI bus configuration , but normally the 3-line bus is most often used and sometimes the 2-line bus such as the IIC bus.

Figure 7. shows the serial data transfer format.

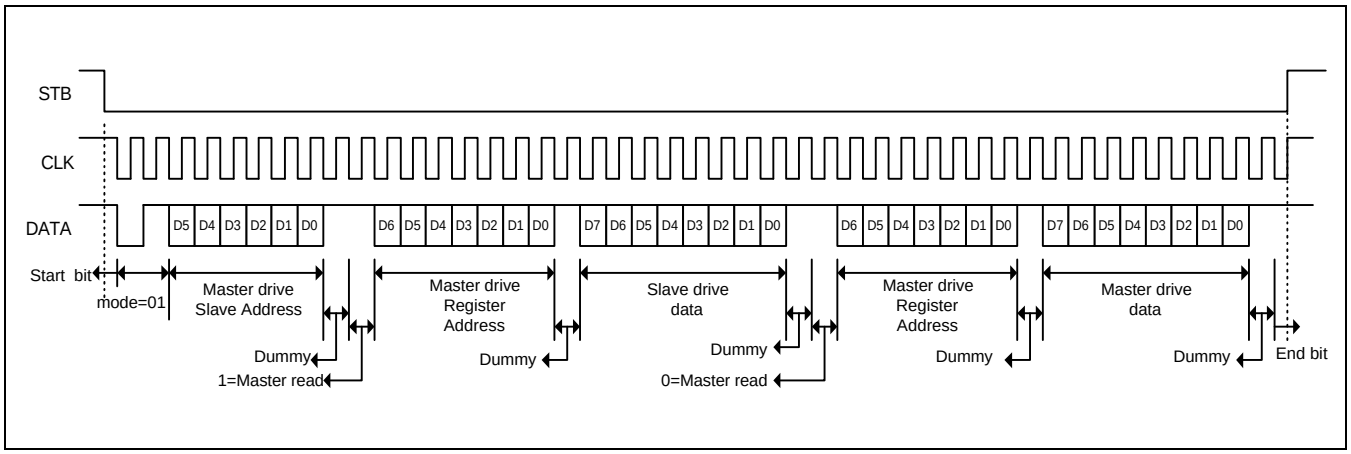


Figure 6. Serial Data Transfer Format

(1) The first 2-BITs are for transmission only and this product must send '01'.(Others are not permitted.)

(2) The following 6-bit data specifies the slave device, which is connected to the SPI bus and has its own ID.

(3) The following 1-bit is a dummy bit, which marks the end of the 8-bit data transmission and the beginning of the next data to be sent.

(4) The following 1-bit decides on whether the master will drive the data line or the slave will. If this bit is '1', the master will drive , but if '0' the slave will drive the data line.

(5) The following 7-bit data is the register address of the specified slave device; the 7-bits for an address allows 128 register addresses for slaves.

(6) The following high 1-BIT data is a dummy data.

(7) The following 8-BIT data is the data in the device to be driven.

(8) The following 1-BIT data is a dummy data, which marks the end of the 8-bit data transmission and beginning of the next data to be sent.

(9) The following 1-bit decides on whether the master will drive the data line or the slave will. If this bit is '1', the master will drive , but if '0' the slave will drive the data line.

(10) The following 7-bit data is the register address of the specified slave device.

(11) The following high 1-BIT data is a dummy data.

(12) The following 8-BIT data is the data in the device to be driven.
(Continous data transmission such as this can be ended with a 1-byte transmission or can be read/written repeatedly.)

(13) After the last data is sent, the data line opens and becomes high;

(14) the CLK continues for half the 1-clock cycle and then becomes high;

(15) and the STB becomes high as soon as the clock becomes high and this marks the end of data transmission.

Modes of Operation

S1M8662A can be controlled by the SPI bus.
Table 2 shows the various modes.

Table 2. Mode control in the DC control mode

Mode	0x03[1:0] BLOCK_CTL	0x06[7] VCO_CTL	0x052:0] FILTER_SEL	CHIPx8
Sleep	00	X	XXX	All circuit are off
CDMA idle(Rx)	01 or 11	0	100	CDMA Mode
GPS idle(Rx)	01 or 11	1	111	CDMA Mode
CDMA Sot	10	0	100	All circuit are off except the VCO, VCO buffer
GPS Slot	10	1	111	Not used

CONTROL REGISTERS

S1M8662A has various registers which can be programmed by the SPI bus. These registers have their own function which are described below.

Table 3. S1M8660A Control Registers

Register name	Address	R/W	Default vale	Description
RESET	0x00	W	-	Reset. Reset S1M8662A and all the register values are returned to their default value.
SPI_ID	0x01	R	0x1F	SPI_ID. Each slave device has its own, independent code; S1M8662A code is 1E.
BLOCK_CTL	0x03	R/W	0x8	BLOCK_CTL Decides on the S1M8662A operation mode. LO division ratio. Controls VCO output.
FILTER_SEL.	0x05	R/W	0x1C.	FILTER_SEL. Lowpass filter selection
VCO_CTL	0x06	R/W	0x0B	VCO_CTL. Controls the VCO operation and VCO output.

W : MODEM is recorded in the S1M8662A register R : When S1M8662A sends data to the modem

Table 4. Description of Control Registers

Address	Name	Type	Bits	Description
00(h)	RESET	W	-	When the master uses this register, the S1M8662A returns all the programmed register values to their initial value.
01(h)	SPI_ID	R	[5:0]	This read-only register is used to confirm the type of slave connected to the master. It is set to 1Eh and all S1M8662A has the same value. This is the ID absolutely required to differentiate the controller from the data, when there are many slaves connected to the SPI bus.

Table 4. Description Of Control Registers (Continued)

Address	Name	Type	Bits	Description
03(h)	Block_CTL	R/W	[7]	Identifies the S1M8662A Default = 1
			[6]	Default = 0, Reserved Registers
			[5:4]	IF LO Divider, Default = 00 00 : 2, 01 : 3 10 : 4, 11 : 6
			[3]	Default = 1, Reserved Registers
			[2]	RXVCO_OUT2. Default = 1 1 : Singled Ended Output (RXVCO_OUT1 Active, RXVCO_OUT2 Off) 0 : Differential Output (RXVCO_OUT1, 2 Active)
			[1:0]	Mode. Default = 00 00 : Sleep, 01 : Receive 10 : Rx Slot, 11 : Receive
05(h)	FILT_SEL	R/W	[7:2]	Default = 0001 11 Reserved Registers
			[1:0]	FILT_SEL Default = 00 00 : CDMA LPF 10 : GPS LPF
06(h)	VCO	R/W	[7]	GPS_SEL Default = 0 0 : GPS Mode Disabled 1 : GPS Mode abled
			[6:3]	Default = 0001 Reserved Registers
			[2]	CCO_CTL Default = 0 0 : RX_VCO Low Drive 1 : RX_VCO Low Max
			[1]	Default = 11. Reserved Registers

CHARACTERISTIC GRAPH

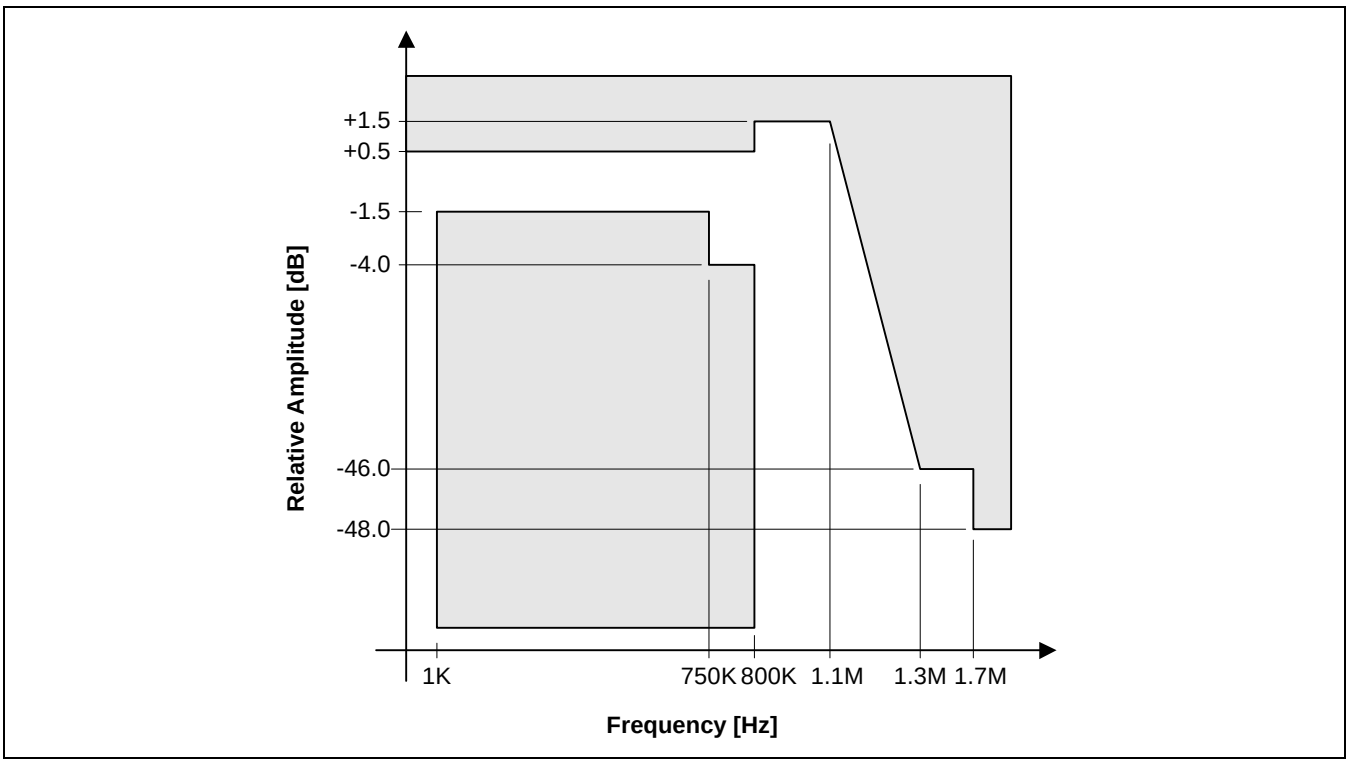


Figure 7. GPS Rx Low Pass Filter Mask

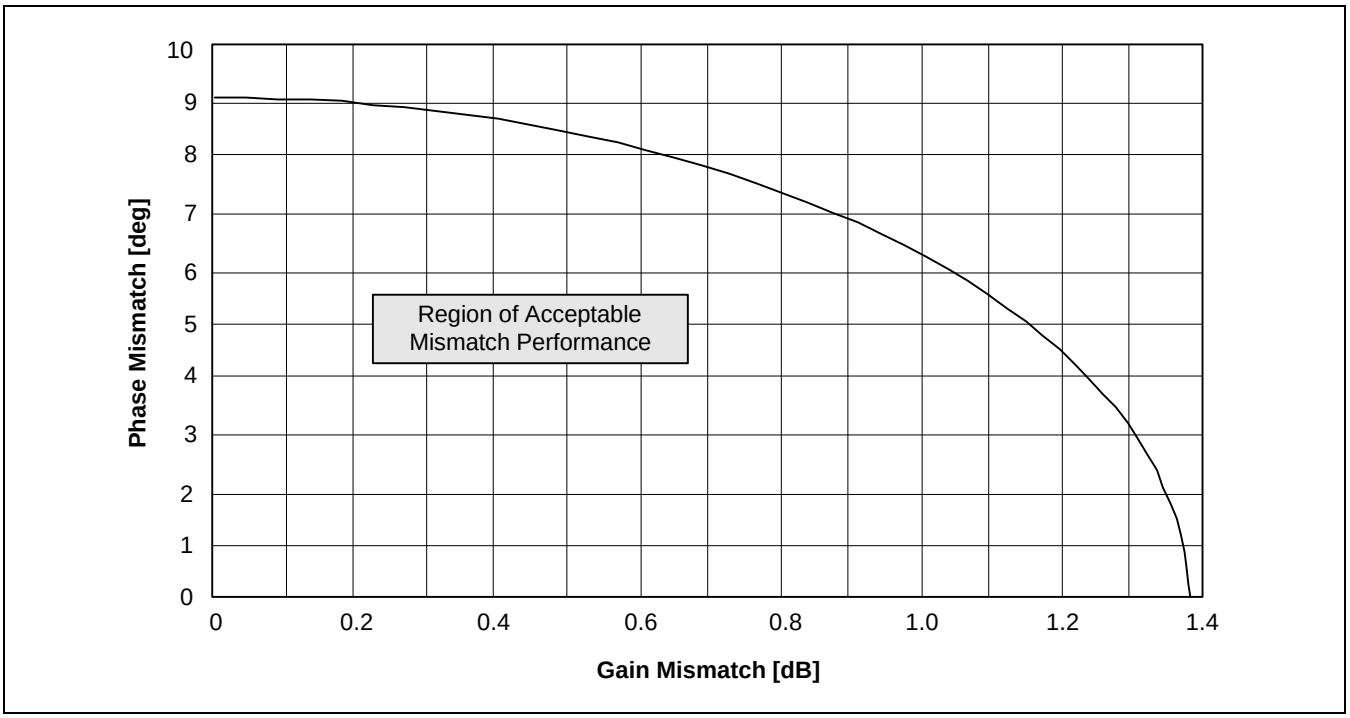


Figure 8. GPS Rx Gain/Phase Mismatch Specification

CHARACTERISTIC GRAPH (Continued)

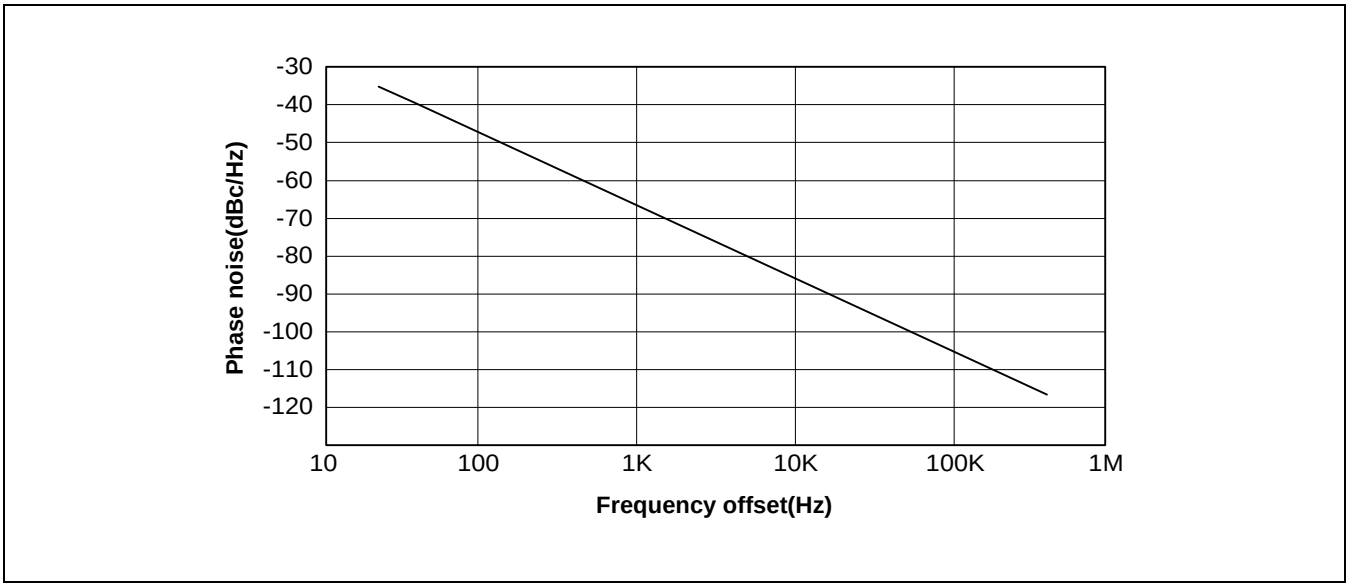


Figure 9. S1M8662A IF VCO Open Loop Phase Noise

CHARACTERISTIC GRAPH (Continued)

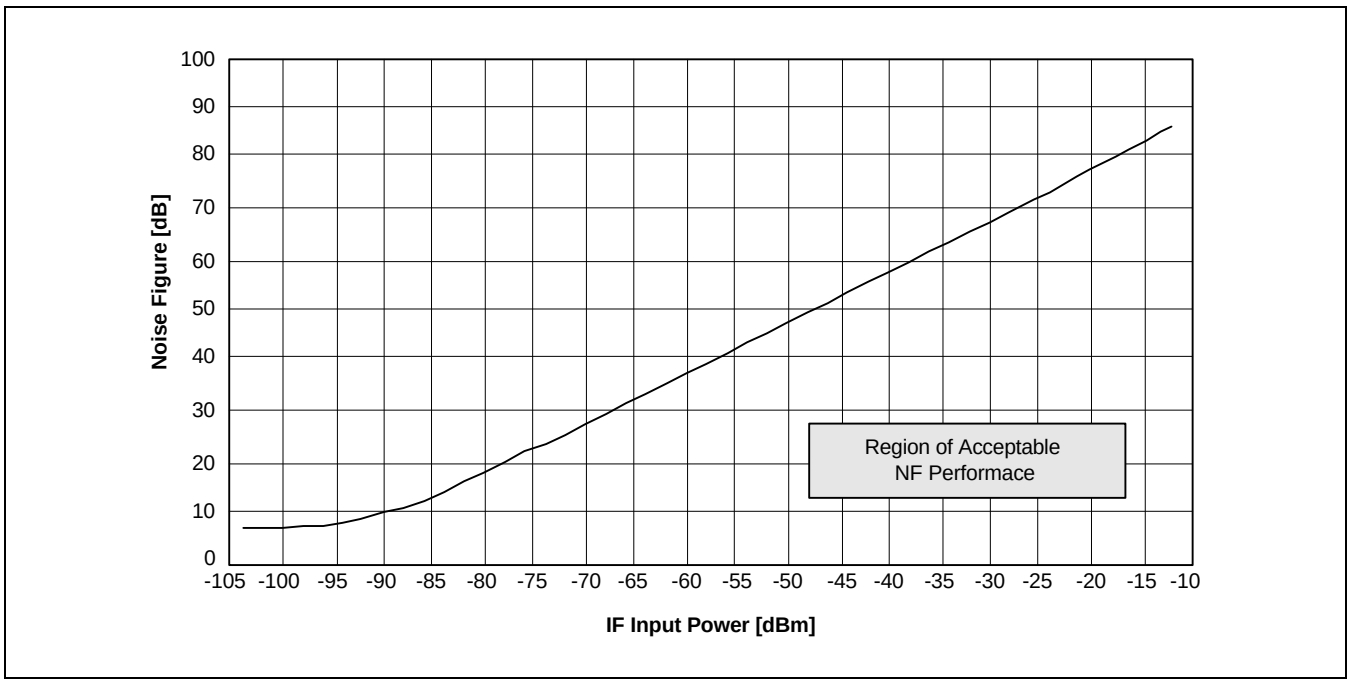


Figure 10. GPS Rx Mode Noise Figure Specification

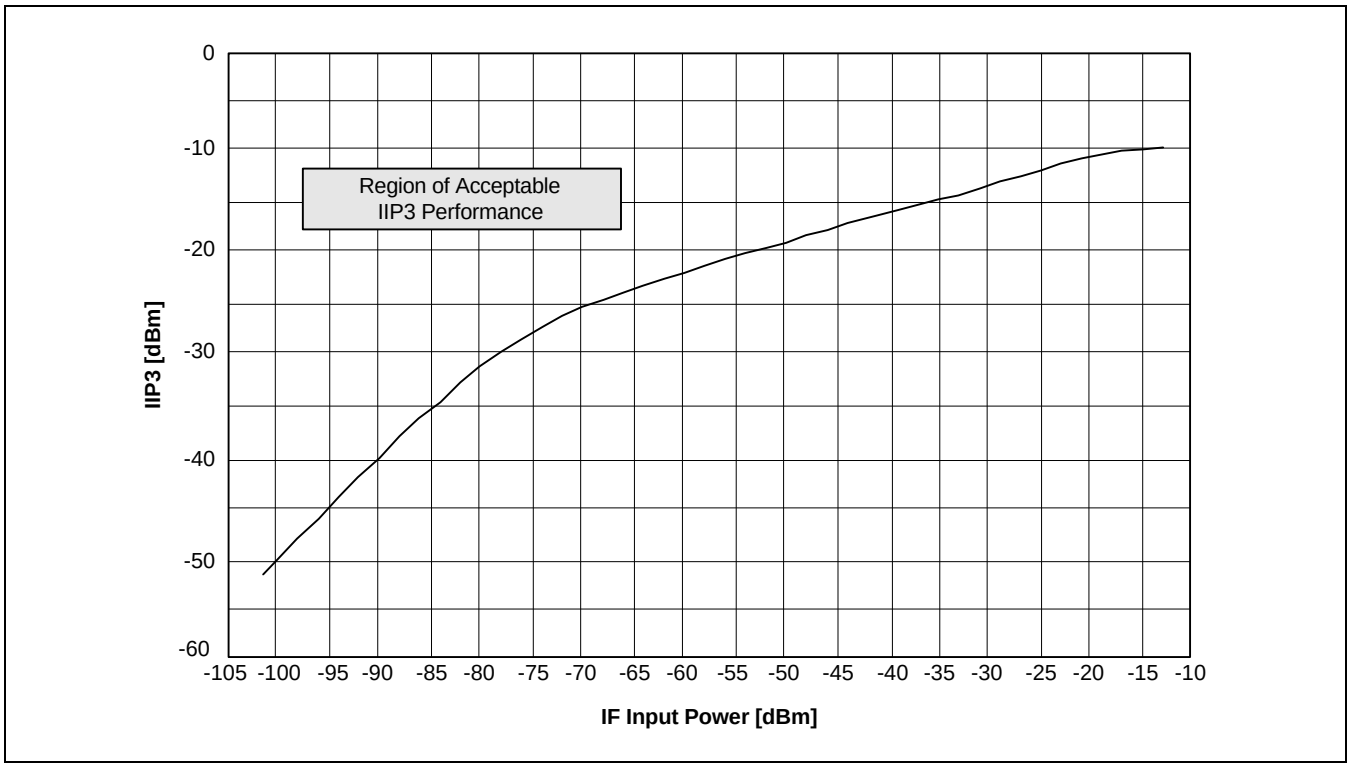


Figure 11. GPS Rx Mode IIP3 Specification

TEST CIRCUIT

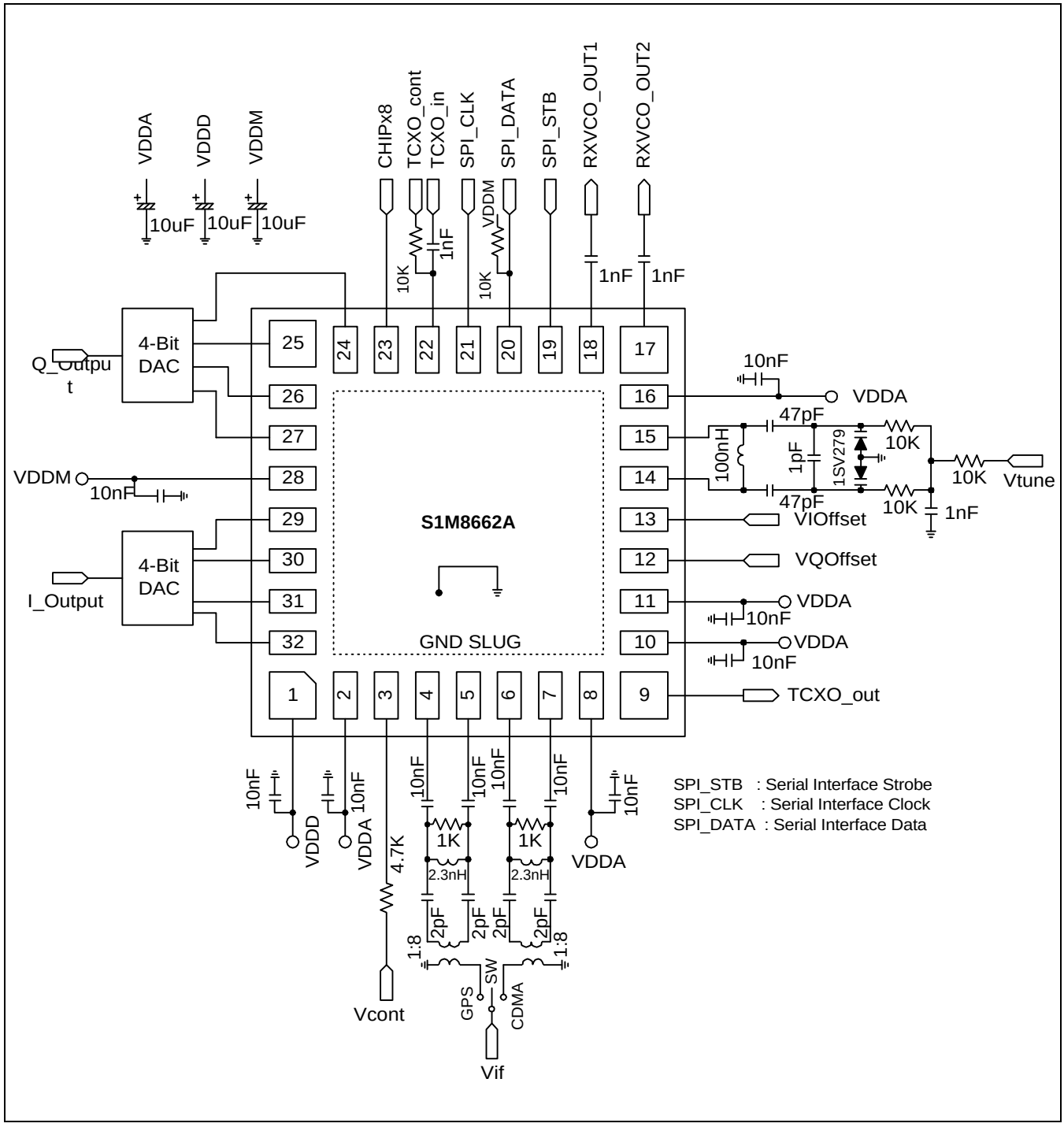


Figure 12. Test Circuit

PACKAGE DIMENSION

32BCC+ Package Outline