EPSON

S1C33L11

32-bit Single Chip Microcomputer

- 32-bit S1C33000 RISC Core
- Multiply Accumulation
- Built-in 16K-byte RAM
- 10-bit ADC
- Built-in LCD Controller
- Built-in USB1.1 Function Controller
- Built-in Camera Interface

■ DESCRIPTION

The S1C33L11 is a Seiko Epson original 32-bit microcomputer that features high speed, low power consumption, and low-voltage operation. The S1C33L11 consists of an S1C33000 32-bit RISC type CPU as its core, peripheral circuits including a bus control unit, DMA controller, interrupt controller, timers, serial interface with FIFO, A/D converter, LCD controller, Camera interface, JPEG codec, USB1.1 function controller, MMC (SPI mode) interface and SmartMedia interface, and also RAM. Three oscillation circuits and two PLLs are also included, supporting advanced operation, power-saving operation, and high-performance realtime clock functions. The S1C33L11 is ideal for portable products that require high-speed data processing. Especially it is suitable for the application processor embedded in cellular phones and PDAs (personal data assistance).

■ FEATURES

- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC Core
- Main clock ..... 50MHz (Max., up to 33MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- LCDC clock ..... 55MHz (Max.)
- USB clock ..... 48MHz (Typ.)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... General-purpose RAM : 16K bytes
  VRAM : 128K bytes
- LCD controller ..... S1D13710 equivalent
  8 to 18-bit color LCD interface
  Supports MD-TFT, D-TFD and TFT panels (up to 2 LCD panels)
  Resolution :
  Programmable (Max. 176 × 240 pixels)
  Color depths :
  A maximum of 64K colors can be simultaneously displayed using a 260K-color pallet (16-bpp mode).
  A maximum of 256 colors can be simultaneously displayed using a 260K-color pallet (8-bpp mode).
  Swivel View (90/180/270-degree hardware rotation of display image), mirror display, picture-in-picture plus, overlay function
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 6 channels and 16 bits × 6 channels
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 4 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
  Ch.0 is selectable between a built-in buffer type (a 4 bytes of receive-data buffer and a 2 bytes of transmit-data buffer) and no buffer type.

- Camera interface ..... 1 channel
  Hardware JPEG codec
  YUV data capture (YUV 4:2:2, 4:2:0), YUV to RGB converter
  Hardware resizer with trimming
- MMC (SPI mode) interface ..... 1 channel
  Supports 1 to 16-bit serial data transfer in master mode.
- SmartMedia interface ..... 1 channel
  Allows direct connection of a SmartMedia.
- USB1.1 function controller ..... Endpoint : EP0, EPa, EPb, EPc, EPd (4 channels)
  FIFO : 1,024 bytes
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits
  I/O port : 51 bits
- Interrupt controller ..... External interrupts : 10 types
  Internal interrupts : 43 types
- External bus interface ..... 26-bit address bus, 16-bit data bus, 7 chip enable pins
  SRAM and Burst ROM may be connected directly.
- Shipping form PFBGA-208pin
- Supply voltage ..... Core voltage : 1.65 to 1.95V (1.8 ±0.15V)
  I/O voltage : 2.70 to 3.30V (3.0 ±0.3V)
  I/O voltage for USB : 3.00 to 3.60V (3.3 ±0.3V)
- Power consumption ..... SLEEP state : 18µW Typ.
  HALT state : 24mW Typ.
  (50MHz, LCDC and USB not included)
  Run state : 50mW Typ.*1
  (50MHz, LCDC and USB not included)
  LCD controller
  - Camera and LCD I/F : 22mW Typ.
    (50MHz, V_{DD}, LCDC block only)
  - Camera, LCD I/F and JPEG : 60mW Typ.
    (50MHz, V_{DD}, LCDC block only)

  USB controller
  - Idle state : 13mW Typ.
    (V_{DD}, USB block only)

*1: The values of power consumption during execution were measured when a test program that consisted of 55% load instructions, 23% arithmetic operation instructions, 1% mac instruction, 12% branch instructions and 9% ext instruction was being continuously executed.

■ BLOCK DIAGRAM

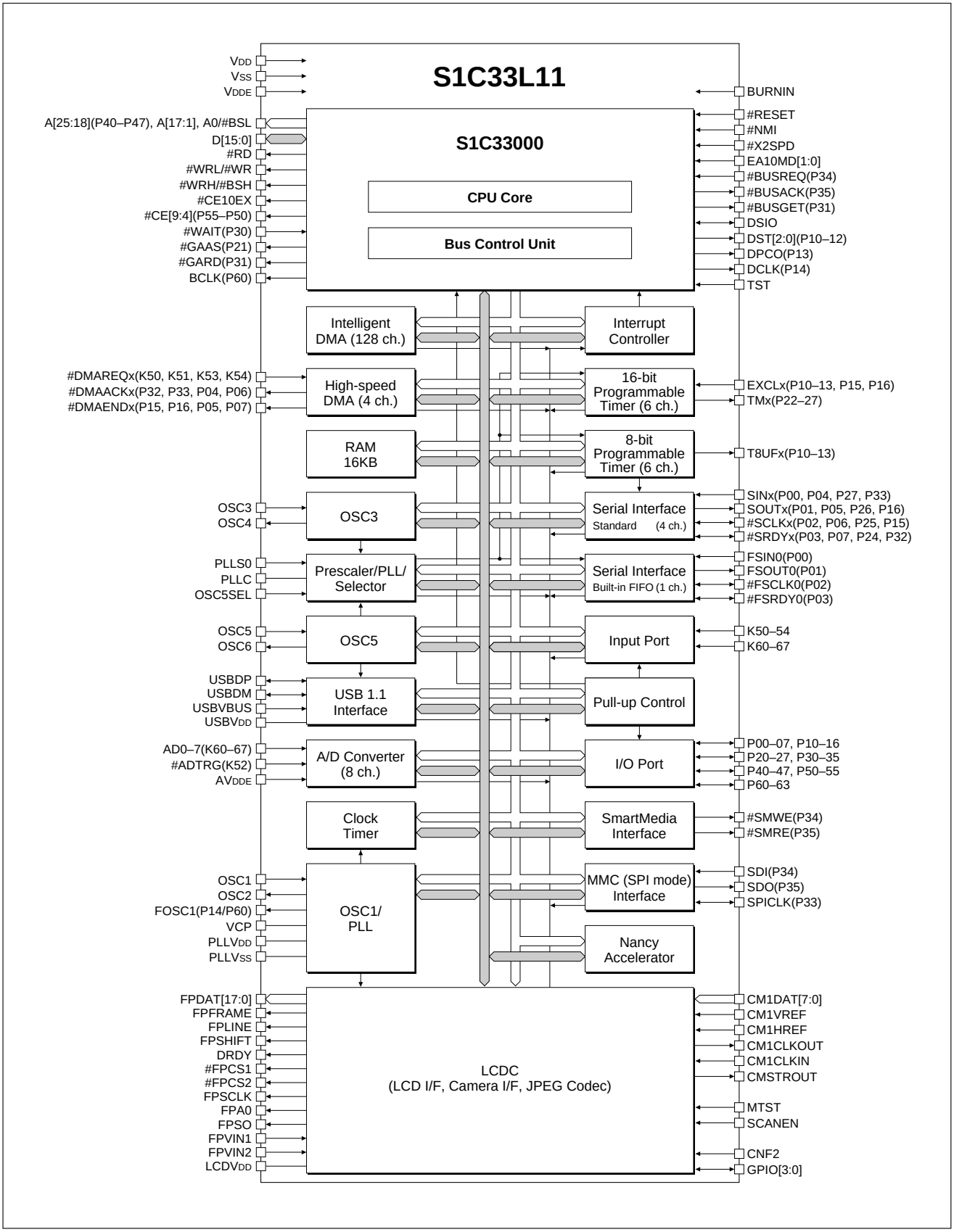
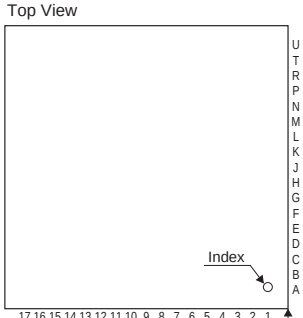


Fig. 1 S1C33L11 Functional Block Diagram

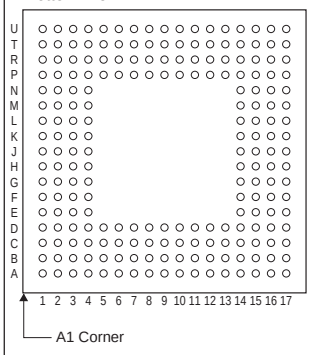
■ PIN LAYOUT

PFBGA-208pin

Top View



Bottom View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
U	N.C.	**FPDAT16**	**FPDAT17**	**GPIO0**	**GPIO3**	**P05** (SOUT1/ #DMAEND2)	**P21** (#DWE/ #GAAS)	**OSC3**	**OSC4**	**PLLC**	**VDDE**	**OSC2**	**OSC1**	**PLLVSS**	**VCP**	**PLLVDD**	N.C.
T	**FPDAT11**	**FPDAT12**	**FPDAT15**	**CNF2**	**VDD**	**P03** (#SRDY0/ #FSRDY0)	**P01** (SOUT0/ FSOUT0)	**P00** (SIN0/ FSIN0)	**VSS**	**EA10MD1**	**VSS**	**P61**	**VDD**	**MTST**	**BURNIN**	**VSS**	**USBDP**
R	**FPDAT9**	**FPDAT13**	**FPDAT14**	**GPIO1**	**P07** (#SRDY1/ #DMAEND3)	**P04** (SIN1/ #DMAACK2)	**P20** (#DRD)	**#RESET**	**PLLS0**	**P23** (TM1)	**SCANEN**	**P26** (TM4/SOUT2)	**P27** (TM5/SIN2)	**TST**	**K50** (#DMAREQ0)	**USBVDD**	**USBDM**
P	**FPDAT8**	**VSS**	**FPDAT10**	**LCDVDD**	**GPIO2**	**P06** (#SCLK1/ #DMAACK3)	**P02** (#SCLK0/ #FSCLK0)	**P22** (TM0)	**EA10MD0**	**#NMI**	**P24** (TM2/#SRDY2)	**P25** (TM3/ #SCLK2)	**P62**	**K51** (#DMAREQ1)	**K53** (#DMAREQ2)	**K52** (#ADTRG)	**USBVBUS**
N	**FPDAT6**	**FPDAT4**	**FPDAT5**	**FPDAT7**										**K54** (#DMAREQ3)	**VDD**	**#CE10EX** (#CE9&10EX)	**VDDE**
M	**FPDAT3**	**VSS**	**FPDAT1**	**FPDAT2**										**#CE8** (#RAS1/ #CE14/ #RAS3/P54)	**#CE7** (#RAS0/ #CE13/ #RAS2/P53)	**OSC5SEL**	**#CE9** (#CE17/ #CE17&18/ P55)
L	**FPDAT0**	**#FPCS1**	**#FPCS2**	**FPFRAME**										**#X2SPD**	**VSS**	**P63**	**OSC5**
K	**DRDY**	**FPSHIFT**	**LCDVDD**	**FPSCLK**										**#CE4** (#CE11/ #CE11&12/ P50)	**#CE6** (#CE7&8/P52)	**#CE5** (#CE15/ #CE15&16/ P51)	**OSC6**
J	**FPSO**	**FPLINE**	**VSS**	**FPA0**										**#WRH** (#BSH)	**#RD**	**#WRL** (#WR/#WE)	**VDD**
H	**CM1CLKOUT**	**VDD**	**CMSTROUT**	**VSS**										**D0**	**D3**	**VDDE**	**BCLK** (P60/FOSC1)
G	**CM1HREF**	**FPVIN2**	**FPVIN1**	**CM1CLKIN**										**VDD**	**D4**	**D1**	**D2**
F	**LCDVDD**	**CM1VREF**	**CM1DAT7**	**CM1DAT6**										**VSS**	**D7**	**D5**	**D6**
E	**CM1DAT4**	**CM1DAT5**	**VSS**	**VSS**										**VDDE**	**D13**	**D9**	**D8**
D	**CM1DAT2**	**CM1DAT3**	**VDD**	**P15** (EXCL4/ #DMAEND0/ #SCLK3)	**DSIO**	**VDD**	**AVDDE**	**VSS**	**P30** (#WAIT/ #CE4&5)	**A23** (P42)	**A20** (P45)	**A17**	**A12**	**A10**	**A1**	**D10**	**D11**
C	**CM1DAT1**	**CM1DAT0**	**DST1** (P11/EXCL1/ T8UF1)	**VDDE**	**DPCO** (P13/EXCL3/ T8UF3)	**P32** (#DMAACK0/ #SRDY3)	**K64** (AD4)	**K61** (AD1)	**#HCAS** (P40/A25)	**A21** (P44)	**A18** (P47)	**A16**	**A11**	**A9**	**A7**	**D15**	**D12**
B	**P16** (EXCL5/ #DMAEND1/ SOUT3)	**DST0** (P10/EXCL0/ T8UF0)	**DCLK** (P14/FOSC1)	**P34** (#BUSREQ/ #CE6/#SMWE/ SDI)	**P33** (#DMAACK1/ SIN3/SPICLK)	**K65** (AD5)	**K63** (AD3)	**K60** (AD0)	**#LCAS** (P41/A24)	**VDD**	**VDDE**	**A14**	**A8**	**VSS**	**A4**	**A0** (#BSL)	**D14**
A	N.C.	**DST2** (P12/EXCL2/ T8UF2)	**VSS**	**P35** (#BUSACK/ #SMRE/SDO)	**P31** (#BUSGET/ #GARD)	**K67** (AD7)	**K66** (AD6)	**K62** (AD2)	**A22** (P43)	**A19** (P46)	**A15**	**A13**	**A6**	**A5**	**A3**	**A2**	N.C.

Bold: The terminal (signal) name of a default setup.

Fig. 2 Pin Layout Diagram (PFBGA-208pin)

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION
IC Marketing & Engineering Group

ED International Marketing Department
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5117

■ EPSON Electronic Devices Website
http://www.epsondevice.com

Document code: 404625402
First issue July, 2003
Printed November, 2003 in Japan Ⓛ