Contents

CMOS 4-bit
1-chip MICROCOMPUTER

S-1462AF/14L62AF

The S-1462AF/14L62AF 4-bit microcomputer integrates 10-bit programmable counter, watchdog timer, and 8-bit programmable timer on one chip. Driven by batteries, this microcomputer is ideal for compact portable equipment.
S-14L62AF is low voltage operating version of S-1462AF.

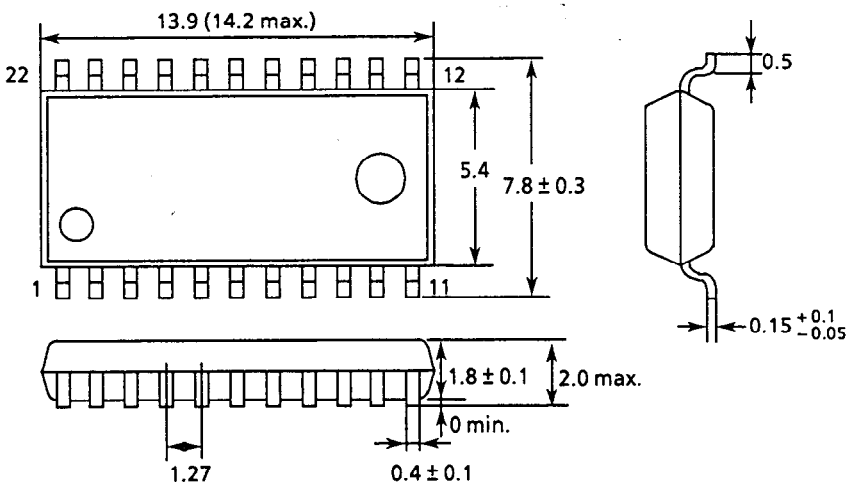
■ Feature

- Si gate CMOS process
- Low power consumption
- Single power supply: 2.2 V min.(for S-1462AF) , 1.2 V min.(for S-14L62AF)
- High-speed operation: 1 MHz max.
- ROM: 2 K×16 bits
- RAM: 128×4 bits
- 14 I/O lines
- 2 timers: timer, programmable countar
- Built-in watchdog timer
- Interrupt function: Two (internal)
- Standby function
- Instruction execution time: 4.0 μs /1 MHz
- Instruction: 35 basic instruction sets (166 if addressing modes are included)
  16-level subroutine nesting
- 22-pin SOP (terminal distance: 1.27 mm)

■ Applications

- Presettable remote controller
- Compact portable equipment, others

■ Dimensions (22-pin SOP)



Unit : mm

Figure 1

■ Pin Assignments

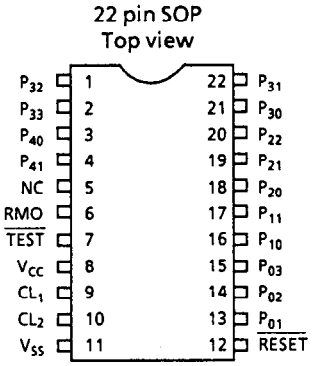


Figure 2

■ Terminal Functions

Table 1

Name	I/O	Functions
V_{SS}	—	GND potential terminal
V_{CC}	—	Positive power supply
$\overline{TEST}$	Input	Test input terminal (built-in pull-up resirtor)
$\overline{RESET}$	Input	Reset input terminal (built-in pull-up resistor)
CL_1	—	Ceramic oscillator connection terminal for system clock oscillation, external clock input
CL_2	—	Ceramia osaillator connection terminal for system clock oscillation
RMO	Output	Remote control signal output terminal
P_{01} to P_{03}	I/O	Port 0 input/output pins, whose directions are selected in bit units (pull-up resistor or Nch opendrain can be selected by mask option)
P_{10}, P_{11}	Input	Port 1 input pins (built-in pull-up resistor)
P_{20} to P_{22}	Input	Port 2 input pins (built-in pull-up resistor)
P_{30} to P_{33}	Output	Port 3 output pins (Nch opendrain output can be selected by mask option)
P_{40}, P_{41}	Output	Port 4 output pins (Nch opendrain output can be selected by mask option)

■ Block Diagram

The S-1462/L62AF blocks connect with a 4-bit data bus (DB), 4-bit address bus (AB), 4-bit RAM address bus (RA), and 12-bit operation bus (OB).

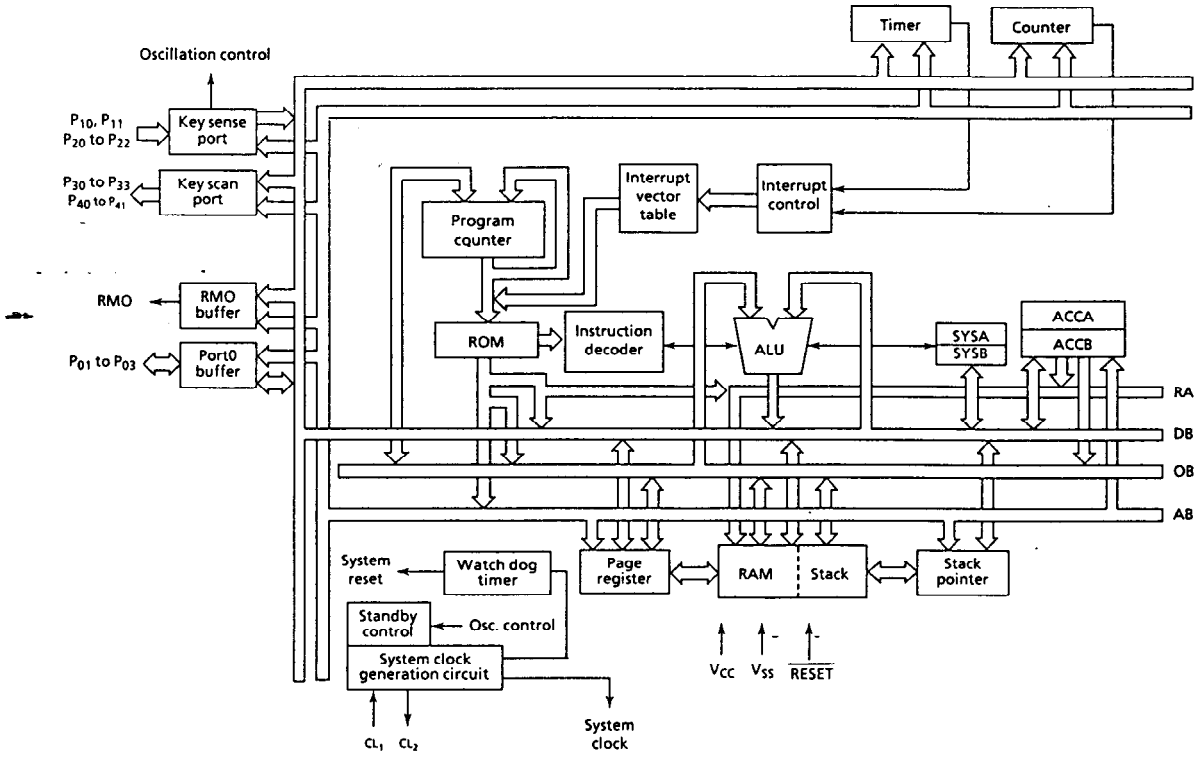


Figure 3

■ Absolute Maximum Ratings

Table 2

Item	Symbol	Conditions	Rating	Unit
Storage temperature	T_{stg}		-40 to + 125	°C
Operating temperature	T_{opr}		-10 to + 70	°C
Power supply voltage	V_{CC}	Ta = 25°C S-1462AF	-0.3 to + 7.0	V
Power supply voltage	V_{CC}	Ta = 25°C S-14L62AF	-0.3 to + 4.0	V
Input voltage	V_{IN}	Ta = 25°C	V_{SS}-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	Ta = 25°C	V_{SS} to V_{CC}	V
Power consumption	P_d	Ta = 25°C	300	mW

■ Recommended Operating Conditions

Table 3

(Ta = -10 °C to + 70 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	System clock: 1 MHz for S-1462AF	2.2	—	6.0	V
Power supply voltage	V_{CC}	System clock: 1 MHz for S-14L62AF	1.2	—	3.6	V
Input voltage	V_{IN}		0	—	V_{CC}	V
System clock frequency	f_{sys}	V_{CC} = 2.2 to 6.0 V for S-1462AF	0.2	—	1.0	MHz
System clock frequency	f_{sys}	V_{CC} = 1.2 to 3.6 V for S-14L62AF	0.2	—	1.0	MHz

■ DC Characteristics

1. S-1462AF (V_{CC} = 3V)

Table 4

(Ta = -10 °C to + 70 °C, V_{CC} = 3 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating current consumption	I_{CCO}	f_O = 1 MHz, No load	—	0.25	0.7	mA
Standby current consumption	I_{CCS}	At OFF mode	—	0.1	2.0	μA
High level input voltage	V_{IH}		0.8 × V_{CC}	—	—	V
Low level input voltage	V_{IL}		—	—	0.2 × V_{CC}	V
High level input leakage current	I_{LH}	All input terminals* V_{IN} = V_{CC}	—	—	1	μA
Low level input leakage current	I_{LL}	Without pull-up resistor, P_{01} to P_{03}, V_{IN} = V_{SS}	-1	—	—	μA
High level input current	I_{IH}	$\overline{RESET}$, V_{IN} = V_{CC}-0.3 V	-9	—	-0.9	μA
Low level input current 1	I_{IL1}	With pull-up resistor, P_{01} to P_{03}, P_{10}, P_{11}, P_{20} to P_{22}, V_{IN} = V_{SS}	-90	-30	-10	μA
Low level input current 2	I_{IL2}	$\overline{RESET}$, V_{IN} = V_{SS}	-6	-2	-0.6	μA
Low level input current 3	I_{IL3}	$\overline{TEST}$, V_{IN} = V_{SS}	-30	-10	-3	μA
High level output current 1	I_{OH1}	RMO, V_{OUT} = 2.1 V	—	—	-5.0	mA
High level output current 2	I_{OH2}	P_{01} to P_{03}, P_{30} to P_{33}, P_{40}, P_{41}, V_{OUT} = 2.6 V	—	—	-100	μA
Low level output current 1	I_{OL1}	RMO, V_{OUT} = 0.4 V	250	—	—	μA
Low level output current 2	I_{OL2}	P_{01} to P_{03}, P_{30} to P_{33}, P_{40}, P_{41}, V_{OUT} = 0.4 V	1.0	—	—	mA
Schmitt hysteresis width	V_{WD}		—	1.0	—	V

* $\overline{TEST}$, $\overline{RESET}$, P_{01} to P_{03}, P_{10}, P_{11}, P_{20} to P_{22}

2. S-1462AF (VCC = 5V)

Table 5

(Ta = -10 °C to + 70 °C, V_{CC} = 5 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating current consumption	I_{CCO}	f_O = 1 MHz, No load	—	0.6	1.2	mA
Standby current consumption	I_{CCS}	At OFF mode	—	0.1	5.0	μA
High level input voltage	V_{IH}		0.8 × V_{CC}	—	—	V
Low level input voltage	V_{IL}		—	—	0.2 × V_{CC}	V
High level input leakage current	I_{LH}	All input terminals* V_{IN} = V_{CC}	—	—	1	μA
Low level input leakage current	I_{LL}	Without pull-up resistor, P_{01} to P_{03}, V_{IN} = V_{SS}	-1	—	—	μA
High level input current	I_{IH}	$\overline{RESET}$, V_{IN} = V_{CC}-0.3 V	-15	—	-1.5	μA
Low level input current 1	I_{IL1}	With pull-up resistor, P_{01} to P_{03}, P_{10}, P_{11}, P_{20} to P_{22}, V_{IN} = V_{SS}	-230	-90	-30	μA
Low level input current 2	I_{IL2}	$\overline{RESET}$, V_{IN} = V_{SS}	-15	-6	-2.4	μA
Low level input current 3	I_{IL3}	$\overline{TEST}$, V_{IN} = V_{SS}	-75	-30	-12	μA
High level output current 1	I_{OH1}	RMO, V_{OUT} = 4.1 V	—	—	-7	mA
High level output current 2	I_{OH2}	P_{01} to P_{03}, P_{30} to P_{33}, P_{40}, P_{41}, V_{OUT} = 4.6 V	—	—	-250	μA
Low level output current 1	I_{OL1}	RMO, V_{OUT} = 0.4 V	450	—	—	μA
Low level output current 2	I_{OL2}	P_{01} to P_{03}, P_{30} to P_{33}, P_{40}, P_{41}, V_{OUT} = 0.4 V	1.5	—	—	mA
Schmitt hysteresis width	V_{WD}		—	2.2	—	V

* $\overline{TEST}$, $\overline{RESET}$, P_{01} to P_{03}, P_{10}, P_{11}, P_{20} to P_{22}

3. S-14L62AF (V_{CC} = 1.5 V)

Table 6

(T_a = -10 °C to + 70 °C, V_{CC} = 1.5 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating current consumption	I_{CCO}	f_O = 1 MHz, No load	—	0.1	0.3	mA
Standby current consumption	I_{CCS}	At OFF mode	—	1	10	μA
High level input voltage	V_{IH}		0.8 × V_{CC}	—	—	V
Low level input voltage	V_{IL}		—	—	0.2 × V_{CC}	V
High level input leakage current	I_{LH}	All input terminals* V_{IN} = V_{CC}	—	—	1	μA
Low level input leakage current	I_{LL}	Without pull-up resistor, P_{01} to P_{03}, V_{IN} = V_{SS}	-1	—	—	μA
High level input current	I_{IH}	$\overline{RESET}$, V_{IN} = V_{CC}-0.3 V	-4	—	-1	μA
Low level input current 1	I_{IL1}	With pull-up resistor, P_{01} to P_{03}, P_{10}, P_{11}, P_{20} to P_{22}, V_{IN} = V_{SS}	-30	-10	-3	μA
Low level input current 2	I_{IL2}	$\overline{RESET}$, V_{IN} = V_{SS}	-2	-0.6	-0.2	μA
Low level input current 3	I_{IL3}	$\overline{TEST}$, V_{IN} = V_{SS}	-8	-2	-0.5	μA
High level output current 1	I_{OH1}	RMO, V_{OUT} = 1.1 V	—	—	-2	mA
High level output current 2	I_{OH2}	P_{01} to P_{03}, P_{30} to P_{33}, P_{40}, P_{41}, V_{OUT} = 1.1 V	—	—	-100	μA
Low level output current 1	I_{OL1}	RMO, V_{OUT} = 0.4 V	200	—	—	μA
Low level output current 2	I_{OL2}	P_{01} to P_{03}, P_{30} to P_{33}, P_{40}, P_{41}, V_{OUT} = 0.4 V	0.5	—	—	mA
Schmitt hysteresis width	V_{WD}		—	0.4	—	V

* $\overline{TEST}$, $\overline{RESET}$, P_{01} to P_{03}, P_{10}, P_{11}, P_{20} to P_{22}

4. S-14L62AF (V_{CC} = 3 V)

Table 7

(T_a = -10 °C to + 70 °C, V_{CC} = 3 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating current consumption	I_{CCO}	f_O = 1 MHz, No load	—	0.5	1.0	mA
Standby current consumption	I_{CCS}	At OFF mode	—	1	15	μA
High level input voltage	V_{IH}		0.8 × V_{CC}	—	—	V
Low level input voltage	V_{IL}		—	—	0.2 × V_{CC}	V
High level input leakage current	I_{LH}	All input terminals* V_{IN} = V_{CC}	—	—	1	μA
Low level input leakage current	I_{LL}	Without pull-up resistor, P_{01} to P_{03}, V_{IN} = V_{SS}	-1	—	—	μA
High level input current	I_{IH}	$\overline{RESET}$, V_{IN} = V_{CC}-0.3 V	-8	—	-2	μA
Low level input current 1	I_{IL1}	With pull-up resistor, P_{01} to P_{03}, P_{10}, P_{11}, P_{20} to P_{22}, V_{IN} = V_{SS}	-120	-50	-20	μA
Low level input current 2	I_{IL2}	$\overline{RESET}$, V_{IN} = V_{SS}	-10	-4	-1.5	μA
Low level input current 3	I_{IL3}	$\overline{TEST}$, V_{IN} = V_{SS}	-40	-16	-6	μA
High level output current 1	I_{OH1}	RMO, V_{OUT} = 2.6 V	—	—	-3	mA
High level output current 2	I_{OH2}	P_{01} to P_{03}, P_{30} to P_{33}, P_{40}, P_{41}, V_{OUT} = 2.6 V	—	—	-200	μA
Low level output current 1	I_{OL1}	RMO, V_{OUT} = 0.4 V	400	—	—	μA
Low level output current 2	I_{OL2}	P_{01} to P_{03}, P_{30} to P_{33}, P_{40}, P_{41}, V_{OUT} = 0.4 V	1.0	—	—	mA
Schmitt hysteresis width	V_{WD}		—	1.0	—	V

* $\overline{TEST}$, $\overline{RESET}$, P_{01} to P_{03}, P_{10}, P_{11}, P_{20} to P_{22}

■ Instructions

1. Instructions are 16-bit length, and executed in a single instruction cycle (4 clocks).
2. The S-1462AF/14L62AF has 6 addressing modes.
   1) Direct addressing mode
   2) Relative addressing mode
   3) Immediate addressing mode
   4) Register addressing mode
   5) Accumulator indirect addressing mode
   6) Accumulator indexed addressing mode
3. Number of instructions

Table 8

	Basic	Including addressing modes
Transfer instruction	6	15
Arithmetic operation instruction	9	57
Logical operation instruction	8	66
Branch instruction	7	19
Rotate/shift instruction	2	6
CPU control instruction	3	3
Total	35	166

■ Application Example (S-1462AF)

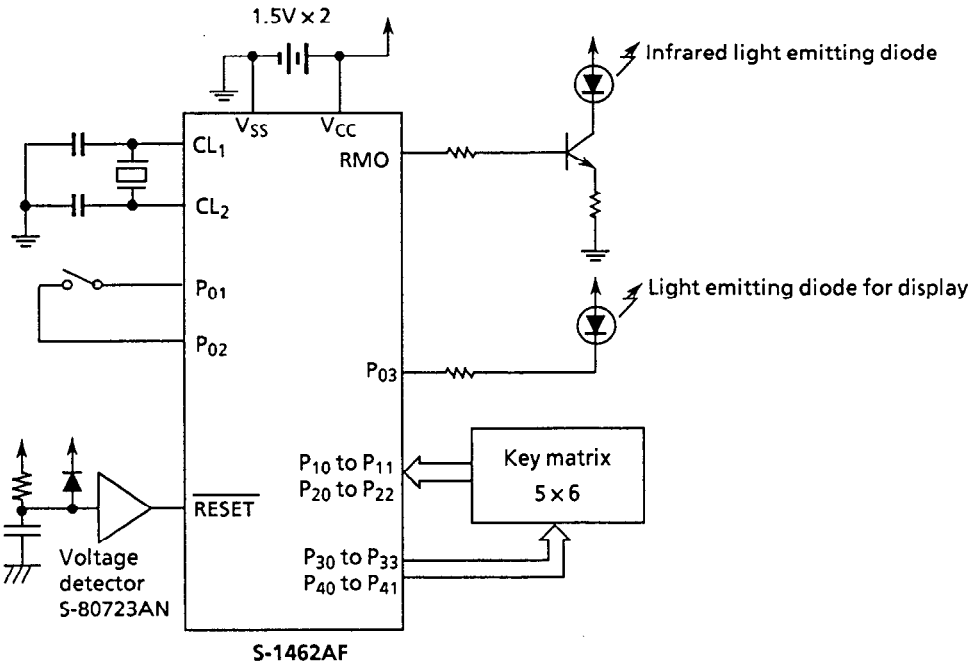


Figure 4