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RTL8192SE-GR

SINGLE-CHIP IEEE 802.11b/g/n 2T2R WLAN CONTROLLER w/PCI EXPRESS INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.1
12 June 2009
Track ID: JATR-1076-21

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/05/14	First release.
1.1	2009/06/12	Revised Table 9 Ordering Information, page 13.

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek RTL8192SE is a highly integrated single-chip MIMO (Multiple In, Multiple Out) Wireless LAN (WLAN) solution for the wireless high throughput 802.11n draft specification. It combines a MAC, a 2T2R capable baseband, and RF in a single chip. The RTL8192SE provides a complete solution for a high throughput performance wireless client.

The RTL8192SE baseband implements Multiple Input, Multiple Output (MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with 2 transmit and 2 receive paths (2T2R) and is compatible with the IEEE 802.11n Draft specification 2.0. Features include two spatial streams transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth. The RTL8192SE also supports explicit sounding packet feedback that helps senders with beamforming capability. With 2 independent RF blocks, the RTL8192SE can perform fast roaming without link interruption.

For legacy compatibility, direct sequence spread spectrum (DSSS), complementary code keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available along with complementary code keying to provide the data rates of 1, 2, 5.5 and 11Mbps with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provides the maximum data rate of 54Mbps and 300Mbps for IEEE 802.11g and 802.11n MIMO OFDM respectively.

The RTL8192SE builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate the severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with maximal-ratio-combine (MRC) applying up to 2 receive paths are implemented. Robust interference detection and suppression are provided to protect against bluetooth, cordless phone, and microwave oven. Receive vector diversity for multi-stream application is implemented for efficient utilization of MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset and timing offset compensations are provided for the radio frequency front-end impairments. Selectable digital transmit and receiver FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8192SE supports fast receiver automatic gain control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain the better performance in the analog portions of the transceiver.

The RTL8192SE MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The RTL8192SE provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 68-pin QFN
- CMOS MAC, Baseband MIMO PHY, and RF in a single chip for IEEE 802.11b/g/n compatible WLAN
- Complete 802.11n MIMO solution for 2.4GHz band
- 2x2 MIMO technology for extended reception robustness and exceptional throughput
- Maximum PHY data rate up to 144.4Mbps using 20MHz bandwidth, 300Mbps using 40MHz bandwidth
- Compatible with 802.11n draft 2.0 specification
- Backward compatible with 802.11b/g devices while operating at 802.11n data rates

Host Interface

- Complies with PCI Express Base Specification Revision 1.1

Standards Supported

- IEEE 802.11e QoS Enhancement (WMM, WMM-SA Client mode)
- IEEE 802.11h TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- Cisco Compatible Extensions (CCX) for WLAN devices

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8192SE to assume multiple MAC identities when used as a wireless bridge
- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

Peripheral Interfaces

- General Purpose Input/Output (8 pins)
- 4-wire EEPROM control interface (93C46)
- Two configurable LED pins
- Configurable Bluetooth Coexistence Interface

PHY Features

- IEEE 802.11n draft 2.0 MIMO OFDM
- Two Transmit and Two Receive path (2T2R)

- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- Sounding packet
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 300Mbps in 802.11n
- OFDM receive diversity with MRC using up to 2 receive paths. Switch diversity used for DSSS/CCK.
- Hardware antenna diversity
- Selectable digital transmit and receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

3. Application Diagram

3.1. Single-Band 11n Application

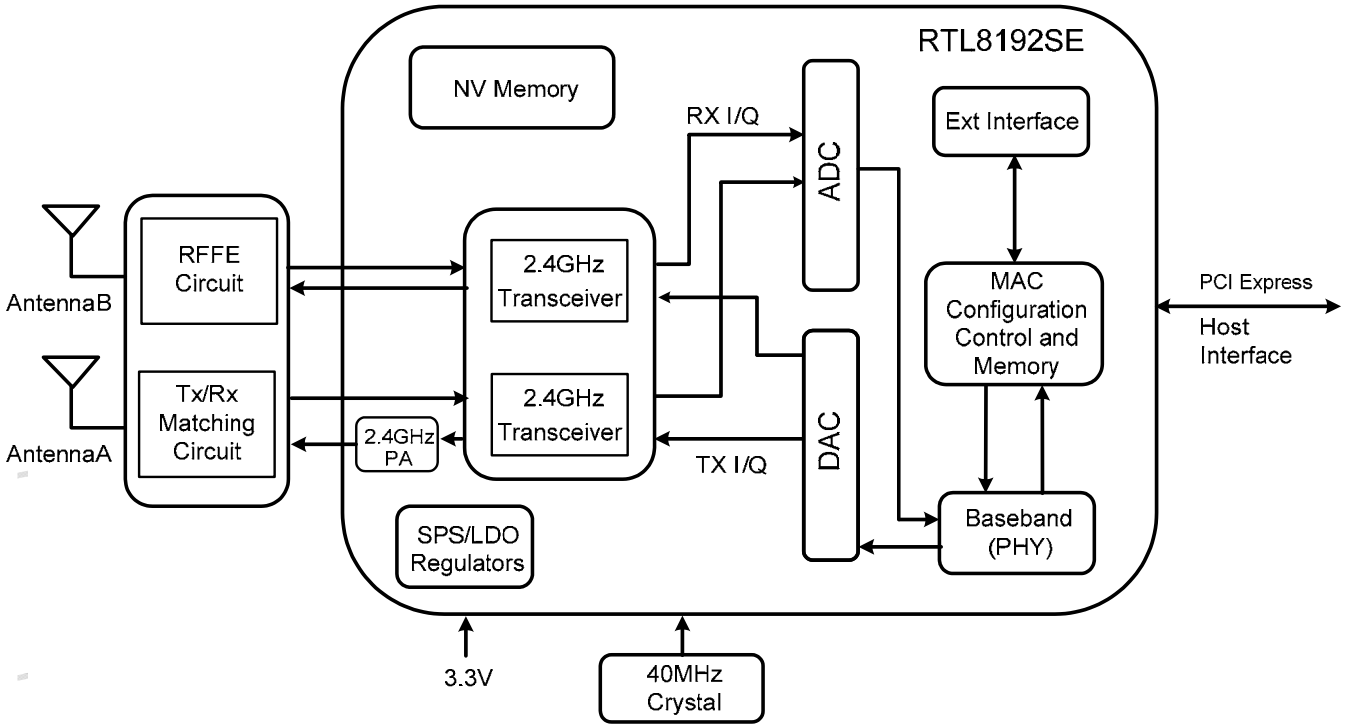


Figure 1. 11n 2x2 MAC/BB/RF Application

4. Pin Assignments

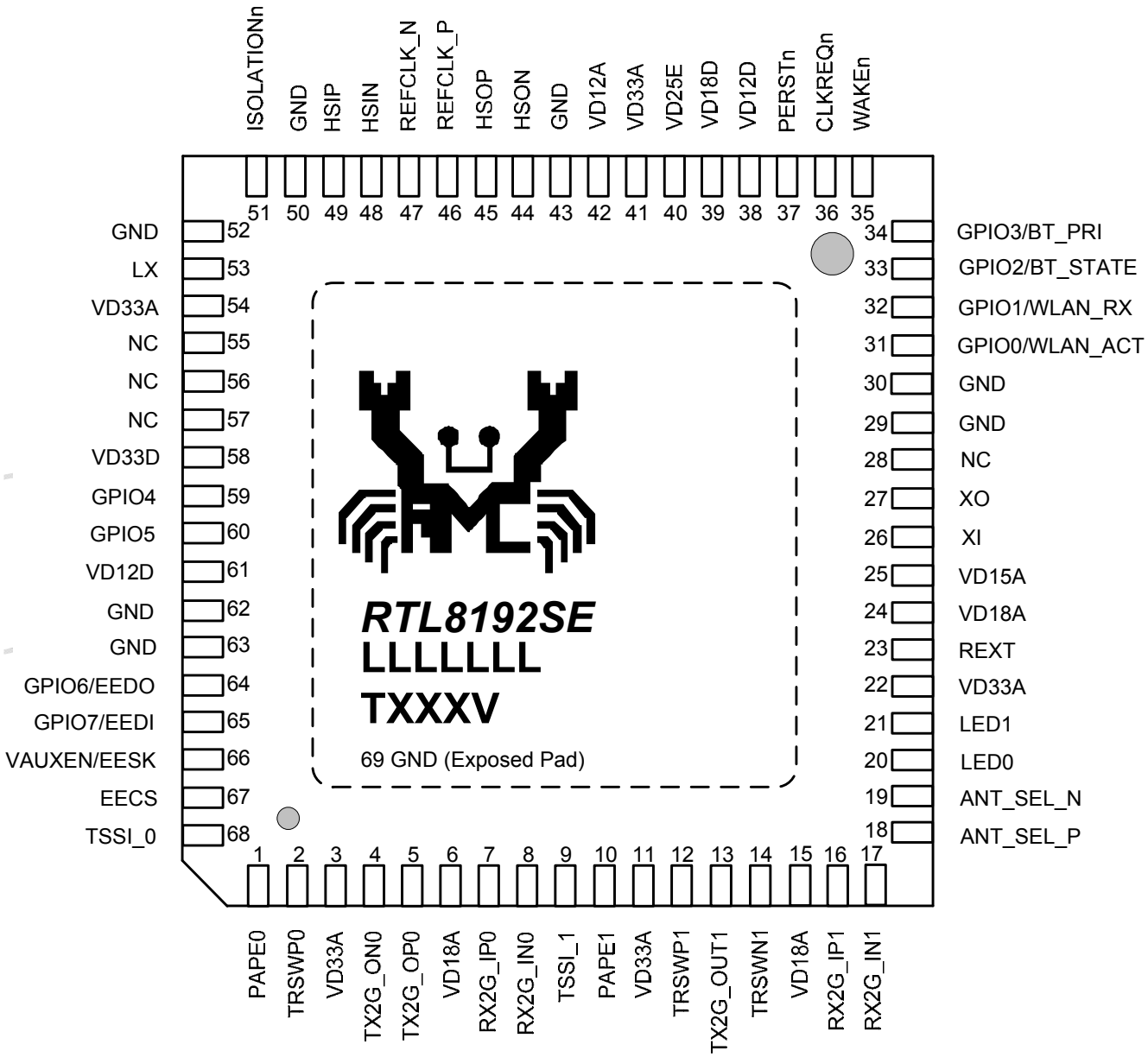


Figure 2. Pin Assignments

4.1. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input

O: Output

T/S: Tri-State bi-directional input/output pin

S/T/S: Sustained Tri-State

O/D: Open Drain

P: Power pin

5.1. PCI Express Transceiver Interface

Table 1. PCI Express Transceiver Interface

Symbol	Type	Pin No	Description
HSIN/HSIP	I	48/49	PCI Express Receive Differential Pair
HSON/HSOP	O	44/45	PCI Express Transmit Differential Pair
REFCLK_P/REFCLK_N	I	46/47	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm
CLKREQn	O	36	Reference Clock Request Signal. This signal is used by the RTL8192SE-GR to request starting of the PCI Express reference clock
WAKEn	O/D	35	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
PERSTn	I	37	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8192SE-GR returns. to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.

5.2. EEPROM Interface

Table 2. EEPROM Interface

Symbol	Type	Pin No	Description
EESK	O	66	EESK in 93C46 Programming or Auto-Load Mode
EEDI	O	65	EEDI in 93C46 Programming or Auto-Load Mode
EEDO	IO	64	EEDO in 93C46 Programming or Auto-Load Mode
EECS	O	67	EEPROM Chip Select 93C46 chip select.

5.3. Power Pins

Table 3. Power Pins

Symbol	Type	Pin No	Description
LX	P	53	Switching Regulator Output
GND	P	29, 30, 43, 50, 52, 62, 63, 69	Regulator GND
VD33A	P	3, 11, 22, 41, 54	VDD 3.3V for Analog
VD18A	P	6, 15, 24	VDD 1.8V for Analog
VD15A	P	25	Analog 1.5V Capacitor
VD25E	P	40	Analog 2.5V Capacitor
VD12A	P	42	VDD 1.2V for Analog
VD12D	P	38, 61	VDD 1.2V for Digital
VD33D	P	58	VDD 3.3V for Digital
VD18D	P	39	VDD 1.8V for Digital
REXT	P	23	For Bandgap and Bias

5.4. RF Interface

Table 4. RTL8192SE-GR RF Interface

Symbol	Type	Pin No	Description
PAPE0	O	1	2.4GHz Transmit Power Amplifier Power Enable
TRSWP0	O	2	Transmit/Receive Path Select 0
TX2G_ON0	O	4	RF TX Positive Signal to Antenna A
TX2G_OP0	O	5	RF TX Negative Signal to Antenna A
RX2G_IP0	O	7	RF RX Positive Signal from Antenna A
RX2G_IN0	O	8	RF RX Negative Signal from Antenna A
TSSI_1	I	9	Input to the Transmit Power A/D Converter for Transmit AGC Control
PAPE1	O	10	2.4GHz Transmit Power Amplifier Power Enable
TRSWP1	O	12	Transmit/Receive Path Select 1
TX2G_OUT1	O	13	RF TX Positive Signal to PA 1
TRSWN1	O	14	Transmit/Receive Path Select 1
RX2G_IP1	I	16	RF RX Positive Signal from Antenna B
RX2G_IN1	I	17	RF RX Negative Signal from Antenna B
ANT_SEL_P	O	18	Antenna Control Positive Signal
ANT_SEL_N	O	19	Antenna Control Negative Signal
TSSI_0	I	68	Transmit Signal Strength Indication from External Power Amplifier

5.5. LED Interface

Table 5. LED Interface

Symbol	Type	Pin No	Description
LED0/LED1	O	20/21	LED Pins (Active Low)

5.6. Clock and Other Pins

Table 6. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	26	40MHz OSC Input. Input of 40MHz Crystal clock reference
XO	O	27	Output of 40MHz Crystal Clock Reference
ISOLATIONn	I	51	This Pin can Externally Shutdown the RTL8192SE (no requirement for Extra Power Switch). This pin can also support the WLAN Radio-off function with host interface remaining connected.
VAUXEN/EESK	I	66	Weakly pull high at power on to indicate the presence of the auxiliary power on the mainboard. Otherwise, this is for EEPROM autoload.
GPIO0/WLAN_ACT	IO	31	General Purpose Input/Output Pin or Bluetooth Coexistence WLAN_ACT Pin. The WLAN_ACT signal indicates when WLAN is either transmitting or receiving in the 2.4GHz ISM band.
GPIO1/WLAN_RX	IO	32	General Purpose Input/Output Pin or Bluetooth Coexistence WLAN_RX Pin. WLAN_RX is an indicator for wireless LAN RX activity.
GPIO2/BT_STATE	IO	33	General Purpose Input/Output Pin or Bluetooth Coexistence BT_STAT Pin. The BTSTAT signal indicates when normal Bluetooth packets are being transmitted or received.
GPIO3/BT_PRI	IO	34	General Purpose Input/Output Pin or Bluetooth Coexistence BT_PRI Pin. The BT_PRI signal indicates when a high priority Bluetooth packet is being transmitted or received.
GPIO4	IO	59	General Purpose Input/Output Pin
GPIO5	IO	60	General Purpose Input/Output Pin
GPIO6/EEDO	IO	64	General Purpose Input/Output Pin or EEPROM Interface EEDO Signal
GPIO7/EEDI	IO	65	General Purpose Input/Output Pin or EEPROM Interface EEDI Signal

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 7. Temperature Limit Ratings

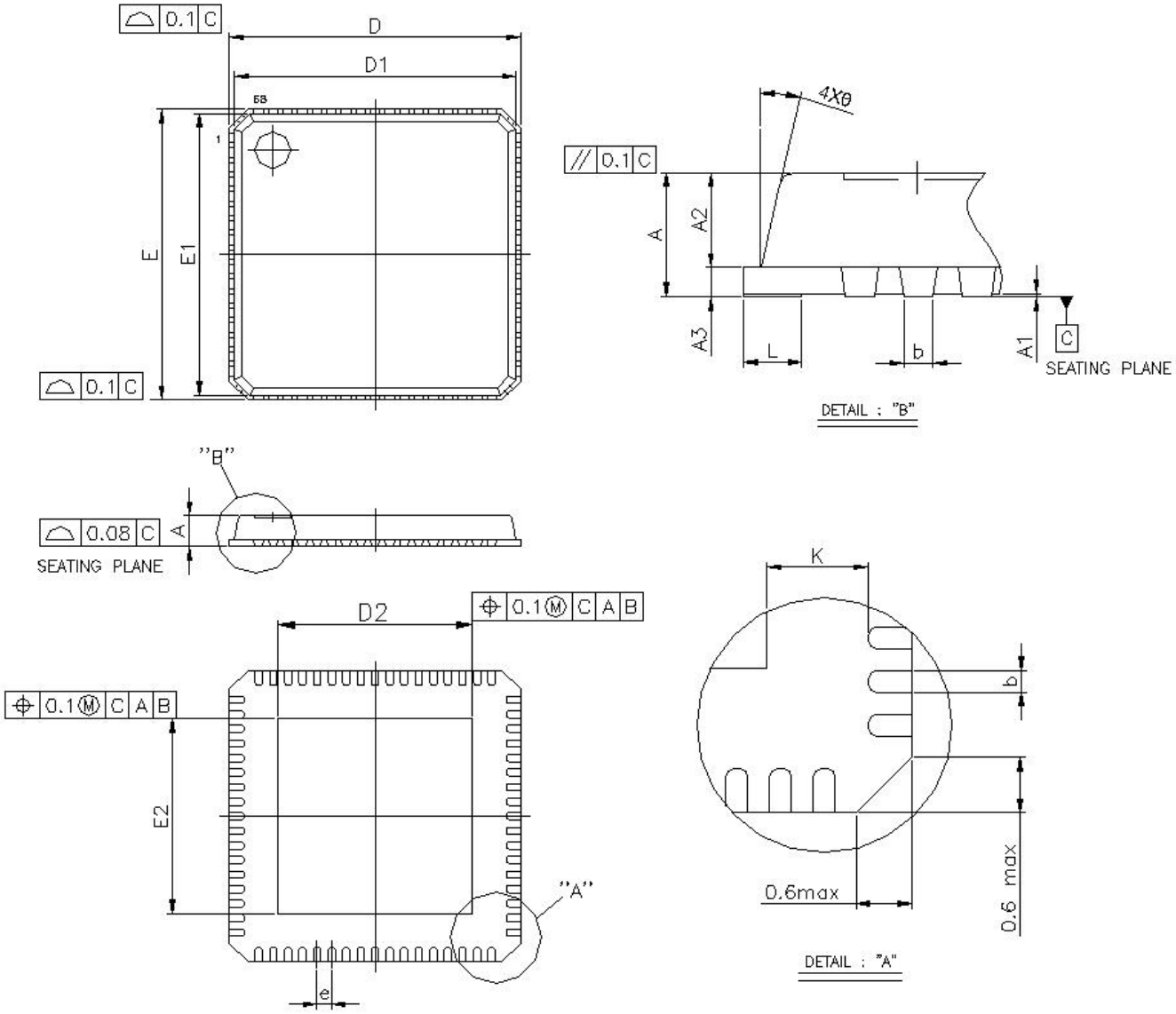
Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

Table 8. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
DVDD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
DVDD18	1.8V Supply Voltage	1.71	1.8	1.89	V
DVDD12	1.2V Core Supply Voltage	1.10	1.2	1.32	V

7. Mechanical Dimensions



7.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	0.55	0.65	0.80	0.022	0.026	0.032
A_3		0.20REF			0.008REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		8.00BSC			0.236BSC	
D_1/E_1		7.75BSC			0.226BSC	
D_2/E_2	5.25	5.5	5.75	0.206	0.216	0.226
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0^o	-	14^o	0^o	-	14^o

Note1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note2: REFERENCE DOCUMENT: JEDEC MO-220.

8. Ordering Information

Table 9. Ordering Information

Part Number	Package	Status
RTL8192SE-GR	QFN-68, 'Green' Package	Mass Production

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com