REALTEK SINGLE CHIP FAST ETHERNET CONTROLLER WITH MII & AUI INTERFACE RTL8130

1. Features:

- 160 pins QFP
- Integrated Fast Ethernet MAC, Physical chip and transceiver in one chip
- All drivers of RTL8130 are compatible to RTL8139A
- 10 Mb/s and 100 Mb/s operation
- Supports 10 Mb/s and 100 Mb/s N-way Auto-negotiation operation
- PCI local bus single-chip Fast Ethernet controller
  - ✧ Compliant to PCI Revision 2.2
  - ✧ Supports PCI clock 16.75MHz-40MHz
  - ✧ Supports PCI target fast back-to-back transaction
  - ✧ Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of RTL8130's operational registers
  - ✧ Supports ACPI, PCI power management
- Support AUI & MII interfaces
- Medium auto-detect priority: UTP > MII in UTP+MII application or UTP > AUI in UTP+AUI application. UTP+MII+AUI application is not supported.
- Auto detect the status of cable connection
- Support redundant link capability by UTP+MII, or UTP+AUI for fault-tolerant applications
- Supports up to 128K bytes Boot ROM interface for both EPROM and Flash memory
- Supports 50MHz OSC as the internal clock source. The frequency deviation of either crystal or OSC must be within 50 PPM.
- Supports Wake-On-LAN function and remote wake-up (Magic packet, LinkChg and Microsoft® wake-up frame)
- Supports 4 Wake-On-LAN (WOL) signals (active high, active low, positive pulse, and negative pulse)
- Supports auxiliary power-on internal reset, to be ready for remote wake-up when main power still remains off

- Includes a programmable, PCI burst size and early tx/rx threshold.
- Supports a 32-bit general-purpose timer with the external PCI clock as clock source, to generate timer-interrupt
- Contains two large (2Kbyte) independent receive and transmit FIFO's
- Uses 93C46 (64*16-bit EEPROM) to store resource configuration, ID parameter.
- Supports LED pins for various network activity indications
- Supports digital and analog loopback capability on both ports
- Half/Full duplex capability
- Supports Full Duplex Flow Control (IEEE 802.3x)

2. General Description

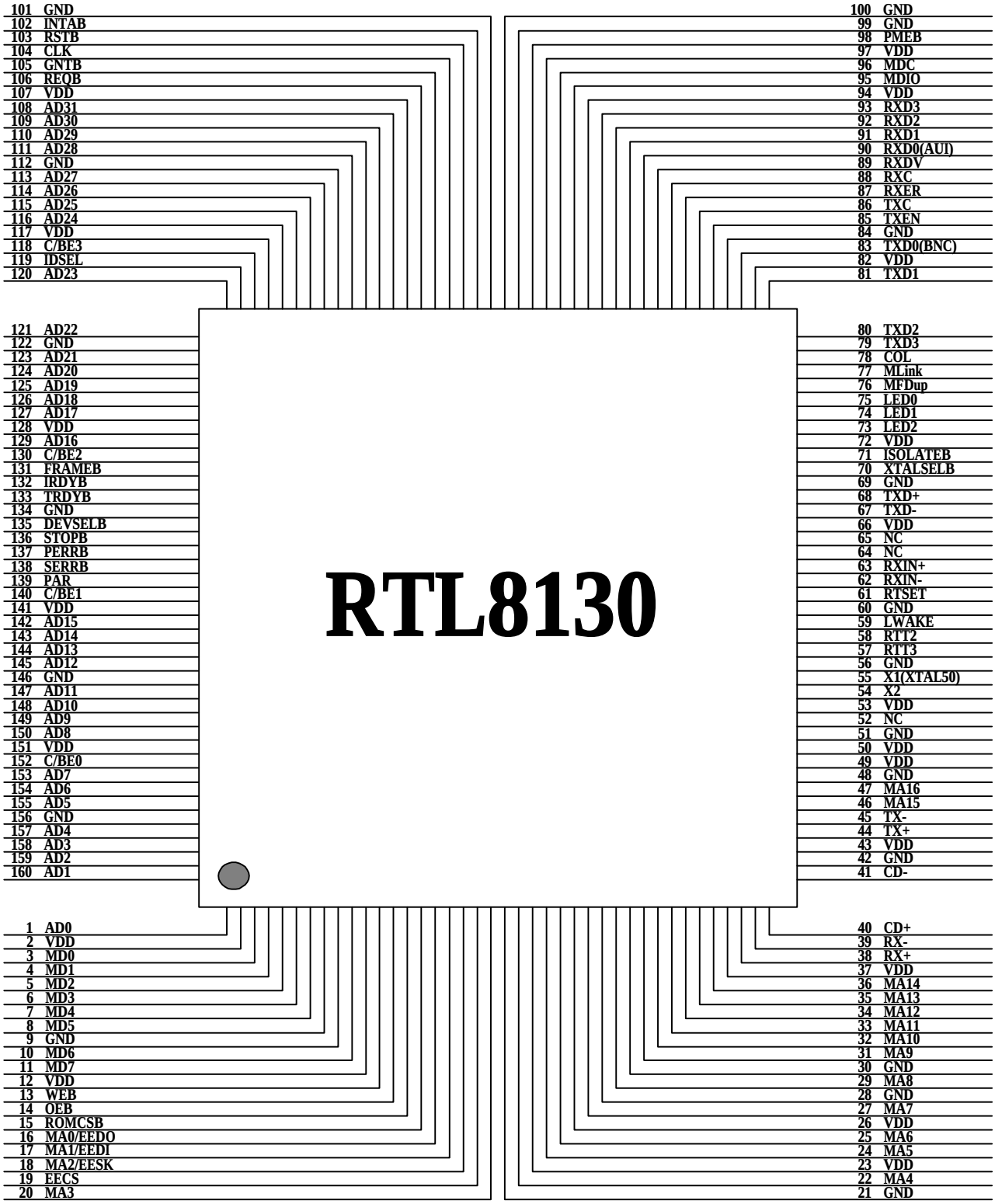
The Realtek RTL8130 is a highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that is capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management.

Besides the ACPI feature, the RTL8130 also supports remote wake-up (including Magic Packet, LinkChg, and Microsoft® wake-up frame) in both ACPI and APM environments. Especially, the RTL8130 is capable of performing internal reset whenever there is (auxiliary) power applied to. Once the auxiliary power is on whereas the main power still remains off, the RTL8130 is ready and is waiting for the Magic packet or Link Change to wake the system up. Also, the LWAKE pin provides 4 different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8130 LWAKE pin satisfies all kinds of motherboards with Wake-On-LAN (WOL) function.

Furthermore, RTL8130 supports MII and AUI interfaces which RTL8139A/B don't. By AUI interface, you can make a Combo LAN adapter that supports 100/10Base-T and 10Base-2/5 medium. By MII interface, you can make a LAN adapter that supports Optical fiber network or you also can use RTL8130 to achieve a cable fault tolerant application for network critical environment.

The RTL8130 keeps network maintenance cost low and eliminates usage barriers. It is the easiest way to upgrade a network from 10 to 100Mbps. It also supports full-duplex operation, making possible 200Mbps of bandwidth at no additional cost. The RTL8130 is highly integrated and requires no "glue" logic or external memory. It includes an interface for a boot ROM and can be used in diskless workstations, providing maximum network security and ease of management.

3. Pin Assignment



4. Pin Descriptions

4.1 Power Management/Isolation Interface(3 pins)

Symbol	Type	Pin No	Description
PMEB (PME#)	O/D	98	Power Management Enable: Open drain, active low. Used by the RTL8130 to request a change in its current power management state and/or to indicate that a power management event has occurred.
ISOLATEB (ISOLATE#)	I	71	Isolate pin: Active low. Used to isolate RTL8130 from the PCI bus. The RTL8130 does not drive its PCI outputs (excluding PME#) and does not sample its PCI input (including RST# and PCICLK) as long as Isolate pin is asserted.
LWAKE	O	59	LAN WAKE-UP pin: Active high. Used to inform the motherboard to execute wake-up process in LAN WAKE-UP mode. (Magic packet only)

4.2 PCI Interface(50 pins)

Symbol	Type	Pin No	Description
AD31-0	T/S	108-111, 113-116, 120-121, 123-127, 129, 142-145, 147-150, 153-155, 157-160, 1	PCI address and data multiplexed pins
C/BE3-0	T/S	118, 130, 140, 152	PCI bus command and byte enables multiplexed pins
CLK	I	104	Clock provides timing for all transactions on PCI and is input to PCI device.
DEVSELB	S/T/S	135	Device Select: When actively driven, indicates the RTL8130 has decoded its address as the target of the current access, As an input, DEVSELB indicates whether any device on the bus has been selected.
FRAMEB	S/T/S	131	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAMEB is asserted to indicated a bus transaction is beginning. While FRAMEB is asserted, data transfers continue. When FRAMEB is deasserted, the transaction is in the final data phase.
GNTB	I	105	Grant: This signal is asserted low to indicate the RTL8130 that has been granted to access to the bus.
REQB	T/S	106	Request: The RTL8130 will assert this signal low to request to access to the bus.
IDSEL	I	119	Initialization Device Select is used as a chip select during configuration read and write transactions.
INTAB	O/D	102	INTAB is used to request an interrupt.
IRDYB	S/T/S	132	Initiator Ready indicates the initiating agent's ability to complete the current data phase of the transaction.
TRDYB	S/T/S	133	Target Ready indicates the target agent's ability to complete the current phase of the transaction.
PAR	T/S	139	Parity is even parity across AD31-0 and C/BE3-0.
PERRB	S/T/S	137	Parity Error: When the RTL8130 is in bus master access mode and a parity error is detected, the RTL8130 asserts both SERR bit in ISR and Configuration Space command bit 8 (SERRB enable). Next, it completes the current data burst transaction, then stops operation and

			resets itself. After the host clears the system error, the RTL8130 continues its operation. When the RTL8130 is the bus target and a parity error is detected, the RTL8130 asserts this PERRB pin.
SERRB	O/D	138	System Error: If an address parity error is detected and Configuration Space Status register bit 15 (detected parity error) is enabled, RTL8130 asserts both SERRB pin and bit 14 of Status register in Configuration Space.
STOPB	S/T/S	136	Stop: Indicates the current target is requesting the master to stop the current transaction.
RSTB	I	103	Reset: When RSTB is asserted low, the RTL8130 performs the internal system hardware reset. RSTB must be held for a minimum of 120ns periods.

4.3 Flash/EEPROM Interface(29 pins)

Symbol	Type	Pin No	Description
MA16-3, MA2/EESK, MA1/EEDI, MA0/EEDO	O O O O/I	47-46, 36-31, 29, 27, 25-24, 22, 20 18 17 16	Boot PROM address bus: used to access up to 128k byte flash memory or boot PROM. These three pins are switched to EESK, EEDI, EEDO in 9346 programming or auto-load mode.
EECS	O	19	9346 chip select
MD7-0	I/O	11, 10, 8-3	Boot PROM data bus
ROMCSB	O	15	ROM Chip Select: This is the chip select signal of the Boot PROM.
OEB	O	14	Output Enable: This enables the output buffer of the boot PROM during a read operation.
WEB	O	13	Write Enable: This signal strobes data into the flash memory during a write cycle.

4.4 Power Pin(38 pins)

Symbol	Type	Pin No	Description
VDD	P	2, 12, 23, 26, 37, 43, 49, 50, 53, 66, 72, 82, 94, 97, 107, 117, 128, 141, 151	+5V
GND	P	9, 21, 28, 30, 42, 48, 51, 56, 60, 69, 84, 99, 100, 101, 112, 122, 134, 146, 156	Ground

4.5 LED Interface(3 pins)

Symbol	Type	Pin No	Description
LED0, 1, 2	O	75, 74, 73	LED pins

LEDS1-0	00	01	10	11
LED0	TX/RX	TX/RX	TX	TX
LED1	LINK100	LINK10/100	LINK10/100	LINK100
LED2	LINK10	FULL	RX	LINK10

During power down mode, the LED's are OFF.

4.6 100/10 Mbps MII Interface(MII mode, 18 pins)

Symbol	Type	Pin No	Description
TXC	I	86	Transmit Clock: TXC is a continuous clock that provides a timing reference for the transfer of TXD[3:0], TEN. In MII mode, it uses the 25 MHz or 2.5 MHz supplied by the external PMD device.
TXEN	O	85	Transmit Enable: Indicates the presence of valid nibble data on TXD[3:0].
TXD3 TXD2 TXD1 TXD0(BNC)	O	79 80 81 83	MII mode: (bit1=0, Config3) Transmit Data(MII mode, Config3 bit1=1): Four parallel transmit data lines which are driven synchronous to the TXC for transmission by the external physical layer chip. AUI mode: (bit1=1, Config3) TXD0=BNC
RXC	I	88	Receive Clock: This is a continuous clock that is recovered from the incoming data. RXC is 25MHz in 100Mbps and 2.5Mhz in 10Mbs.
COL	I	78	Collision Detected: This signal is asserted high synchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
RXDV	I	89	Receive Data Valid: Data valid is asserted by an external PHY when receive data is present on the RXD[3:0] lines, and it is deasserted at the end of the packet. This signal is valid on the rising of the RXC.
RXD3 RXD2 RXD1 RXD0(AUI)	I	93 92 91 90	MII mode: (bit1=1, Config3) Receive Data: This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RXC by the external physical unit. AUI mode: (bit1=0, Config3) RXD0= AUI.
RXER	I	87	Receive Error: This pin is asserted to indicate that invalid symbol has been detected in 100Mbps MII mode. This signal is synchronized to RXC and can be asserted for a minimum of one receive clock. When asserted during a packet reception, it sets the ISE bit of the RSR register in the header of the Rx packet.
MDC	O	96	Management Data Clock: Synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks.
MDIO	I/O	95	Management Data: Bi-directional signal used to transfer management information.
MLink	I	77	MII link status notification
MFDup	I	76	MII full-duplex status notification

4.7 10 Mbps AUI Interface(AUI mode, 8 pins)

Symbol	Type	Pin No	Description
CD+, CD-	I	40, 41	This AUI collision input pair carries the differential collision input signal from the MAU.
RX+, RX-	I	38, 39	This AUI receive input pair carries the differential receive input signal from the MAU.
TX+, TX-	O	44, 45	This AUI transmit output pair contains differential line drivers which send Manchester encoded data to the MAU. These outputs are source followers and require 270Ω pull-down resistors to GND.
AUI(RXD0)	I	90	AUI mode: This input is used to detect the usage of an external MAU on the AUI interface. The input should be driven low for embedded BNC and high for external MAU. This pin is pulled low internally.
BNC(TXD0)	O	83	AUI mode: This pin is used to control the power of the embedded coaxial transceiver. When low, it will disable the power of the transceiver. This pin goes high only when: 1. The medium type is forced to BNC mode, and the AUI pin is low. 2. Both UTP and MII link fail in auto-detect medium mode, and the AUI pin is low.

4.8 100/10BASE-T UTP Interface(7 pins)

Symbol	Type	Pin No	Description
TXD+ TXD-	O O	68 67	100/10BASE-T transmit(Tx) data.
RXIN+ RXIN-	I I	63 62	100/10BASE-T receive(Rx) data.
X1(XTAL50)	I	55	X1 is internal clock input from 50 MHz OSC.
X2	O	54	X2 is crystal feedback output and is left open when 50MHz OSC is applied.
XTALSELB	I	70	The XTALSELB must be left open to use 50MHz OSC as the clock source.

4.9 TEST AND THE OTHER PINS(6 pins)

Symbol	Type	Pin No	Description
RTT2-3	TEST	58, 57	Chip test pins.
RTSET	I/O	61	This pin must pull low by 1.8KΩ resistor.
NC		52, 64, 65	

* All pins are relatively assigned and are subject to change when needed.

5. Register Descriptions

The RTL8130 provides the following set of operational registers mapped into PCI memory space or I/O space.

Offset	R/W	Tag	Description
0000h	R/W	IDR0	ID Register 0, The ID register0-5 are only permitted to read/write by 4-bye access.
0001h	R/W	IDR1	ID Register 1
0002h	R/W	IDR2	ID Register 2
0003h	R/W	IDR3	ID Register 3
0004h	R/W	IDR4	ID Register 4
0005h	R/W	IDR5	ID Register 5
0006h-0007h	-	-	Reserved
0008h	R/W	MAR0	Multicast Register 0, The MAR register0-7 are only permitted to read/write by 4-bye access.
0009h	R/W	MAR1	Multicast Register 1
000Ah	R/W	MAR2	Multicast Register 2
000Bh	R/W	MAR3	Multicast Register 3
000Ch	R/W	MAR4	Multicast Register 4
000Dh	R/W	MAR5	Multicast Register 5
000Eh	R/W	MAR6	Multicast Register 6
000Fh	R/W	MAR7	Multicast Register 7
0010h-0013h	R/W	TSD0	Transmit Status of Descriptor 0
0014h-0017h	R/W	TSD1	Transmit Status of Descriptor 1
0018h-001Bh	R/W	TSD2	Transmit Status of Descriptor 2
001Ch-001Fh	R/W	TSD3	Transmit Status of Descriptor 3
0020h-0023h	R/W	TSAD0	Transmit Start Address of Descriptor0
0024h-0027h	R/W	TSAD1	Transmit Start Address of Descriptor1
0028h-002Bh	R/W	TSAD2	Transmit Start Address of Descriptor2
002Ch-002Fh	R/W	TSAD3	Transmit Start Address of Descriptor3
0030h-0033h	R/W	RBSTART	Receive (Rx) Buffer Start Address
0034h-0035h	R	ERBCR	Early Receive (Rx) Byte Count Register
0036h	R	ERSR	Early Rx Status Register
0037h	R/W	CR	Command Register
0038h-0039h	R/W	CAPR	Current Address of Packet Read
003Ah-003Bh	R	CBR	Current Buffer Address: The initial value is 0000h. It reflects total received byte-count in the rx buffer.
003Ch-003Dh	R/W	IMR	Interrupt Mask Register
003Eh-003Fh	R/W	ISR	Interrupt Status Register
0040h-0043h	R/W	TCR	Transmit (Tx) Configuration Register
0044h-0047h	R/W	RCR	Receive (Rx) Configuration Register
0048h-004Bh	R/W	TCTR	Timer CounT Register: This register contains a 32-bit general-purpose timer. Writing any value to this 32-bit register will reset the original timer and begin to count from zero.
004Ch-004Fh	R/W	MPC	Missed Packet Counter: Indicates the number of packets discarded due to rx FIFO overflow. It is a 24-bit counter. After s/w reset, MPC is cleared. Only the lower 3 bytes are valid. When written any value, MPC will be reset also.
0050h	R/W	9346CR	93C46 Command Register
0051h	R/W	CONFIG0	Configuration Register 0
0052h	R/W	CONFIG1	Configuration Register 1

0053H	-	-	Reserved
0054h-0057h	R /W	TimerInt	Timer Interrupt Register. Once having written a nonzero value to this register, the Timeout bit of ISR register will be set whenever the TCTR reaches to this value. The Timeout bit will never be set as long as TimerInt register is zero.
0058h	R/W	MSR	Media Status Register
0059h	R/W	CONFIG3	Configuration register 3
005Ah	R/W	CONFIG4	Configuration register 4
005Bh	-	-	Reserved
005Ch-005Dh	R/W	MULINT	Multiple Interrupt Select
005Eh	R	RERID	PCI Revision ID = 10h.
005Fh	-	-	Reserved
0060h-0061h	R	TSAD	Transmit Status of All Descriptors
0062h-0063h	R/W	BMCR	Basic Mode Control Register
0064h-0065h	R	BMSR	Basic Mode Status Register
0066h-0067h	R/W	ANAR	Auto-Negotiation Advertisement Register
0068h-0069h	R	ANLPAR	Auto-Negotiation Link Partner Register
006Ah-006Bh	R	ANER	Auto-Negotiation Expansion Register
006Ch-006Dh	R	DIS	Disconnect Counter
006Eh-006Fh	R	FCSC	False Carrier Sense Counter
0070h-0071h	R/W	NWAYTR	N-way Test Register
0072h-0073h	R	REC	RX_ER Counter
0074h-0075h	R/W	CSCR	CS Configuration Register
0076-0077h	-	-	Reserved
0078h-007Bh	R/W	PHY1_PARM	PHY parameter 1
007Ch-007Fh	R/W	TW_PARM	Twister parameter
0080h	R/W	PHY2_PARM	PHY parameter 2
0081h	-	-	Reserved
0082h	R/W	MIIR	MII Register
0083h	-	-	Reserved
0084h	R/W	CRC0	Power Management CRC register0 for wakeup frame0
0085h	R/W	CRC1	Power Management CRC register1 for wakeup frame1
0086h	R/W	CRC2	Power Management CRC register2 for wakeup frame2
0087h	R/W	CRC3	Power Management CRC register3 for wakeup frame3
0088h	R/W	CRC4	Power Management CRC register4 for wakeup frame4
0089h	R/W	CRC5	Power Management CRC register5 for wakeup frame5
008Ah	R/W	CRC6	Power Management CRC register6 for wakeup frame6
008Bh	R/W	CRC7	Power Management CRC register7 for wakeup frame7
008Ch–0093h	R/W	Wakeup0	Power Management wakeup frame0 (64bit)
0094h–009Bh	R/W	Wakeup1	Power Management wakeup frame1 (64bit)
009Ch–00A3h	R/W	Wakeup2	Power Management wakeup frame2 (64bit)
00A4h–00ABh	R/W	Wakeup3	Power Management wakeup frame3 (64bit)
00ACh–00B3h	R/W	Wakeup4	Power Management wakeup frame4 (64bit)
00B4h–00BBh	R/W	Wakeup5	Power Management wakeup frame5 (64bit)
00BCh–00C3h	R/W	Wakeup6	Power Management wakeup frame6 (64bit)
00C4h–00CBh	R/W	Wakeup7	Power Management wakeup frame7 (64bit)
00CCh	R/W	LSBCRC0	LSB of the mask byte of wakeup frame0 within offset 12 to 75
00CDh	R/W	LSBCRC1	LSB of the mask byte of wakeup frame1 within offset 12 to 75
00CEh	R/W	LSBCRC2	LSB of the mask byte of wakeup frame2 within offset 12 to 75
00CFh	R/W	LSBCRC3	LSB of the mask byte of wakeup frame3 within offset 12 to 75
00D0h	R/W	LSBCRC4	LSB of the mask byte of wakeup frame4 within offset 12 to 75

00D1h	R/W	LSBCRC5	LSB of the mask byte of wakeup frame5 within offset 12 to 75
00D2h	R/W	LSBCRC6	LSB of the mask byte of wakeup frame6 within offset 12 to 75
00D3h	R/W	LSBCRC7	LSB of the mask byte of wakeup frame7 within offset 12 to 75
00D4h-00D7h	R/W	FLASH	Flash memory read/write register

5.1 Receive Status Register in Rx packet header

Bit	R/W	Symbol	Description
15	R	MAR	Multicast Address Received: Set to 1 indicates that a multicast packet is received.
14	R	PAM	Physical Address Matched: Set to 1 indicates that the destination address of this packet matches the value written in ID registers.
13	R	BAR	Broadcast Address Received: Set to 1 indicates that a broadcast packet is received. BAR, MAR bit will not be set simultaneously.
12-6	-	-	Reserved
5	R	ISE	Invalid Symbol Error: (100BASE-TX only) An invalid symbol was encountered during the reception of this packet if this bit set to 1.
4	R	RUNT	Runt Packet Received: Set to 1 indicates that the received packet length is smaller than 64 bytes (i.e. media header + data + CRC < 64 bytes)
3	R	LONG	Long Packet: Set to 1 indicates that the size of the received packet exceeds 4k bytes.
2	R	CRC	CRC Error: When set, indicates that a CRC error occurred on the received packet.
1	R	FAE	Frame Alignment Error: When set, indicates that a frame alignment error occurred on this received packet.
0	R	ROK	Receive OK: When set, indicates that a good packet is received.

5.2 Transmit Status Register (TSD0-3)(Offset 0010h-001Fh, R/W)

The read-only bits (CRS, TABT, OWC, CDH, NCC3-0, TOK, TUN) will be cleared by RTL8130 when the Transmit Byte Count (bit12-0) in the corresponding Tx descriptor is written. It is not affected when software writes to these bits. These registers are only permitted to write by double-word access. After software reset, all bits except OWN bit are reset to “0”.

Bit	R/W	Symbol	Description
31	R	CRS	Carrier Sense Lost: Set to 1 when the carrier is lost during transmitting a packet.
30	R	TABT	Transmit Abort: Set to 1 if the transmission of a packet was aborted. This bit is read only, writing to this bit is not affected.
29	R	OWC	Out of Window Collision: Set to 1 if the RTL8130 encountered an "out of window" collision during the transmission of a packet.
28	R	CDH	CD Heart Beat: The same as RTL8029(AS). This bit is cleared in the 100 Mbps mode.
27-24	R	NCC3-0	Number of Collision Count: Indicates that the number of collisions encountered during the transmission of a packet.
23-22	-	-	Reserved
21-16	R/W	ERTXTH5-0	Early Tx Threshold: Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the Tx FIFO reaches this level, (or the FIFO contains at least one complete

			packet) the RTL8130 will transmit this packet. 000000 = 8 bytes These fields count from 000001 to 111111 in unit of 32 bytes. This threshold must be avoided from exceeding 2K byte.
15	R	TOK	Transmit OK: Set to 1 indicates that the transmission of a packet was completed successfully and no transmit underrun occurs.
14	R	TUN	Transmit FIFO Underrun: Set to 1 if the Tx FIFO was exhausted during the transmission of a packet. The RTL8130 can re-transfer data if the Tx FIFO underruns and can also transmit the packet to the wire successfully even though the Tx FIFO underruns. That is, when TSD<TUN>=1, TSD<TOK>=0 and ISR<TOK>=1 (or ISR<TER>=1).
13	R/W	OWN	OWN: The RTL8130 sets this bit to 1 when the Tx DMA operation of this descriptor was completed. The driver must set this bit to 0 when the Transmit Byte Count (bit0-12) is written. The default value is 1.
12-0	R/W	SIZE	Descriptor Size: The total size in bytes of the data in this descriptor. If the packet length is more than 1792 byte (0700h), the Tx queue will be invalid, i.e. the next descriptor will be written only after the OWN bit of that long packet's descriptor has been set.

5.3 ERSR: Early Rx Status Register (Offset 0036h, R)

Bit	R/W	Symbol	Description
7-4	-	-	Reserved
3	R	ERGood	Early Rx Good packet: This bit is set whenever a packet is completely received and the packet is good. This bit is cleared when writing 1 to it,
2	R	ERBad	Early Rx Bad packet: This bit is set whenever a packet is completely received and the packet is bad. Writing 1 will clear this bit.
1	R	EROVW	Early Rx OverWrite: This bit is set when the RTL8130's local address pointer is equal to CAPR. In the early mode, this is different from buffer overflow. It happens that the RTL8130 detected an Rx error and wanted to fill another packet data from the beginning address of that error packet. Writing 1 will clear this bit.
0	R	EROK	Early Rx OK: The power-on value is 0. It is set when the Rx byte count of the arriving packet exceeds the Rx threshold. After the whole packet is received, the RTL8130 will set ROK or RER in ISR and clear this bit simultaneously. Setting this bit will invoke a ROK interrupt.

5.4 Command Register (Offset 0037h, R/W)

Bit	R/W	Symbol	Description
7-5	-	-	Reserved
4	R/W	RST	Reset: Setting to 1 forces the RTL8130 to a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, resets the system buffer pointer to the initial value (Tx buffer is at TSAD0, Rx buffer is empty). The values of IDR0-5 and MAR0-7 and PCI configuration space will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the RTL8130 when the reset

			operation is complete.
3	R/W	RE	Receiver Enable
2	R/W	TE	Transmitter Enable
1	-	-	Reserved
0	R	BUFE	Buffer Empty: Rx Buffer Empty. There is no packet stored in the Rx buffer ring.

5.5 Interrupt Mask Register (Offset 003Ch-003Dh, R/W)

Bit	R/W	Symbol	Description
15	R/W	SERR	System Error Interrupt: 1 => Enable, 0 => Disable.
14	R/W	TimeOut	Time Out Interrupt: 1 => Enable, 0 => Disable.
13	R/W	LenChg	Cable Length Change Interrupt: 1 => Enable, 0 => Disable.
12-7	-	-	Reserved
6	R/W	FOVW	Rx FIFO Overflow Interrupt: 1 => Enable, 0 => Disable.
5	R/W	PUN/LinkChg	Packet Underrun/Link Change Interrupt: 1 => Enable, 0 => Disable.
4	R/W	RXOVW	Rx Buffer Overflow Interrupt: 1 => Enable, 0 => Disable.
3	R/W	TER	Transmit Error Interrupt: 1 => Enable, 0 => Disable.
2	R/W	TOK	Transmit OK Interrupt: 1 => Enable, 0 => Disable.
1	R/W	RER	Receive Error Interrupt: 1 => Enable, 0 => Disable.
0	R/W	ROK	Receive OK Interrupt: 1 => Enable, 0 => Disable.

5.6 Interrupt Status Register (Offset 003Eh-003Fh, R/W)

Bit	R/W	Symbol	Description
15	R/W	SERR	System Error: Set to 1 when the RTL8130 signals a system error on the PCI bus.
14	R/W	TimeOut	Time Out: Set to 1 when the TCTR register reaches to the value of the TimerInt register.
13	R/W	LenChg	Cable Length Change: Cable length is changed after Receiver is enabled.
12 - 7	-	-	Reserved
6	R/W	FOVW	Rx FIFO Overflow
5	R/W	PUN/LinkChg	Packet Underrun/Link Change: Set to 1 when CAPR is written but Rx buffer is empty, or when link status is changed.
4	R/W	RXOVW	Rx Buffer Overflow: Set when receive (Rx) buffer ring storage resources have been exhausted.
3	R/W	TER	Transmit (Tx) Error: Indicates that a packet transmission was aborted, due to excessive collisions, according to the TXRR's setting
2	R/W	TOK	Transmit (Tx) OK: Indicates that a packet transmission is completed successfully.
1	R/W	RER	Receive (Rx) Error: Indicates that a packet has either CRC error or frame alignment error (FAE). The collided frame will not be recognized as CRC error if the length of this frame is shorter than 16 byte.
0	R/W	ROK	Receive (Rx) OK: In normal mode, indicates the successful completion of a packet reception. In early mode, indicates that the Rx byte count of the arriving packet exceeds the early Rx threshold.

5.7 Transmit Configuration Register (Offset 0040h-0043h, R/W)

Bit	R/W	Symbol	Description
31	-	-	Reserved
30-28	R	HWVER	Hardware Version number: 7 for RTL8139A and RTL8130 6 for RTL8139
27	R	OEMID	OEM ID = 1
26	R	8130ID	RTL8130ID = 1
25-24	R/W	IFG1, 0	Interframe Gap Time: This field allows the user to adjust the interframe gap time below the standard: 9.6 us for 10Mbps, 960 ns for 100Mbps. The time can be programmed from 9.6 us to 8.4 us (10Mbps) and 960ns to 840ns (100Mbps). Note that any value other than zero will violate the IEEE 802.3 standard. The formula for the inter frame gap is: 10Mbps 8.4us + 0.4(IFG(1:0)) us 100Mbps 840ns + 40(IFG(1:0)) ns
23-19	-	-	Reserved
18, 17	R/W	LBK1, LBK0	Loopback test. There will be no packet on the TX+/- lines under the Loopback test condition. The loopback function must be independent of the link state. 00 : normal operation 01 : MAC Loopback 10 : PHY Loopback 11 : Twister Loopback
16	R/W	CRC	Append CRC: Setting to 1 means that there's no CRC appended at the end of a packet. Setting to 0 means that there's CRC appended at the end of a packet.
15-11	-	-	Reserved
10-8	R/W	MXDMA2, 1, 0	Max DMA Burst Size per Tx DMA Burst: This field sets the maximum size of transmit DMA data bursts according to the following table: 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = 2048 bytes
7-4	R/W	TXRR	Tx Retry Count: These are used to specify additional transmission retries in multiple of 16(IEEE 802.3 CSMA/CD retry count). If the TXRR is set to 0, the transmitter will re-transmit 16 times before aborting due to excessive collisions. If the TXRR is set to a value greater than 0, the transmitter will re-transmit a number of times equals to the following formula before aborting: Total retries = 16 + (TXRR * 16) The TER bit in the ISR register or transmit descriptor will be set when the transmission fails and reaches to this specified retry count.
3-1	-	-	Reserved
0	W	CLRABT	Clear Abort: Setting this bit to 1 causes the RTL8130 to retransmit the packet at the last transmitted descriptor when this transmission was aborted, Setting this bit is only permitted in the transmit abort state.

5.8 Receive Configuration Register (Offset 0044h-0047h, R/W)

Bit	R/W	Symbol	Description
31-28	-	-	Reserved
27-24	R/W	ERTH3, 2, 1, 0	Early Rx threshold bits: These bits are used to select the Rx threshold multiplier of the whole packet that has been transferred to the system buffer in early mode when the frame protocol is under the RTL8130's definition. 0000 = no early rx threshold 0001 = 1/16 0010 = 2/16 0011 = 3/16 0100 = 4/16 0101 = 5/16 0110 = 6/16 0111 = 7/16 1000 = 8/16 1001 = 9/16 1010 = 10/16 1011 = 11/16 1100 = 12/16 1101 = 13/16 1110 = 14/16 1111 = 15/16
23-18	-	-	Reserved
17	R/W	MulERINT	Multiple early interrupt select: When this bit is set, any received packet invokes early interrupt according to MULINT<MISR[11:0]> setting in early mode. When this bit is reset, the packets of familiar protocol (IPX, IP, NDIS, etc) invoke early interrupt according to RCR<ERTH[3:0]> setting in early mode. The packets of unfamiliar protocol will invoke early interrupt according to the setting of MULINT<MISR[11:0]>.
16	R/W	RER8	The RTL8130 receives the error packet whose length is larger than 8 bytes after setting the RER8 bit to 1. The RTL8130 receives the error packet larger than 64-byte long when the RER8 bit is cleared. The power-on default is zero. If AER or AR is set, the RER will be set when the RTL8130 receives an error packet whose length is larger than 8 bytes. The RER8 is " Don't care " in this situation.
15-13	R/W	RXFTH2, 1, 0	Rx FIFO Threshold: Specifies Rx FIFO Threshold level. When the number of the received data bytes from a packet, which is being received into the RTL8130's Rx FIFO, has reached to this level (or the FIFO has contained a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following table: 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = no rx threshold. The RTL8130 begins the transfer of data after having received a whole packet in the FIFO.
12-11	R/W	RBLEN1, 0	Rx Buffer Length: This field indicates the size of the Rx ring buffer. 00 = 8k + 16 byte 01 = 16k + 16 byte 10 = 32K + 16 byte

			11 = 64K + 16 byte
10-8	R/W	MXDMA2, 1, 0	Max DMA Burst Size per Rx DMA Burst: This field sets the maximum size of the receive DMA data bursts according to the Following table: 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = unlimited
7	R/W	WRAP	When set to 0: The RTL8130 will transfer the rest of the packet data into the beginning of the Rx buffer if this packet has not been completely moved into the Rx buffer and the transfer has arrived at the end of the Rx buffer. When set to 1: The RTL8130 will keep moving the rest of the packet data into the memory immediately after the end of the Rx buffer, if this packet has not been completely moved into the Rx buffer and the transfer has arrived at the end of the Rx buffer. The software driver must reserve at least 1.5K bytes buffer to accept the remainder of the packet. We assume that the remainder of the packet is X bytes. The next packet will be moved into the memory from the X byte offset at the top of the Rx buffer. This bit is invalid when Rx buffer is selected to 64K bytes.
6	-	-	Reserved
5	R/W	AER	Accept Error Packet: When set to 1, all packets with CRC error, alignment error, and/or collided fragments will be accepted. When set to 0, all packets with CRC error, alignment error, and/or collided fragments will be rejected.
4	R/W	AR	Accept Runt: This bit allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt. Set to 1 to accept runt packets.
3	R/W	AB	Set to 1 to accept broadcast packets, 0 to reject.
2	R/W	AM	Set to 1 to accept multicast packets, 0 to reject.
1	R/W	APM	Set to 1 to accept physical match packets, 0 to reject.
0	R/W	AAP	Set to 1 to accept all packets with physical destination address, 0 to reject.

5.9 9346CR: 93C46 Command Register (Offset 0050h, R/W)

Bit	R/W	Symbol	Description
7-6	R/W	EEM1-0	These 2 bits select the RTL8130 operating mode.

EEM1	EEM0	Operating Mode
0	0	Normal (RTL8130 network/host communication mode)
0	1	Auto-load: Entering this mode will make the RTL8130 load the contents of 93C46 like when the RSTB signal is asserted. This auto-load operation will take about 2 ms. After it is completed, the RTL8130 goes back to the normal mode automatically (EEM1 = EEM0 = 0) and all the other registers are reset to default values.
1	0	93C46 programming: In this mode, both network and host

			<table><tr><td></td><td></td><td>bus master operations are disabled. The 93C46 can be directly accessed via bit3-0 which now reflect the states of EECS, EESK, EEDI, & EEDO pins respectively.</td></tr><tr><td>1</td><td>1</td><td>Config register write enable: Before writing to CONFIG0, 1 registers, the RTL8130 must be placed in this mode. This will prevent RTL8130's configurations from accidental change.</td></tr></table>
4-5	-	-	Reserved
3	R/W	EECS	These bits reflect the state of EECS, EESK, EEDI & EEDO pins in auto-load or 93C46 programming mode and are valid only when Flash bit is cleared. Note: EESK, EEDI and EEDO is valid after boot ROM complete.
2	R/W	EESK	
1	R/W	EEDI	
0	R	EEDO	

5.10 CONFIG 0: Configuration Register 0 (Offset 0051h, R/W)

Bit	R/W	Symbol	Description
7	R	SCR	Scrambler Mode: Always 0.
6	R	PCS	PCS Mode: Always 0.
5	R	T10	10 Mbps Mode: Always 0.
4-3	R	PL1, PL0	Select 10 Mbps medium type: Always (PL1, PL0) = (1, 0)
2-0	R	BS2, BS1, BS0	Select Boot ROM size <table><tr><th>BS2</th><th>BS1</th><th>BS0</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>0</td><td>No Boot ROM</td></tr><tr><td>0</td><td>0</td><td>1</td><td>8K Boot ROM</td></tr><tr><td>0</td><td>1</td><td>0</td><td>16K Boot ROM</td></tr><tr><td>0</td><td>1</td><td>1</td><td>32K Boot ROM</td></tr><tr><td>1</td><td>0</td><td>0</td><td>64K Boot ROM</td></tr><tr><td>1</td><td>0</td><td>1</td><td>128K Boot ROM</td></tr><tr><td>1</td><td>1</td><td>0</td><td>unused</td></tr><tr><td>1</td><td>1</td><td>1</td><td>unused</td></tr></table>

5.11 CONFIG 1: Configuration Register 1 (Offset 0052h, R/W)

Bit	R/W	Symbol	Description
7-6	R/W	LEDS1-0	Refer to LED PIN definition. These bits initial value com from 93C46.
5	R/W	DVRLOAD	Driver Load: Software maybe use this bit to make sure that the driver has been loaded. Writing 1 is 1. Writing 0 is 0. When the command register bits IOEN, MEMEN, BMEN of PCI configuration space are written, the RTL8130 will clear this bit automatically.

<table>
<tr><td>4</td><td>R/W</td><td>LWACT</td><td>LWAKE active mode: The LWACT bit and LWPTN bit in CONFIG4 register are used to program the LWAKE pin’s output signal. According to the combination of these two bits, there may be 4 choices of LWAKE signal, i.e., active high, active low, positive (high) pulse, and negative (low) pulse. The output pulse width is about 150 ms.
The default value of each of these two bits is 0, i.e., the default output signal of LWAKE pin is an active high signal.
<table>
<tr><th colspan="2" rowspan="2">LWAKE output</th><th colspan="2">LWACT</th></tr>
<tr><th>0</th><th>1</th></tr>
<tr><td rowspan="2">LWPTN</td><td>0</td><td>Active high*</td><td>Active low</td></tr>
<tr><td>1</td><td>Positive pulse</td><td>Negative pulse</td></tr>
</table>
* Default value.</td></tr>
<tr><td>3</td><td>R</td><td>MEMMAP</td><td>Memory Mapping: The operational registers are mapped into PCI memory space.</td></tr>
<tr><td>2</td><td>R</td><td>IOMAP</td><td>I/O Mapping: The operational registers are mapped into PCI I/O space.</td></tr>
<tr><td>1</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>0</td><td>R/W</td><td>PMEn</td><td>Power Management Enable
Writable only when 93C46CR register EEM1=EEM0=1
Let A denote the New_Cap bit (bit 4 of the Status Register) in the PCI Configuration space offset 06H.
Let B denote the Cap_Ptr register in the PCI Configuration space offset 34H.
Let C denote the Cap_ID (power management) register in the PCI Configuration space offset 50H.
Let D denote the power management registers in the PCI Configuration space offset from 52H to 57H.
Let E denote the Next_Ptr (power management) register in the PCI Configuration space offset 51H.
<table>
<tr><th>PMEn</th><th>Description</th></tr>
<tr><td>0</td><td>A=B=C=E=0, D not valid</td></tr>
<tr><td>1</td><td>A=1, B=50h, C=01h, D valid, E=0</td></tr>
</table></td></tr>
</table>

5.12 Media Status Register (Offset 0058h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>R/W</td><td>TXFCE/
LdTXFCE</td><td>Tx Flow Control Enable: The flow control is valid in full-duplex mode only. This register’s default value comes from 93C46.
<table>
<tr><th>RTL8130</th><th>Remote</th><th>TXFCE/LdTXFCE</th></tr>
<tr><td>ANE = 1</td><td>NWAY FLY mode</td><td>R/O</td></tr>
<tr><td>ANE = 1</td><td>NWAY mode only</td><td>R/W</td></tr>
<tr><td>ANE = 1</td><td>No NWAY</td><td>R/W</td></tr>
<tr><td>ANE = 0 & full-duplex mode</td><td>-</td><td>R/W</td></tr>
<tr><td>ANE = 0 & half-duplex mode</td><td>-</td><td>invalid</td></tr>
</table>
NWAY FLY mode : NWAY with flow controo capability
NWAY mode only : NWAY without flow control capability</td></tr>
</table>

6	R/W	RXFCE	RX Flow control Enable: The flow control is enabled in full-duplex mode only. The default value comes from 93C46.
5-4	R	Medium	Current medium status: Medium / Bit4: 0 = NoLink, 1 = UTP; Bit5 = 1: MII, AUI
3	R	SPEED_10	Set, when current media is 10Mbps mode. Reset, when current media is 100Mbps mode.
2	R	LINKB	Inverse of Link status. 0 = Link OK. 1 = Link Fail.
1	R	TXPF	Set, when RTL8130 sends pause packet. Reset, when RTL8130 sends timer done packet.
0	R	RXPF	Pause Flag: Set, when RTL8130 is in backoff state because a pause packet received. Reset, when pause state is clear.

5.13 CONFIG 3: Configuration Register3 (Offset 0059h, R/W)

Bit	R/W	Symbol	Description
7	R	GNTSel	Gnt Select: Select the Frame's asserted time after the Grant signal has been asserted. The Frame and Grant are the PCI signals. 0: No delay 1: delay one clock from GNT assertion.
6	R/W	PARM_En	Parameter Enable: Setting to 0 and 9346CR register EEM1=EEM0=1 enable the PHY1_PARM, PHY2_PARM, TW_PARM be written via software. Setting to 1 will allow parameter auto-load from 9346 and disable writing to PHY1_PARM, PHY2_PARM and TW_PARM registers via software. The parameter auto-loaded form 9346 is TW_PARM only. The PHY parameters can not be auto-loaded from 9346.
5	R/W	Magic	Magic Packet: This bit is valid when the PWEn bit of CONFIG1 register is set. The RTL8130 will assert the PMEB signal to wakeup the operating system when the magic packet is received. Once the RTL8130 has been put into the magic packet mode, it scans all incoming packets addressed to the node for a specific data sequence, which indicates to the controller that this is a Magic packet frame. A Magic packet frame must also meet the basic requirements: Destination address + Source address + data + CRC The destination address may be the node ID of the receiving station or a multicast address which includes the broadcast address. The specific sequence consists of 16 duplications of 6 byte ID registers, with no breaks or interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE address match the address of the ID registers. If the Node ID is 11h 22h 33h 44h 55h 66h, then the magic frame's format is like the following: Destination address + source address + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 +

			11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC
4	R/W	LinkUp	Link Up: This bit is valid when the PWEn bit of CONFIG1 register is set. The RTL8130, in adequate power state, will assert the PMEB signal to wakeup the operating system when the cable connection is re-established.
3-2	R/W	Medium1, Medium0	These two bits are used to select medium mode. Medium mode / Medium0: 0 = AutoDetect, 1 = UTP; Medium1 0 = MII, 1 = AUI In AutoDetect mode, the priority is UTP > MII or UTP > AUI. The MEDIUMWE (bit21, FLASH) should be set to 1 before performing a config register write to these 2 bits.
1	R	MIIorAUI	1: AUI mode. The RTL8130 is configured to support UTP, AUI, and flash. 0: MII mode. The RTL8130 is configured to support UTP and MII.
0	R	FBtBEn	Fast Back to Back Enable; Set to 1 to enable Fast Back to Back.

5.14 CONFIG 4: Configuration Register4 (Offset 005Ah, R/W)

Bit	R/W	Symbol	Description
7	-	-	Reserved.
6	-	-	Reserved.
5	R/W	LongWF	Long Wake-up Frame: Set to 0: The RTL8139A OEM supports up to 8 wake-up frames, each with masked bytes selected from offset 12 to 75. Set to 1: The RTL8139A OEM supports up to 5 wake-up frames. The wake-up frame 0 to 1 are the same as above, the wake-up frame 2 and 3 are merged into one long wake-up frame with masked bytes selected from offset 12 to 139. So as to wakeup frame 4 and 5, 6 and 7.
4	R/W	LWPME	LANWAKE vs PMEB: Set to 0: The LWAKE and PMEB are asserted at the same time. Set to 1: The LWAKE can only be asserted when the PMEB is asserted and the ISOLATEB is low.
3	R/W	MSWFB	Microsoft® Wake-up Frame: This bit is valid when the PWEn bit of CONFIG1 register is set. Set to 0: The RTL8130 supports Microsoft® Wake-up Frame. Set to 1: Disable Wake-up Frame support.
2	R/W	LWPTN	LWAKE pattern: Please refer to LWACT bit in CONFIG1 register.
1	R/W	PARM_En2	Parameter Enable2: This bit is valid only when the PARM_En(bit6, Config1) is set to 1. Set to 0: The value of TW_PARM is auto-loaded from EEPROM directly. Set to 1: The value of TW_PARM is determined by twister parameter auto-scan mechanism of the RTL8130, each time when Link is ok in 100Mbps mode. The twister parameters used by auto-scan mechanism are built-in in the RTL8130.

0	-	-	Reserved.

5.15 Multiple Interrupt Select Register (Offset 005Ch-005Dh, R/W)

If the received packet data is not the familiar protocol (IPX, IP, NDIS, etc.) to RTL8130, RCR<ERTH[3:0]> won't be used to transfer data in early mode. This register will be written to the received data length in order to make early rx interrupt for the unfamiliar protocol.

Bit	R/W	Symbol	Description
15-12	-	-	Reserved
11-0	R/W	MISR11-0	Multiple Interrupt Select: Indicates that the RTL8130 makes an rx interrupt after RTL8130 has transferred the byte data into the system memory. If the value of these bits is zero, there will be no early interrupt as soon as the RTL8130 prepares to execute the first PCI transaction of the received data. Bit1, 0 must be zero. The ERTH3-0 bits should not be set to 0 when the multiple interrupt select register is used.

- The above is true when MulERINT=0 (bit17, RCR). When MulERINT=1, any received packet invokes early interrupt according to MISR[11:0] setting in early mode.

5.16 PCI Revision ID (Offset 005Eh, R)

Bit	R/W	Symbol	Description
7-0	R	Revision ID	The value in PCI Configuration Space offset 08h is 10h.

5.17 Transmit Status of All Descriptors (TSAD) Register (Offset 0060h-0061h, R/W)

Bit	R/W	Symbol	Description
15	R	TOK3	TOK bit of Descriptor 3
14	R	TOK2	TOK bit of Descriptor 2
13	R	TOK1	TOK bit of Descriptor 1
12	R	TOK0	TOK bit of Descriptor 0
11	R	TUN3	TUN bit of Descriptor 3
10	R	TUN2	TUN bit of Descriptor 2
9	R	TUN1	TUN bit of Descriptor 1
8	R	TUN0	TUN bit of Descriptor 0
7	R	TABT3	TABT bit of Descriptor 3
6	R	TABT2	TABT bit of Descriptor 2
5	R	TABT1	TABT bit of Descriptor 1
4	R	TABT0	TABT bit of Descriptor 0
3	R	OWN3	OWN bit of Descriptor 3
2	R	OWN2	OWN bit of Descriptor 2
1	R	OWN1	OWN bit of Descriptor 1
0	R	OWN0	OWN bit of Descriptor 0

5.18 Basic Mode Control Register (Offset 0062h-0063h, R/W)

Bit	Name	Description/Usage	Default/ Attribute
15	Reset	This bit sets the status and control registers of the PHY(register 0062-0074H) in a default state. This bit is self-clearing. 1 = software reset; 0 = normal operation.	0, RW
14	-	Reserved	-
13	Spd_Set	This bit sets the network speed. 1 = 100Mbps; 0 = 10Mbps. This bit‘s initial value comes from 93C46.	0, RW
12	Auto Negotiation Enable (ANE)	This bit enables/disables the NWay auto-negotiation function. Set to 1 to enable auto-negotiation, bit13 will be ignored. Set to 0 disables auto-negotiation, bit13 and bit8 will determine the link speed and the data transfer mode, respectively. This bit‘s initial value comes from 93C46.	0, RW
11	MLinkActiveState	The initial value comes from 9346. Set to 1: Mlink = high ⇔ MII link OK Set to 0: Mlink = low ⇔ MII link OK	0, R
10	MDupActiveState	The initial value comes from 9346 Set to 1: MFDup = high ⇔ MII interface is in full duplex mode Set to 0: MFDup = low ⇔ MII interface is in full duplex mode	0, R
9	Restart Auto Negotiation	This bit allows the NWay auto-negotiation function to be reset. 1 = re-start auto-negotiation; 0 = normal operation.	0, RW
8	Duplex Mode	This bit sets the duplex mode. 1 = full-duplex; 0 = normal operation. This bit‘s initial value comes from 93C46. If bit12 = 1, read = status write = register value. If bit12 = 0, read = write = register value.	0, RW
7-0	-	Reserved	-

5.19 Basic Mode Status Register (Offset 0064h-0065h, R)

Bit	Name	Description/Usage	Default/ Attribute
15	100Base-T4	1 = enable 100Base-T4 support; 0 = suppress 100Base-T4 support.	0, RO
14	100Base_TX_ FD	1 = enable 100Base-TX full duplex support; 0 = suppress 100Base-TX full duplex support.	1, RO
13	100BASE_TX_HD	1 = enable 100Base-TX half-duplex support; 0 = suppress 100Base-TX half-duplex support.	1, RO
12	10Base_T_FD	1 = enable 10Base-T full duplex support; 0 = suppress 10Base-T full duplex support.	1, RO
11	10_Base_T_HD	1 = enable 10Base-T half-duplex support; 0 = suppress 10Base-T half-duplex support.	1, RO
10-6	-	Reserved	-
5	Auto Negotiation Complete	1 = auto-negotiation process completed; 0 = auto-negotiation process not completed.	0, RO
4	Remote Fault	1 = remote fault condition detected (cleared on read); 0 = no remote fault condition detected.	0, RO
3	Auto Negotiation	1 = Link had not been experienced fail state.	1, RD

		0 = Link had been experienced fail state	
2	Link Status	1 = valid link established; 0 = no valid link established.	0, RO
1	Jabber Detect	1 = jabber condition detected; 0 = no jabber condition detected.	0, RO
0	Extended Capability	1 = extended register capability; 0 = basic register capability only.	1, RO

5.20 Auto-negotiation Advertisement Register (Offset 0066h-0067h, R/W)

Bit	Name	Description/Usage	Default/ Attribute
15	NP	Next Page bit. 0 = transmitting the primary capability data page; 1 = transmitting the protocol specific data page.	0, RO
14	ACK	1 = acknowledge reception of link partner capability data word.	0, RO
13	RF	1 = advertise remote fault detection capability; 0 = do not advertise remote fault detection capability.	0, RW
12-11	-	Reserved	-
10	Pause	1 = flow control is supported by local node. 0 = flow control is not supported by local mode.	1, RO
9	-	Reserved	-
8	TXFD	1 = 100Base-TX full duplex is supported by local node; 0 = 100Base-TX full duplex not supported by local node.	1, RW
7	TX	1 = 100Base-TX is supported by local node; 0 = 100Base-TX not supported by local node.	1, RW
6	10FD	1 = 10Base-T full duplex supported by local node; 0 = 10Base-T full duplex not supported by local node.	1, RW
5	10	1 = 10Base-T is supported by local node; 0 = 10Base-T not supported by local node.	1, RW
4-0	Selector	Binary encoded selector supported by this node. Currently only CSMA/ CD <00001> is specified. No other protocols are supported.	<00001>, RW

5.21 Auto-Negotiation Link Partner Ability Register (Offset 0068h-0069h, R)

Bit	Name	Description/Usage	Default/ Attribute
15	NP	Next Page bit. 0 = transmitting the primary capability data page; 1 = transmitting the protocol specific data page.	0, RO
14	ACK	1 = link partner acknowledges reception of local node's capability data word.	0, RO
13	RF	1 = link partner is indicating a remote fault.	0, RO
12-11	-	Reserved	-
10	Pause	1 = Flow control is supported by link partner , 0 = Flow control is not supported by link partner.	0, RO

9	-	Reserved	-
8	TXFD	1 = 100Base-TX full duplex is supported by link partner; 0 = 100Base-TX full duplex not supported by link partner.	0, RO
7	TX	1 = 100Base-TX is supported by link partner; 0 = 100Base-TX not supported by link partner.	0, RO
6	10FD	1 = 10Base-T full duplex is supported by link partner; 0 = 10Base-T full duplex not supported by link partner.	0, RO
5	10	1 = 10Base-T is supported by link partner; 0 = 10Base-T not supported by link partner.	0, RO
4-0	Selector	Link Partner's binary encoded node selector. Currently only CSMA/ CD <00001> is specified.	<00000>, RO

5.22 Auto-negotiation Expansion Register (Offset 006Ah-006Bh, R)

This register contains additional status for NWay auto-negotiation.

Bit	Name	Description/Usage	Default/ Attribute
15-5	-	Reserved, This bit is always set to 0.	-
4	MLF	Status indicating if a multiple link fault has occurred. 1 = fault occurred; 0 = no fault occurred.	0, RO
3	LP_NP_ABLE	Status indicating if the link partner supports Next Page negotiation. 1 = supported; 0 = not supported.	0, RO
2	NP_ABLE	This bit indicates if the local node is able to send additional Next Pages.	0, RO
1	PAGE_RX	This bit is set when a new Link Code Word Page has been received. The bit is automatically cleared when the auto-negotiation link partner's ability register (register 5) is read by management.	0, RO
0	LP_NW_ABLE	1 = link partner supports NWay auto-negotiation.	0, RO

5.23 Disconnect Counter (Offset 006Ch-006Dh, R)

Bit	Name	Description/Usage	Default/ Attribute
15-0	DCNT	This 16-bit counter increments by 1 for every disconnect event. It rolls over when becomes full. It is cleared to zero by read command.	h'[0000], R

5.24 False Carrier Sense Counter (Offset 006Eh-006Fh, R)

Bit	Name	Description/Usage	Default/ Attribute
15-0	FCSCNT	This 16-bit counter increments by 1 for each false carrier event. It is cleared to zero by read command.	h'[0000], R

5.25 NWay Test Register (Offset 0070h-0071h, R/W)

Bit	Name	Description/Usage	Default/ Attribute
15-8	-	Reserved	-
7	NWLPBK	1 = set NWay to loopback mode.	0, RW
6-4	-	Reserved	-
3	ENNWLE	1 = LED0 Pin indicates linkpulse	0, RW
2	FLAGABD	1 = Auto-neg experienced ability detect state	0, RO
1	FLAGPDF	1 = Auto-neg experienced parallel detection fault state	0, RO
0	FLAGLSC	1 = Auto-neg experienced link status check state	0, RO

5.26 RX_ER Counter (Offset 0072h-0073h, R)

Bit	Name	Description/Usage	Default/ Attribute
15-0	RXERCNT	This 16-bit counter increments by 1 for each valid packet received . It is cleared to zero by read command.	h'[0000], R

5.27 CS Configuration Register (Offset 0074h-0075h, R/W)

Bit	Name	Description/Usage	Default/ Attribute
15	Testfun	1 = Auto-neg speeds up internal timer	0,WO
14-10	-	Reserved	-
9	LD	Active low TPI link disable signal. When low, TPI still transmits link pulses and TPI stays in good link state.	1, RW
8	HEART BEAT	1 = HEART BEAT enable, 0 = HEART BEAT disable. HEART BEAT function is only valid in 10Mbps mode.	1, RW
7	JBEN	1 = enable jabber function. 0 = disable jabber function	1, RW
6	F_LINK_100	Used to login force good link in 100Mbps for diagnostic purposes. 1 = DISABLE, 0 = ENABLE.	1, RW
5	F_Connect	Assertion of this bit forces the disconnect function to be bypassed.	0, RW
4	-	Reserved	-
3	Con_status	This bit indicates the status of the connection. 1 = valid connected link detected; 0 = disconnected link detected.	0, RO
2	Con_status_En	Assertion of this bit configures LED1 pin to indicate connection status.	0, RW
1	-	Reserved	-
0	PASS_SCR	Bypass Scramble	0, RW

5.28 MII Register (Offset 0082h, R/W)

Bit	R/W	Symbol	Description
7	R/W	MDM	Management Data Mode: Setting this bit indicates that MDIO pin is output, and the state of MDIO pin reflects with MDO bit. When this pin is reset, MDIO pin is input. MDI bit reflects the state of

			MDIO pin. The default value is "0".
6-3	-	-	RESERVED
2	R/W	MDO	MII Management Data-OUT: Used by the RTL8130 to write data to the MDIO pin.
1	R/W	MDI	MII Management Data-IN: Used by the RTL8130 to read data from the MDIO pin.
0	R/W	MDC	Management Data Clock: This bit reflects the state of MDC pin.

5.29 Flash Memory Read/Write Register (Offset 00D4h-00D7h, R/W)

Bit	R/W	Symbol	Description
31-24	R/W	MD7-MD0	Flash Memory Data Bus: These bits set and reflect the state of the MD7 - MD0 pins, during write and read process respectively.
23-21	-	-	Reserved.
20	W	ROMCSB	Chip Select: This bit sets the state of the ROMCSB pin.
19	W	OEB	Output Enable: This bit sets the state of the OEB pin.
18	W	WEB	Write Enable: This bit sets the state of the WEB pin.
17	W	SWRWEn	Enable software access to flash memory: 0: Disable read/write access to flash memory via software. 1: Enable read/write access to flash memory via software and disable the EEPROM access during flash memory access via software.
16-0	W	MA16-MA0	Flash Memory Address Bus: These bits set the state of the MA16-0 pins.

6. EEPROM 93C46 Contents

The 93C46 is a 1K-bit EEPROM. Although it is actually addressed by words, we list its contents by bytes below for convenience.
After the valid duration of the RSTB pin or auto-load command in 9346CR, the RTL8130 performs a series of EEPROM read operation from the 93C46 address 00H to 3DH.

Bytes	Contents	Description
00h 01h	29h 81h	These 2 bytes contain ID code word for the RTL8130. The RTL8130 will load the contents of EEPROM into the corresponding location if the ID word (8129h) is right, otherwise, the Vendor ID and Device ID of the PCI configuration space are "10ECh" and "8129h".
02h-03h	VID	PCI Vendor ID, PCI configuration space offset 00h-01h.
04h-05h	DID	PCI Device ID, PCI configuration space offset 02h-03h.
06h-07h	SVID	PCI Subsystem Vendor ID, PCI configuration space offset 2Ch-2Dh.
08h-09h	SMID	PCI Subsystem ID, PCI configuration space offset 2Eh-2Fh.
0Ah	MNGNT	PCI Minimum Grant Timer, PCI configuration space offset 3Eh.
0Bh	MXLAT	PCI Maximum Latency Timer, PCI configuration space offset 3Fh.
0Ch	MSRBMCR	Bit7-6 map to the bit7-6 of MSR register, Bit5, 4, 3, 2, 0 map to the bit13, 12, 11, 10, 8 of Basic Mode Control register, Bit1 is reserved.
0Dh	CONFIG3	RTL8130 Configuration register 3, operational register offset 59H.
0Eh-13h	Ethernet ID	Ethernet ID, After auto-load command or hardware reset, RTL8130 loads Ethernet ID

		to IDR0-IDR5 of RTL8130's.
14h	CONFIG0	RTL8130 Configuration register 0, operational registers offset 51h.
15h	CONFIG1	RTL8130 Configuration register 1, operational registers offset 52h.
16h - 17h	PMC	Power Management Capabilities. PCI configuration space address 52h and 53h.
18h	PMCSR	Power Management Control/Status. PCI configuration space address 55h.
19h	CONFIG4	RTL8130 Configuration register 4, operational registers offset 5Ah.
1Ah - 1Dh	PHY1_PARM	PHY Parameter 1. Operational registers of the RTL8130 are from 78h to 7Bh.
1Eh	PHY2_PARM	PHY Parameter 2. Operational register of the RTL8130 is 80h.
1Fh	-	Reserved
20h - 2Dh	TW1_PARM	Twister Parameter 1. Operational registers offset of the RTL8130 is 7Ch.
30h - 3Dh	TW2_PARM	Twister Parameter 2. Operational registers offset of the RTL8130 is 7Ch.
38h - 7Fh	-	Reserved

6.1 Summary of RTL8130's registers in the EEPROM(9346)

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h-05h	IDR0 – IDR5	R/W*								
51h	CONFIG0	R		-	-	-	-	BS2	BS1	BS0
		W*	-	-	-	-	-	-	-	-
52h	CONFIG1	R	LEDS1	LEDS0	DVRLOAD	-	MEMMAP	IOMAP	-	PMEN
		W*	LEDS1	LEDS0	DVRLOAD	-	-	-	-	PMEN
58h	MSR	R	TxFCE	RxFCE	-	-	-	-		
		W	TxFCE	RxFCE	-	-	-	-		
62H	BMCR	R	-	-	Spd_Set	ANE	MLinkActiveState	MDupActiveState	-	FUDUP
		W	-	-	Spd_Set	ANE	MLinkActiveState	MDupActiveState	-	FUDUP
59h	CONFIG3	R	GNTDel	PARM_EN	Magic	LinkUp	Medium1	Medium0	MIIorAUI	FBtBEn
		W	-	PARM_EN	Magic	LinkUp	Medium1	Medium0	-	-
5Ah	CONFIG4	R/W*	-	-	LongWF	LWPME	MSWFB	LWPTN	PARM_En2	-
78h-7Bh	PHY1_PARM	R/W**	32 bit Read Write							
7Ch-7Fh	TW1_PARM TW2_PARM	R/W**	32 bit Read Write 32 bit Read Write							
80h	PHY2_PARM	R/W**	8 bit Read Write							

* The registers marked with type = 'W*' can be written only if bits EEM1=EEM0=1.

** The registers marked with type = 'W**' can be written only if bits EEM1=EEM0=1 and CONFIG3<PARM_EN> = 0.

6.2 Summary of Power Management registers in the EEPROM

Configuration Space offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
53h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
55h	PMCSR	R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En

7. PCI Configuration Space Registers

7.1 PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	0	-	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	FBTBEN	SERREN
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	FBBC	0	0	NewCap	0	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	DST1	DST0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R	0	0	0	0	0	0	0	0
0Dh	LTR	R	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		R/W	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		R/W	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		R/W	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h	MEMAR	R	0	0	0	0	0	0	0	MEMIN
		W	-	-	-	-	-	-	-	-
15h		R/W	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
16h		R/W	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
17h		R/W	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
18h-27h	RESERVED									
28h-2Bh	RESERVED									

2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		R/W	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	0	1	0	1	0	0	0	0
35h-3Bh	RESERVED									
3Ch	ILR	R/W	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h–4Fh	RESERVED									
50h	PMID	R	0	0	0	0	0	0	0	1
51h	NextPtr	R	0	0	0	0	0	0	0	0
52h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
53h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
54h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
55h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
56h-FFh	RESERVED									

7.2 PCI Configuration Space functions

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of RTL8130's configuration space are described below.

VID: Vendor ID. This field will be set to a value corresponding to PCI Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh which is Realtek Semiconductor's PCI Vendor ID.

DID: Device ID. This field will be set to a value corresponding to PCI Device ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

Command: The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Bit	Symbol	Description
15-10	-	Reserved
9	FBTBEN	Fast Back-To-Back Enable: Config3<FBtBEn>=0:Read as 0. Write operation has no effect. The RTL8130 will not generate Fast Back-to-back cycles. When Config3<FbtBEn>=1, This read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of 1 means

		the master is allowed to generate fast back-to-back transaction to different agents. A value of 0 means fast back-to-back transactions are only allowed to the same agent. This bit's state after RST# is 0.
8	SERREN	System Error Enable: When set to 1, the RTL8130 asserts the SERRB pin when it detects a parity error on the address phase (AD<31:0> and CBEB<3:0>).
7	ADSTEP	Address/Data Stepping: Read as 0, write operation has no effect. The RTL8130 never make address/data stepping.
6	PERRSP	Parity Error Response: When set to 1, RTL8130 will assert the PERRB pin on the detection of a data parity error when acting as the target, and will sample the PERRB pin as the master. When set to 0, any detected parity error is ignored and the RTL8130 continues normal operation. Parity checking is disabled after hardware reset (RSTB).
5	VGASNOOP	VGA palette SNOOP. Read as 0, write operation has no effect.
4	MWIEN	Memory Write and Invalidate cycle Enable: Read as 0, write operation has no effect.
3	SCYCEN	Special Cycle Enable: Read as 0, write operation has no effect. The RTL8130 ignores all special cycle operation.
2	BMEN	Bus Master Enable: When set to 1, the RTL8130 is capable of acting as a bus master. When set to 0, it is prohibited from acting as a PCI bus master. For the normal operation, this bit must be set by the system BIOS.
1	MEMEN	Memory Space Access: When set to 1, the RTL8130 responds to memory space accesses. When set to 0, the RTL8130 ignores memory space accesses.
0	IOEN	I/O Space Access: When set to 1, the RTL8130 responds to IO space access. When set to 0, the RTL8130 ignores I/O space accesses.

Status: The status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Bit	Symbol	Description
15	DPERR	Detected Parity Error: When set indicates that the RTL8130 detected a parity error, even if parity error handling is disabled in command register PERRSP bit.
14	SSERR	Signaled System Error: When set indicates that the RTL8130 asserted the system error pin, SERRB. Writing a 1 clears this bit to 0.
13	RMABT	Received Master Abort: When set indicates that the RTL8130 terminated a master transaction with master abort. Writing a 1 clears this bit to 0.
12	RTABT	Received Target Abort: When set indicates that the RTL8130 master transaction was terminated due to a target abort. Writing a 1 clears this bit to 0.
11	STABT	Signaled Target Abort: Set to 1 whenever the RTL8130 terminates a transaction with target abort. Writing a 1 clears this bit to 0.
10-9	DST1-0	Device Select Timing: These bits encode the timing of DEVSELB. They are set to 01b (medium), indicating the RTL8130 will assert DEVSELB two clocks after FRAMEB is asserted.
8	DPD	Data Parity error Detected: This bit sets when the following conditions are met: °The RTL8130 asserts parity error(PERRB pin) or it senses the assertion of PERRB pin by another device. ¡ °The RTL8130 operates as a bus master for the operation that caused the error. ¡ °The Command register PERRSP bit is set. Writing a 1 clears this bit to 0.
7	FBBC	Fast Back-To-Back Capable: Config3<FbtBEn>=0, Read as 0, write operation has no effect. Config3<FbtBEn>=1, Read as 1.
6	UDF	User Definable Features Supported: Read as 0, write operation has no effect. The RTL8130 does not support UDF.
5	66MHz	66 MHz Capable: Read as 0, write operation has no effect. The RTL8130 has no 66MHz capability.

4	NewCap	New Capability: Config3<PMEn>=0, Read as 0, write operation has no effect. Config3<PMEn>=1, Read as 1.
0-3	-	Reserved

RID: Revision ID Register

The Revision ID register is an 8-bit register that specifies the RTL8130 controller revision number.

PIFR: Programming Interface Register

The programming interface register is an 8-bit register that identifies the programming interface of the RTL8130 controller. The PCI specification reversion 2.1 doesn't define any other specific value for network devices. So PIFR = 00h.

SCR: Sub-Class Register

The Sub-class register is an 8-bit register that identifies the function of the RTL8130. SCR = 00h indicates that the RTL8130 is an Ethernet controller.

BCR: Base-Class Register

The Base-class register is an 8-bit register that broadly classifies the function of the RTL8130. BCR = 02h indicates that the RTL8130 is a network controller.

CLS: Cache Line Size

Reads will return a 0, writes are ignored.

LTR: Latency Timer Register

Specifies, in units of PCI bus clocks, the value of the latency timer of the RTL8130.

When the RTL8130 asserts FRAMEB, it enables its latency timer to count. If the RTL8130 deasserts FRAMEB prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the RTL8130 initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write, and the default value is 00H.

HTR: Header Type Register

Reads will return a 0, writes are ignored.

BIST: Built-in Self Test

Reads will return a 0, writes are ignored.

IOAR: This register specifies the BASE IO address which is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into IO space.

Bit	Symbol	Description
31-7	IOAR31-7	BASE IO Address: This is set by software to the Base IO address for the operational register map.
6-2	IOSIZE	Size Indication: Read back as 0. This allows the PCI bridge to determine that the RTL8130 requires 128 bytes of IO space.
1	-	Reserved
0	IOIN	IO Space Indicator: Read only. Set to 1 by the RTL8130 to indicate that it is capable of being mapped into IO space.

MEMAR: This register specifies the base memory address for memory accesses to the RTL8130 operational registers. This register must be initialized prior to accessing any RTL8130's register with memory access.

Bit	Symbol	Description
31-7	MEM31-7	Base Memory Address: This is set by software to the base address for the operational register map.
6-4	MEMSIZE	Memory Size: These bits return 0, which indicates that the RTL8130 requires 128 bytes of Memory Space.
3	MEMPF	Memory Prefetchable: Read only. Set to 0 by the RTL8130.
2-1	MEMLOC	Memory Location Select: Read only. Set to 0 by the RTL8130. This indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space.
0	MEMIN	Memory Space Indicator: Read only. Set to 0 by the RTL8130 to indicate that it is capable of being mapped into memory space.

SVID: Subsystem Vendor ID. This field will be set to a value corresponding to PCI Subsystem Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 11ECh which is Realtek Semiconductor's PCI Subsystem Vendor ID.

SMID: Subsystem ID. This field will be set to value corresponding to PCI Subsystem ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

BMAR: This register specifies the base memory address for memory accesses to the RTL8130 operational registers. This register must be initialized prior to accessing any RTL8130's register with memory access.

Bit	Symbol	Description
31-18	BMAR31-18	Boot ROM Base Address
17-11	ROMSIZE	These bits indicate how many Boot ROM spaces to be supported. The Relationship between Config 0 <BS2:0> and BMAR17-11 is the following: **BS2 BS1 BS0 Description** 0 0 0 No Boot ROM, BROMEN=0 (R) 0 0 1 8K Boot ROM, BROMEN (R/W), BMAR12-11 = 0 (R), BMAR17-13 (R/W) 0 1 0 16K Boot ROM, BROMEN (R/W), BMAR13-11 = 0 (R), BMAR17-14 (R/W) 0 1 1 32K Boot ROM, BROMEN (R/W), BMAR14-11 = 0 (R), BMAR17-15 (R/W) 1 0 0 64K Boot ROM, BROMEN (R/W), BMAR15-11 = 0 (R), BMAR17-16 (R/W) 1 0 1 128K Boot ROM, BROMEN(R/W), BMAR16-11=0 (R), BMAR17 (R/W) 1 1 0 unused 1 1 1 unused
10-1	-	Reserved (read back 0)
0	BROMEN	Boot ROM Enable: This is used by the PCI BIOS to enable accesses to Boot ROM.

ILR: Interrupt Line Register

The Interrupt Line Register is an 8-bit register used to communicate with the routing of the interrupt. It is written by the POST software to set interrupt line for the RTL8130.

IPR: Interrupt Pin Register

The Interrupt Pin register is an 8-bit register indicating the interrupt pin used by the RTL8130. The RTL8130 uses INTA interrupt pin. Read only. IPR = 01H.

MNGNT: Minimum Grant Timer: Read only

Specifies how long a burst period the RTL8130 needs at 33 MHz clock rate in units of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

MXLAT: Maximum Latency Timer: Read only

Specifies how often the RTL8130 needs to gain access to the PCI bus in unit of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

7.3 The Default Value after Power-on (RSTB asserted)

PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	1	1	1	0	1	1	0	0
01h		R	0	0	0	1	0	0	0	0
02h	DID	R	0	0	1	0	1	0	0	1
03h		R	1	0	0	0	0	0	0	1
04h	Command	R	0	0	0	0	0	0	0	0
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	0	0	0	NewCap	0	0	0	0
07h		R	0	0	0	0	0	0	1	0
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R	0	0	0	0	0	0	0	0
0Dh	LTR	R	0	0	0	0	0	0	0	0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	1
11h		R/W	0	0	0	0	0	0	0	0
12h		R/W	0	0	0	0	0	0	0	0
13h		R/W	0	0	0	0	0	0	0	0
14h	MEMAR	R	0	0	0	0	0	0	0	0
15h		R/W	0	0	0	0	0	0	0	0
16h		R/W	0	0	0	0	0	0	0	0
17h		R/W	0	0	0	0	0	0	0	0
18h | 2Bh	-	RESERVED(ALL 0)								
2Ch	SVID	R	1	1	1	0	1	1	0	0
2Dh		R	0	0	0	1	0	0	0	1
2Eh	SMID	R	0	0	1	0	1	0	0	1
2Fh		R	1	0	0	0	0	0	0	1
30h	BMAR	R	0	0	0	0	0	0	0	0

		W	-	-	-	-	-	-	-	BROMEN
31h		R	0	0	0	0	0	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	0	0	0	0	0	0	0	0
33h		R/W	0	0	0	0	0	0	0	0
34h	Cap-Ptr	R	Ptr7	Ptr6	Ptr5	Ptr4	Ptr3	Ptr2	Ptr1	Ptr0
35h | 3Bh	-	RESERVED(ALL 0)								
3Ch	ILR	R/W	0	0	0	0	0	0	0	0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h | FFh	-	RESERVED(ALL 0)								

7.4 PCI Power Management functions

The RTL8130 is compliant to ACPI (Rev 1.0), PCI Power Management (Rev 1.0), and Device Class Power Management Reference Specification (V1.0a), such as to support OS Directed Power Management (OSPM) environment. To support this, the RTL8130 provides the following capabilities:

- The RTL8130 can monitor the network for a Wakeup Frame, a Magic Packet, or a Link Change, and notify the system via PME# when such a packet or event arrives. Then, the whole system can restore to working state to process the incoming jobs.
- The RTL8130 can be isolated from the PCI bus automatically with the auxiliary power circuit when the PCI bus is in B3 state, i.e. the power on the PCI bus is removed. When in the application of motherboard with built-in RTL8130 single-chip fast ethernet controller, the RTL8130 can be disabled when needed by pulling low the isolate pin to 0V.

When the RTL8130 is in power down mode (D1 ~ D3),

- The Rx state machine is stopped, and the RTL8130 keeps monitoring the network for wakeup event such Magic Packet, Wakeup Frame, and/or Link Change, in order to wake up the system. When in power down mode, the RTL8130 will not reflect the status of any incoming packet in the ISR register and will not receive any packet into Rx FIFO.
- The FIFO status and the packets which are already received into Rx FIFO before entering into power down mode, are kept by the RTL8130 during power down mode
- The transmission is stopped. The action of PCI bus master mode is stopped, too. The Tx FIFO is kept.
- After restoring to D0 state, the PCI bus master mode continues to transfer the data, which is not yet moved into Tx FIFO from the last break. The packet that was not transmitted completely last time is transmitted again.

Link Wakeup occurs only when the following conditions are approved,

- The LinkUp bit (CONFIG3#4) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the RTL8130 is in isolation state, or the PME# can be asserted in current power state.
- The Link status is re-established.

Magic Packet Wakeup occurs only when the following conditions are approved,

- The destination address of the received magic packet matches.
- The received Magic Packet does not contain CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the RTL8130 is in isolation state, or the PME# can be asserted in current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + 16 * DID(Destination ID).

Wakeup Frame event occurs only when the following conditions are approved,

- The MSWFB bit (CONFIG3#4) is set to 0.
- The destination address of the received Wakeup Frame matches.
- The received Wakeup Frame does not contain CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The ***8-bit CRC**** of the received Wakeup Frame matches with the ***8-bit CRC**** of the sample Wakeup Frame pattern received from the local machine's OS.
- The ***last masked byte**** of the received Wakeup Frame matches with the ***last masked byte**** of the sample Wakeup Frame pattern provided by the local machine's OS.

* **8-bit CRC:** This 8-bit CRC logic is to generate an 8-bit CRC from the masked bytes of the received Wakeup Frame packet within offset 12 to 75 (or offset 12 to 139, for Long Wakeup Frames), i.e., the 64 (or 128) bytes starting from the byte of Type/Length field. Software should calculate the 8-bit Power Management CRC for each specific sample wakeup frame and store the calculated CRC in the corresponding CRC register for the RTL8130 to check if there is Wakeup Frame packet coming in.

Long Wakeup Frame: The RTL8130 also supports 3 long Wakeup Frames. If the range of mask bytes of the sample Wakeup Frame, passed down by the OS to the driver, exceeds the range from offset 12 to 75, the related registers of wakeup frame 2 and 3 can be merged to support one long wakeup frame by setting the LongWF (bit0, CONFIG4). Thus, the range of effective mask bytes extends from offset 12 to 139. The calculated 8-bit CRC and the last masked byte from the long sample wakeup frame should be put into register CRC2 and LSBCRC2 respectively. The mask bytes (16 bytes) should be store to register Wakeup2 and Wakeup3. The CRC3 and LSBCRC3 have no meaning in this case and should be reset to 0. So as the long Wakeup Frame pairs, wakeup frame 4 and 5, wakeup frame 6 and 7. The CRC5, CRC7, LSBCRC5, and LSBCRC7 have no meaning in this case and should be reset to 0, if the RTL8130 is set to support long Wakeup

Frame. In this case, the RTL8130 support 5 wakeup frames, that are 2 normal wakeup frames and 3 long wakeup frames.

** **last masked byte:** The last byte of the masked bytes of the received Wakeup Frame packet within offset 12 to 75 (or offset 12 to 139, in Long Wakeup Frame mode) should matches with the last byte of the masked bytes of the sample Wakeup Frame provided by the local machine's OS.

The PME# signal is asserted only when the following are approved,

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8130 may assert PME# in current power state, or the RTL8130 is in isolation state. Refer to PME_Support(bit15-11) of the PMC register in PCI Configuration Space.
- Magic Packet, LinkUp, or Wakeup Frame has occurred.

  * Writing a 1 to the PME_Status (bit15) of PMCSR register in the PCI Configuration Space will clear this bit and cause the RTL8130 to stop asserting a PME# (if enabled).

When the RTL8130 is in power down mode, ex. D1-D3, the IO, MEM, and Boot ROM space are all disabled. After RST# asserted, the power state must be changed to D0 if the original power state is $D3_{cold}$. There is no hardware enforced delays at RTL8130's power state. When in ACPI mode, the RTL8130 does not support PME from D0 (owing to the setting of PMC register. This setting comes from EEPROM).

The RTL8130 also supports LAN WAKE-UP function. The LWAKE pin is used to notify the motherboard to execute wake-up process whenever the RTL8130 receives a wakeup event, such as Magic packet.

The LWAKE is asserted according to the same condition as the PME#'s and the setting of LWPME bit,

- LWPME bit (bit4, CONFIG4):

  0: The LWAKE and PMEB are asserted at the same time.

  1: The LWAKE can only be asserted when the PMEB is asserted and the ISOLATEB is low.

8. Functional Description

8.1 Transmit operation

The host CPU initiates a transmit by storing an entire packet of data in one of the descriptors in the main memory. When the entire packet has been transferred to the Tx buffer, the RTL8130 is instructed to move the data from the Tx buffer to the internal transmit FIFO in PCI bus master mode. When the transmit FIFO contains a complete packet or is filled to the programmed threshold level, the RTL8130 begins packet transmission.

8.2 Receive operation

The incoming packet is placed in the RTL8130's Rx FIFO. Concurrently, the RTL8130 performs address filtering of multicast packets according to its hash algorithms. When the amount of data in the Rx FIFO reaches the level defined in the Receive Configuration Register, the RTL8130 requests the PCI bus to begin transferring the data to the Rx buffer.

8.3 Loopback Operation

The RTL8130 supports two loopback modes : internal loopback and external loopback.

8.3.1 Internal Loopback Mode

Internal loopback mode is normally used to verify that the internal logic functions correctly. In loopback mode, the RTL8130 takes frames from the transmit descriptor and loops them back internally to the receive descriptor. In loopback mode, the RTL8130 disconnects from the Ethernet cable.

8.3.2 External Loopback Mode

External loopback mode is normally used to verify that the logic operations up to the Ethernet cable function correctly. In external loopback mode for 100Mbps, the RTL8130 takes frames from the transmit descriptor and transmits them to clock generator/recovery interface.

8.4 Tx Encapsulation

While operating either in 100Base-Tx mode, the RTL8130 encapsulates the frames that it transmits according to the 4B/5B code-groups table. The changes of the original packet data are listed as follows :

1. The first byte of the preamble in the MAC frame is replaced with the JK symbol pair.

2. After the CRC, the TR symbol pair is inserted.

8.5 Collision

If the RTL8130 is not in the full-duplex mode, a collision event occurs when the receive input is not idle while the RTL8130 transmits. If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble (including the JK symbol pair).

8.6 Rx Decapsulation

The RTL8130 continuously monitors the network when reception is enabled. When activity is recognized it starts to process the incoming data.

After detecting receive activity on the line, the RTL8130 starts to process the preamble bytes based on the mode of operation.

While operating in 100Base-Tx mode, the RTL8130 expects the frame to start with the symbol pair JK in the first bye of the 8-byte preamble.

The RTL8130 checks the CRC bytes and checks if the packet data ends with the TR symbol pair, if not, the RTL8130 reports an CRC error RSR.

The RTL8130 reports a RSR<CRC> error in any of the following cases :

1. In the 100Base-Tx mode, one of the following occur.

a. An invalid symbol (4B/5B Table) is received in the middle of the frame.
RSR<ISE> bit also sets.

b. The frame does not end with the TR symbol pair.

8.7 Flow Control

The RTL8130 supports IEEE802.3X flow control to improve performance in full-duplex mode. It detects PAUSE packet to achieve flow control task.

8.7.1. Control Frame Transmission

When RTL8130 detects its free receive buffer less than 3K bytes, it sends a **PAUSE packet with pause_time(=FFFFh)** to inform the source station to stop transmission for the specified period of time. After the driver has processed the packets in the receive buffer and updated the boundary pointer, the RTL8130 sends the other **PAUSE packet with pause_time(=0000h)** to wake up the source station to restart transmission.

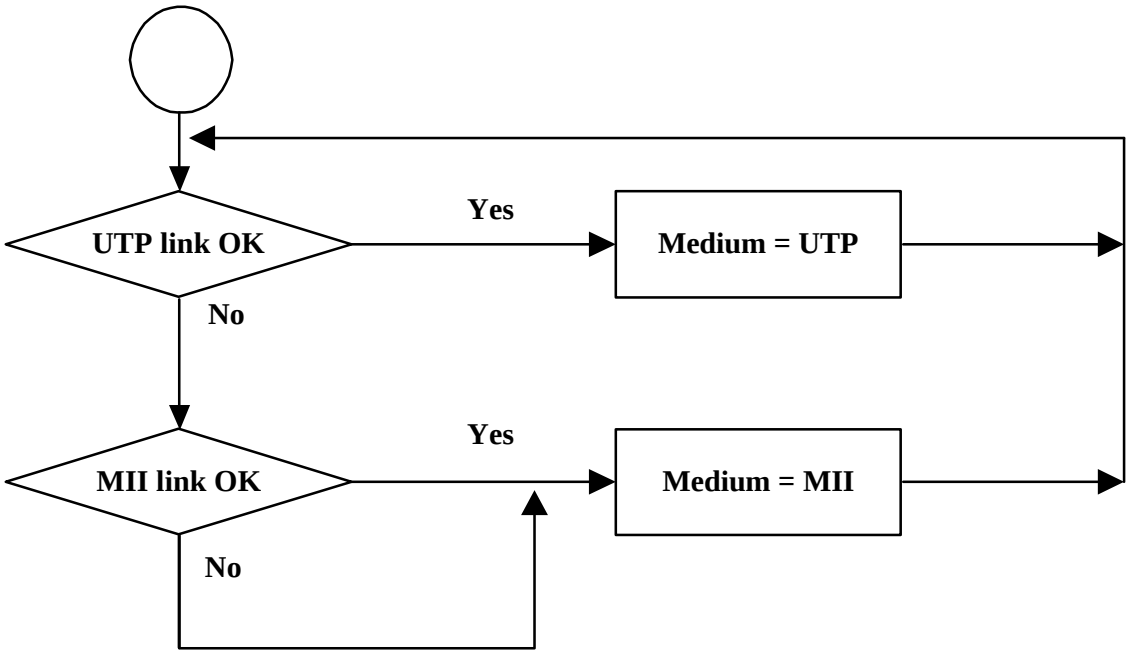
8.7.2. Control Frame Reception

RTL8130 enters backoff state for the specified period of time when it receives a valid **PAUSE packet with pause_time(=n)**. If the PAUSE packet is received while RTL8130 is transmitting, RTL8130 starts to backoff after current transmission completes. RTL8130 frees to transmit next packets again when it receives a valid **PAUSE packet with pause_time(=0000h)** or the **backoff timer(=n*512 bit time)** elapses.

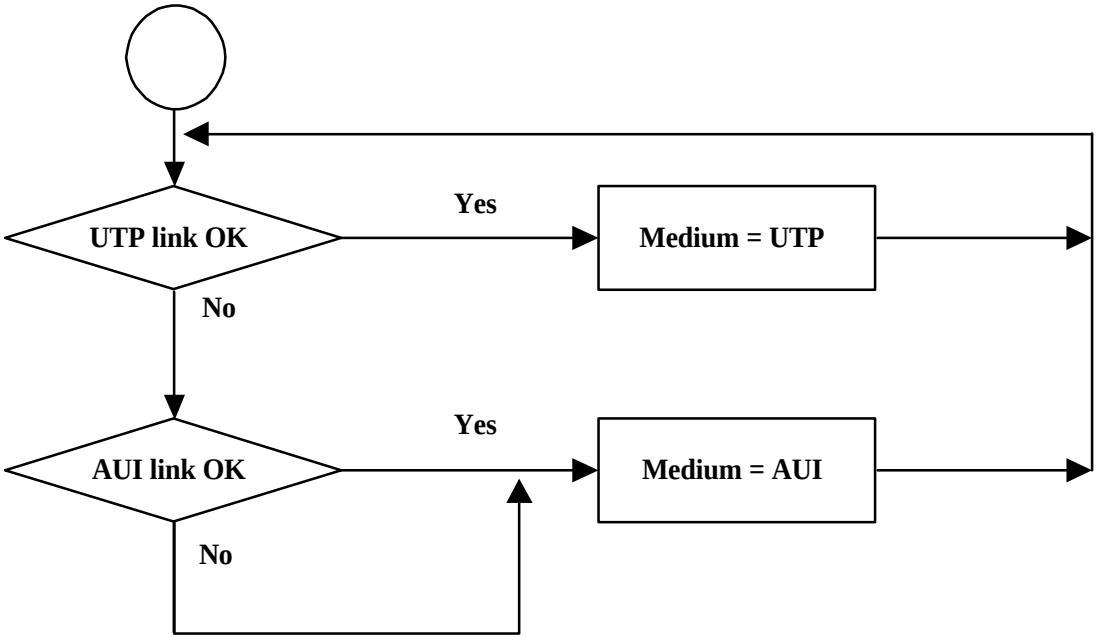
Note: The PAUSE operation cannot be used to inhibit transmission of MAC Control frames (e.g. PAUSE packet).

8.8 Medium auto-detect:

MII mode:



AUI mode:



8.9 Cable connection status:

- The statuses of Link, Speed(UTP & MII), and Duplex(UTP & MII) should be reflected to the relative registers when the medium is either UTP, MII, or AUI. This feature is not supported in UTP + standard external PHYceiver application with that the medium used is through standard external PHYceiver.
- Link change on any interface (including AUI) should generate an interrupt (LinkChg, bit5, ISR) to notify the drivers. This feature is not supported in UTP + standard external PHYceiver application with that the medium used is through standard external PHYceiver.
- Link Force Mode is effective only when UTP LinkOK. When UTP Link-Fail, and either MII or AUI LinkOK, the Link Force Mode does not change anything.

1. UTP: Same as RTL8139A.
2. MII:

   The states come from the PHYceiver. PHYceivers to be supported include Level-one LXT970, Davicom 9101, and NS DP83843.

   Link: by MLink pin 102

   If MLinkActiveState (bit11, BMCR) = 1,

   Then MLink=high means MII link OK

   If MLinkActiveState (bit11, BMCR) = 0,

   Then MLink=low means MII link OK

   MLinkActiveState can be auto-loaded from 9346.

   Duplex: by MFDup pin 101

   If MDupActiveState (bit10, BMCR) = 1

   Then MFDup=high means MII Duplex=Full

   If MDupActiveState (bit10, BMCR) = 0

   Then MFDup=low means MII Duplex=Full

   MDupActiveState can be auto-loaded from 9346.

   Speed: by MTXC

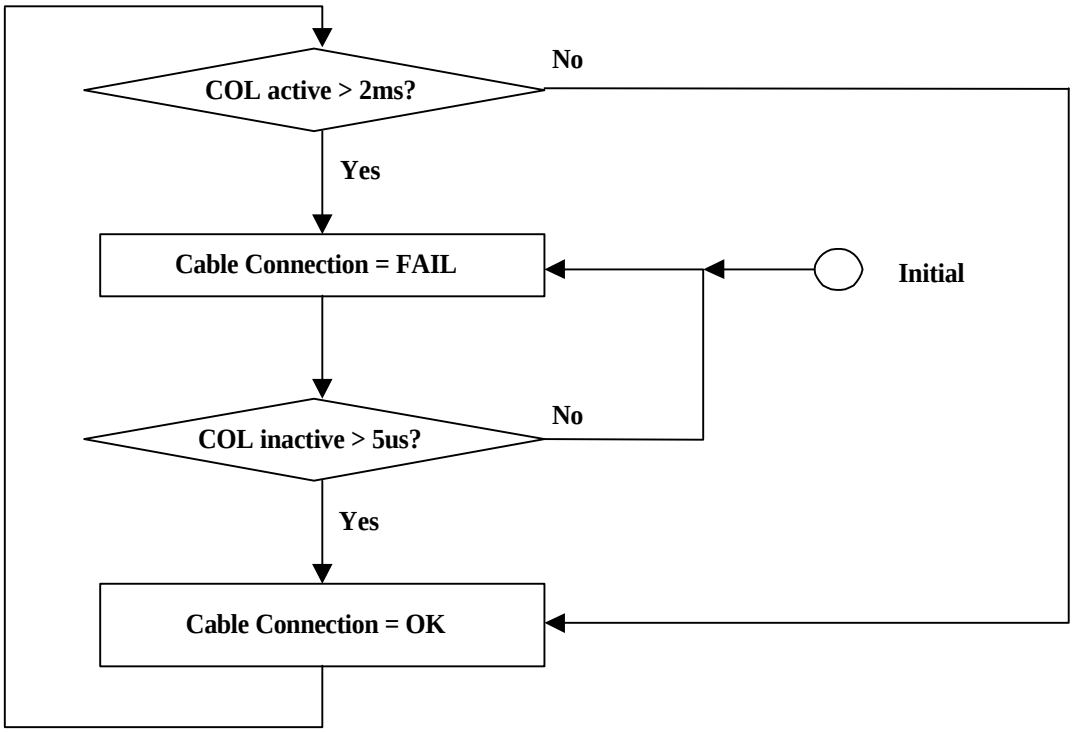
   If 2.5MHz (or 5Mhz), then Speed=10Mbps, otherwise, Speed=100Mbps.
3. AUI:

   Added pin: BNC pin92 (same as RTL8029AS)

   Duplex: If medium type = auto-detect, force to half

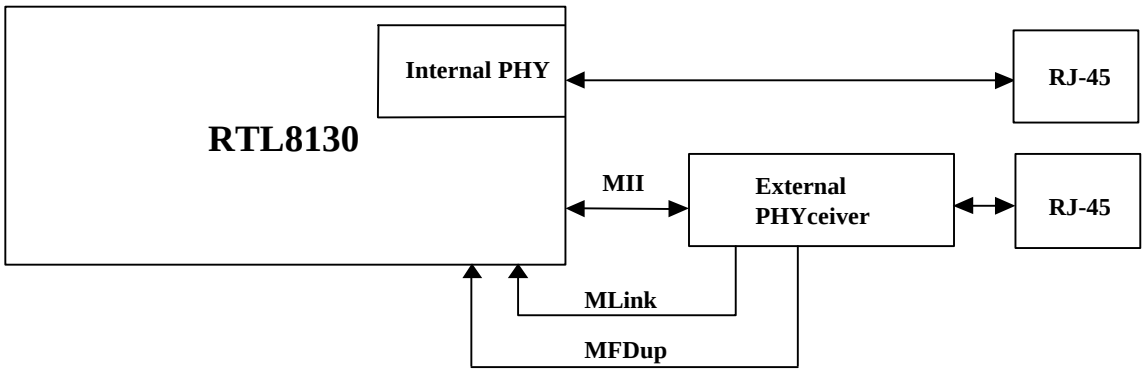
   If medium type = AUI, depends on the duplex bit (in 93C46 and register)

   Use CD+/- pins (i.e.) to detect the cable connection on AUI.

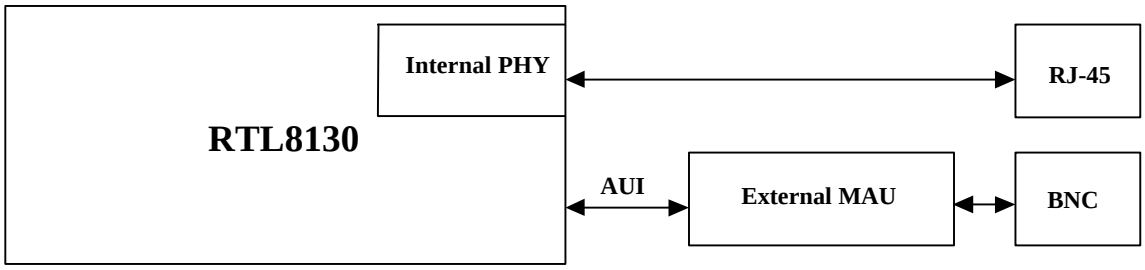


8.10 Redundant link:

MII mode:



AUI mode:



1. The driver must be able to test the status of both links at any time (or at least at initialization).
2. When both link are OK, the phone jack 1 is used.
   When phone jack 1 link fails, use phone jack2 in MII mode or BNC in AUI mode.

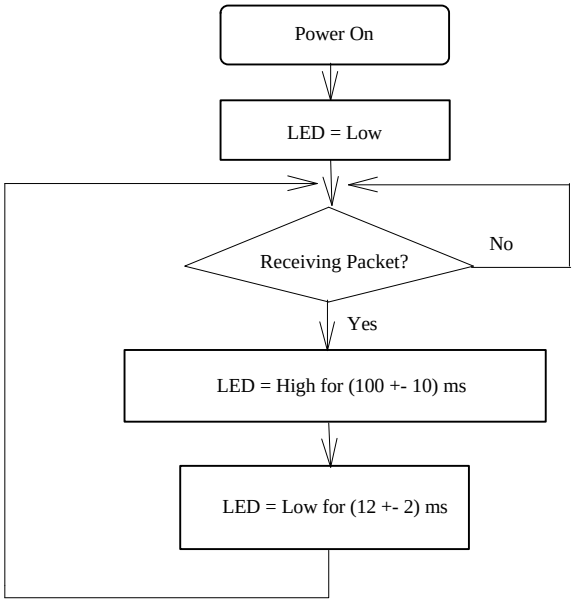
8.11 LED Functions

8.11.1 10/100 Mbps Link Monitor

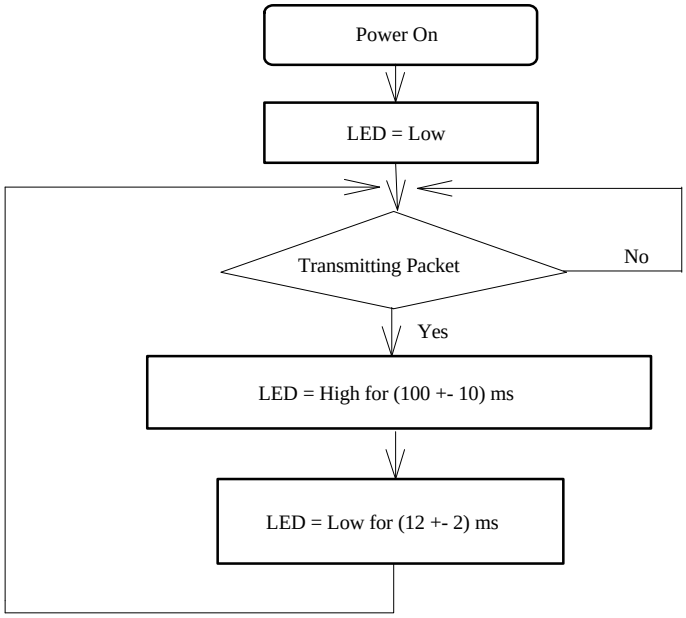
The Link Monitor senses the link integrity or if a station is down.

8.11.2 LED_RX

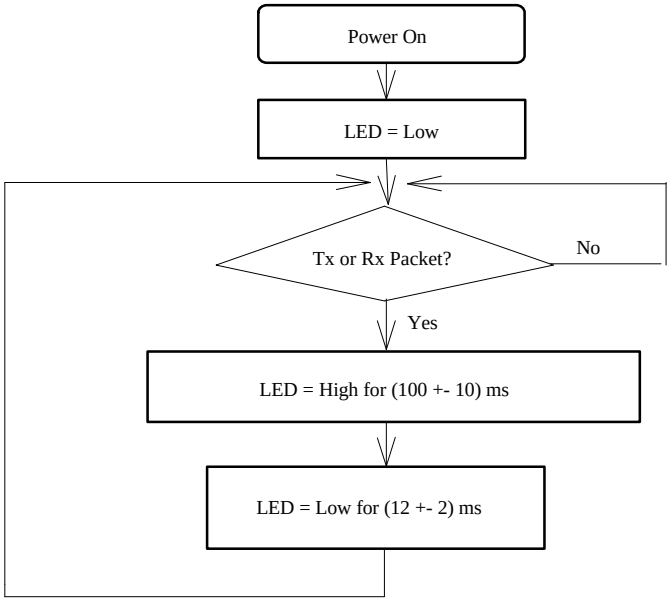
In 10/100 Mbps mode, the LED function is like RTL8130.



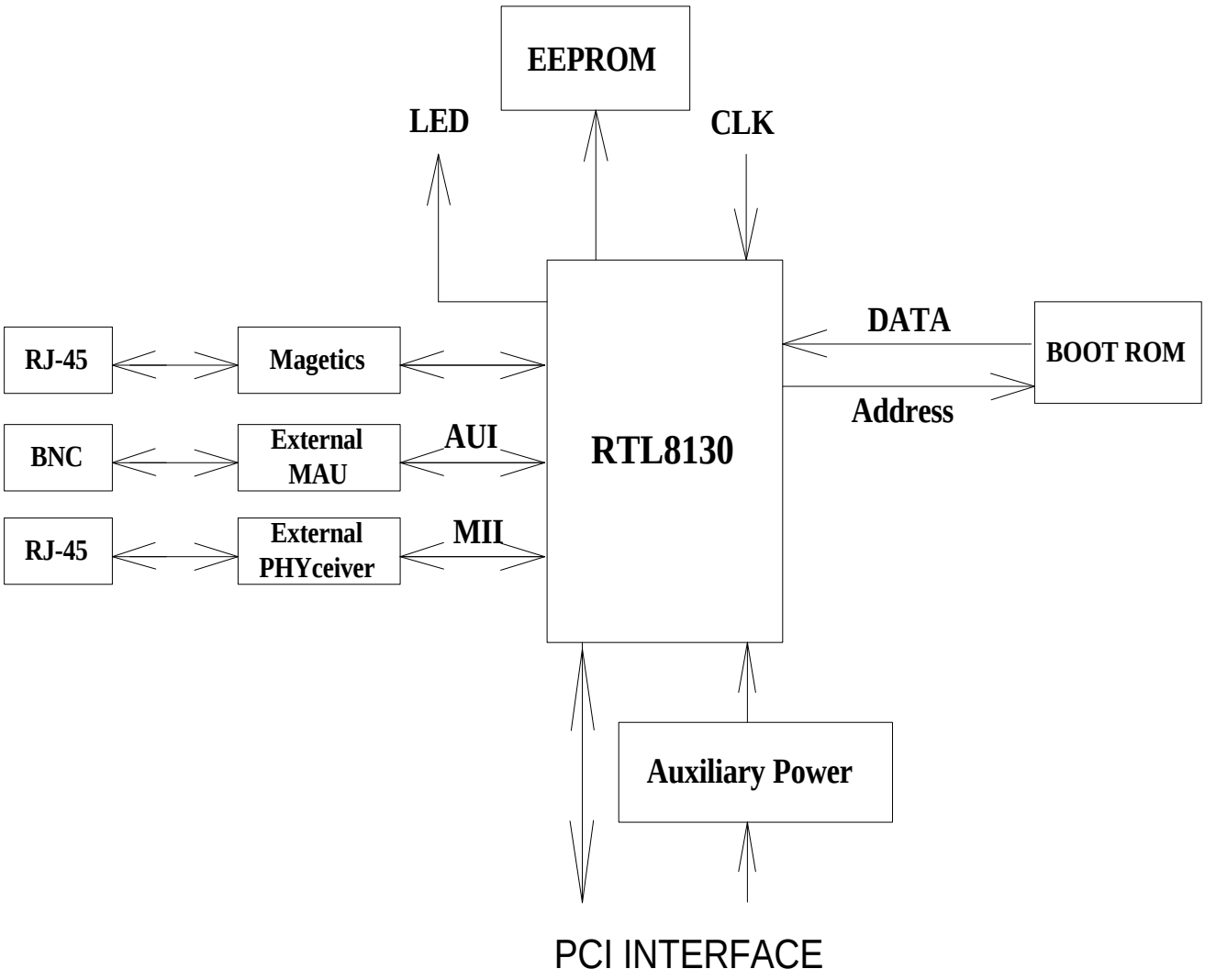
8.11.3 LED_TX



8.11.4 LED_TX+LED_RX



9. Application Diagram



10. ELECTRICAL CHARACTERISTICS

10.1 Temperature Limit Ratings:

Parameter	Minimum	Maximum	Units
Storage temperature	-55	+125	°C
Operating temperature	0	70	°C

10.2 DC CHARACTERISTICS:

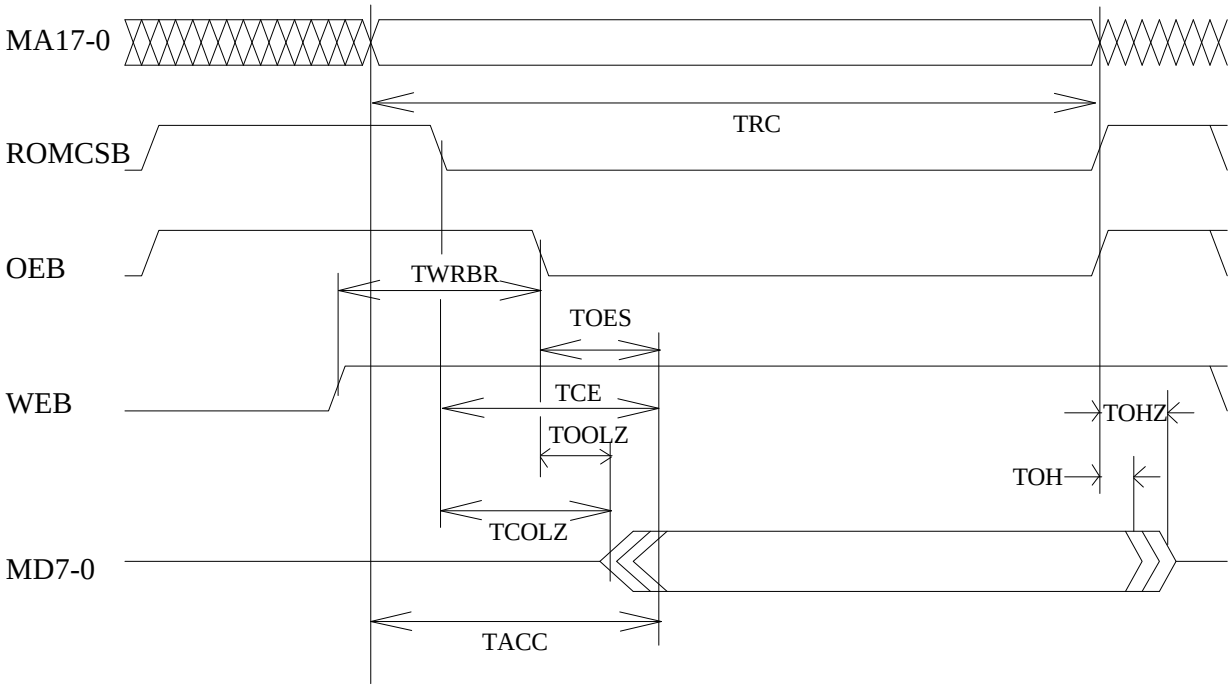
10.2.1 Supply voltage Vcc = 5V±5%

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{OH}	Minimum High Level Output Voltage	I_{OH}= -8mA	3	Vcc	V
V_{OL}	Maximum Low Level Output Voltage	I_{OL}= 8mA		0.4	V
V_{IH}	Minimum High Level Input Voltage		2.0	Vcc+0.5	V
V_{IL}	Maximum Low Level Input Voltage		-0.5	0.8	V
I_{IN}	Input Current	V_{IN}=V_{CC} or GND	-1.0	1.0	uA
I_{OZ}	Tri-State Output Leakage Current	V_{OUT}=V_{CC} or GND	-10	10	uA
I_{CC}	Average Operating Supply Current	I_{OUT}=0mA,		330	mA

10.3 AC CHARACTERISTICS

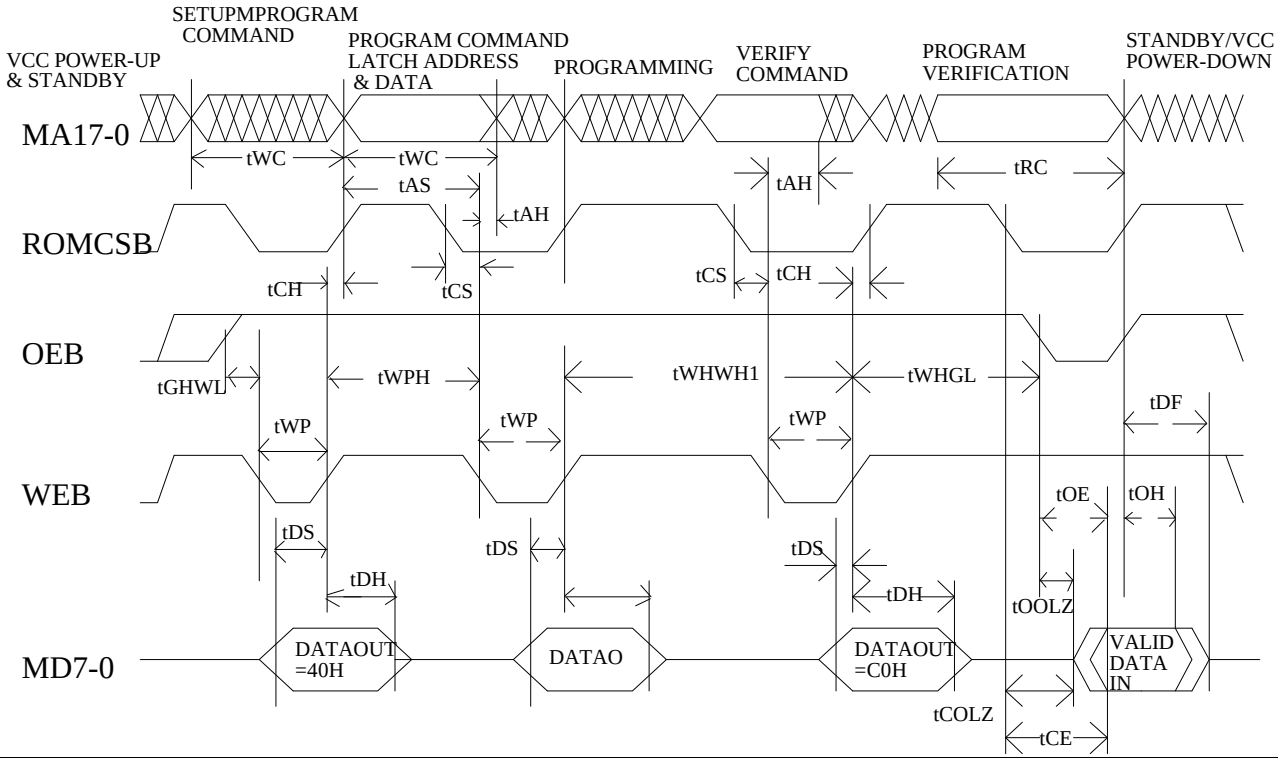
10.3.1 FLASH/BOOT ROM Timing

10.3.1.1 FLASH/BOOT ROM - Read



Symbol	Description	Minimum	Typical	Maximum	Units
TRC	Read Cycle	135	-	-	ns
TCE	Chip Enable Access Time	-	-	200	ns
TACC	Address Access Time	-	-	200	ns
TOES	Output Enable Access Time	-	-	60	ns
TCOLZ	Chip Enable to Output in Low Z	0	-	-	ns
TOOLZ	Output Enable to Output in Low Z	0	-	-	ns
TOHZ	Output Disable to Output in High Z	-	-	40	ns
TOH	Output Hold from Address, ROMCSB, or OEB	0	-	0	ns
TWRBR	Write Recovery time Before Read	6	-	-	us

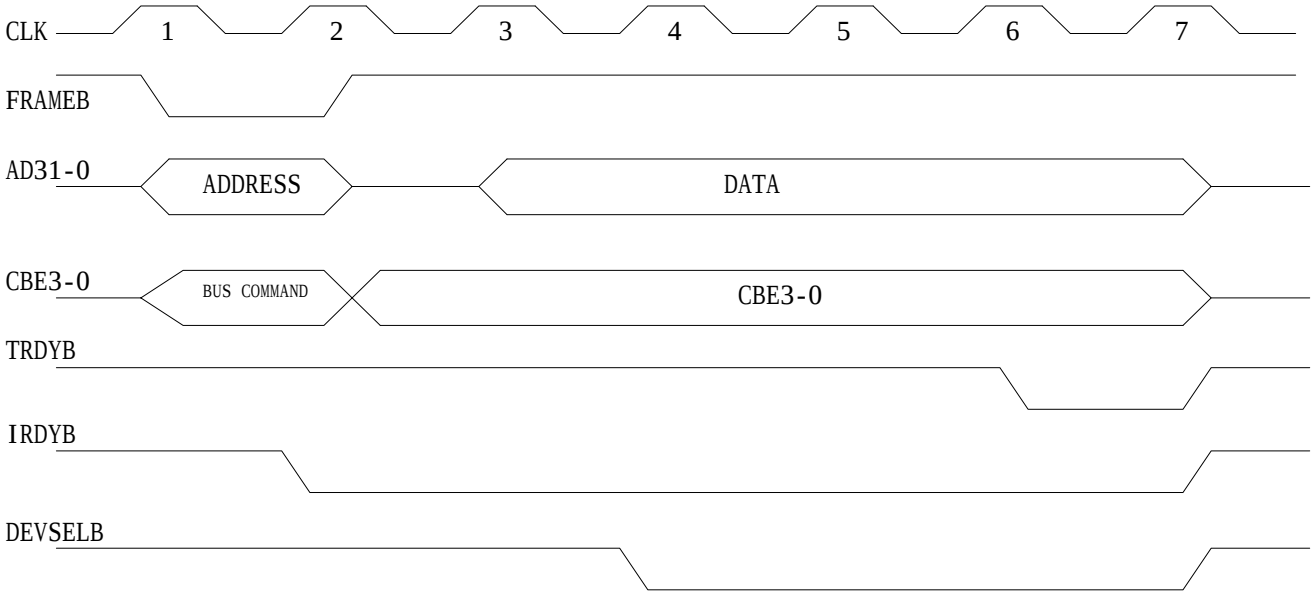
10.3..2 FLASH MEMORY - Write



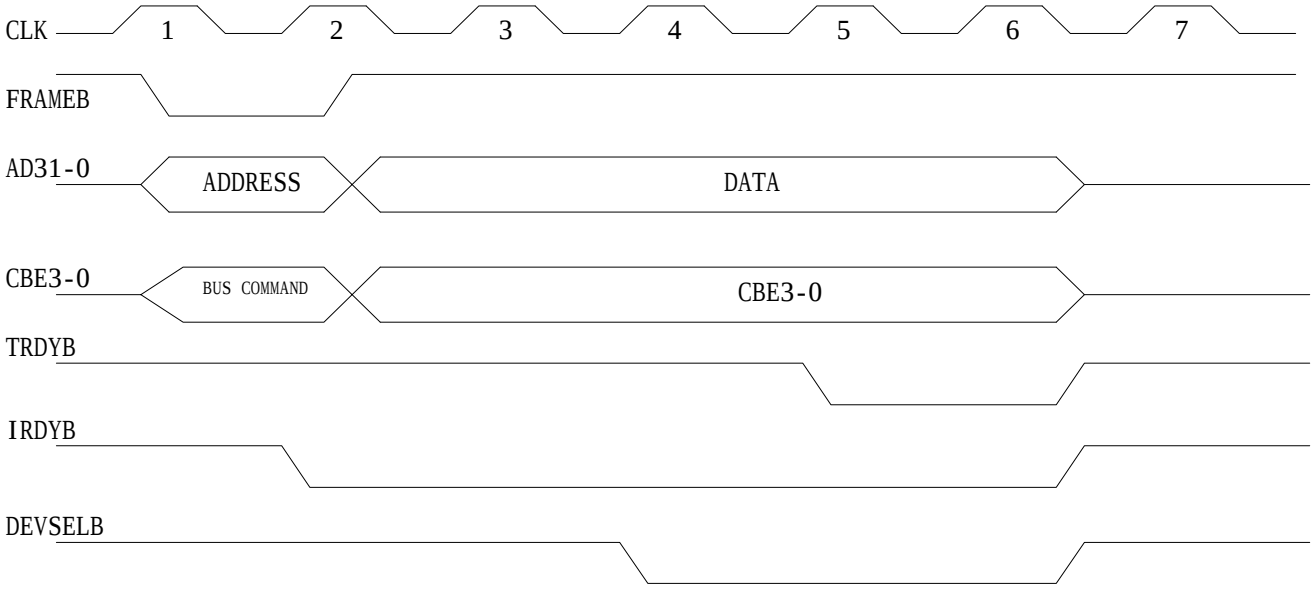
Symbol	Description	Minimum	Typical	Maximum	Units
TWC	Write Cycle Time	135	-	-	ns
TAS	Address Set-up Time	0	-	-	ns
TAH	Address Hold Time	60	-	-	ns
TDS	Data Set-up Time	50	-	-	ns
TDH	Data Hold Time	10	-	-	ns
TWHGL	Write Recovery Time before Read	6	-	-	us
TGHWL	Read Recovery Time before Write	0	-	-	us
TCS	Chip Enable Set-up Time before Write	20	-	-	ns
TCH	Chip Enable Hold Time	0	-	-	us
TWP	Write Pulse Width	50	-	-	ns
TWPH	Write Pulse Width High	20	-	-	ns
TWHWH1	Duration of Programming Operation	10	-	25	us

10.3.2 PCI Bus Operation Timing:

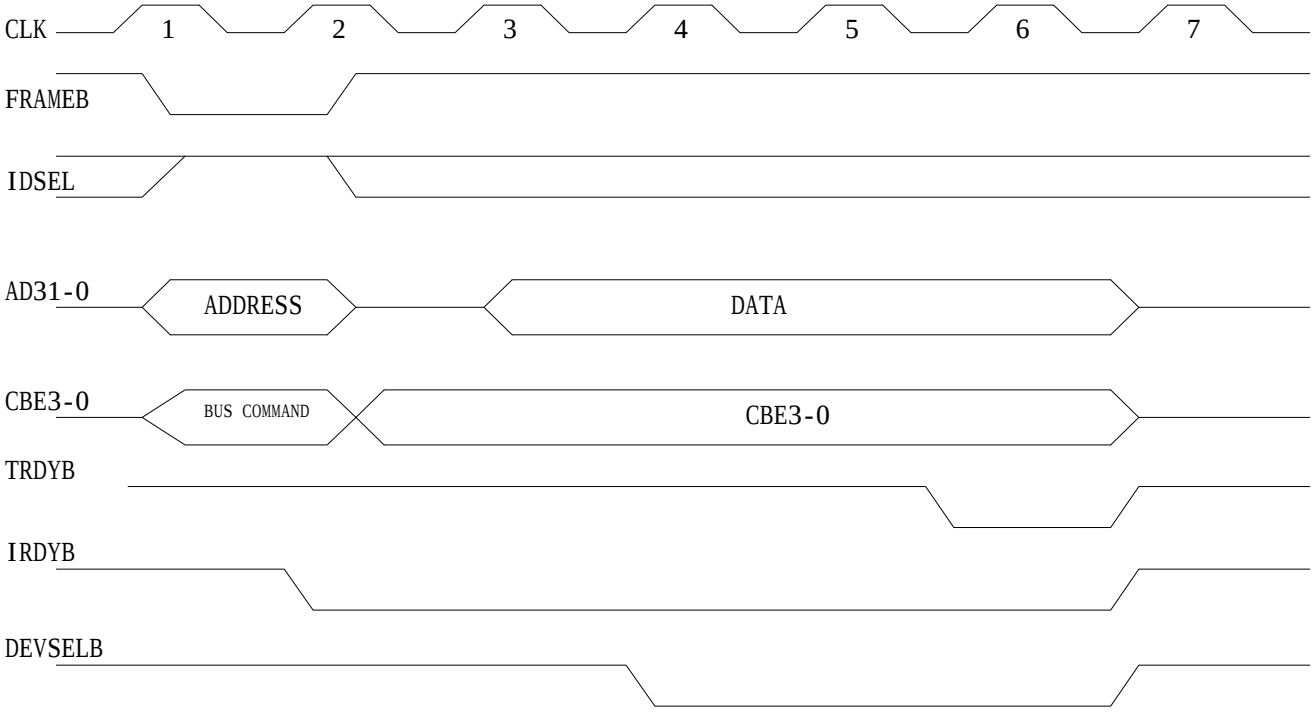
Target Read



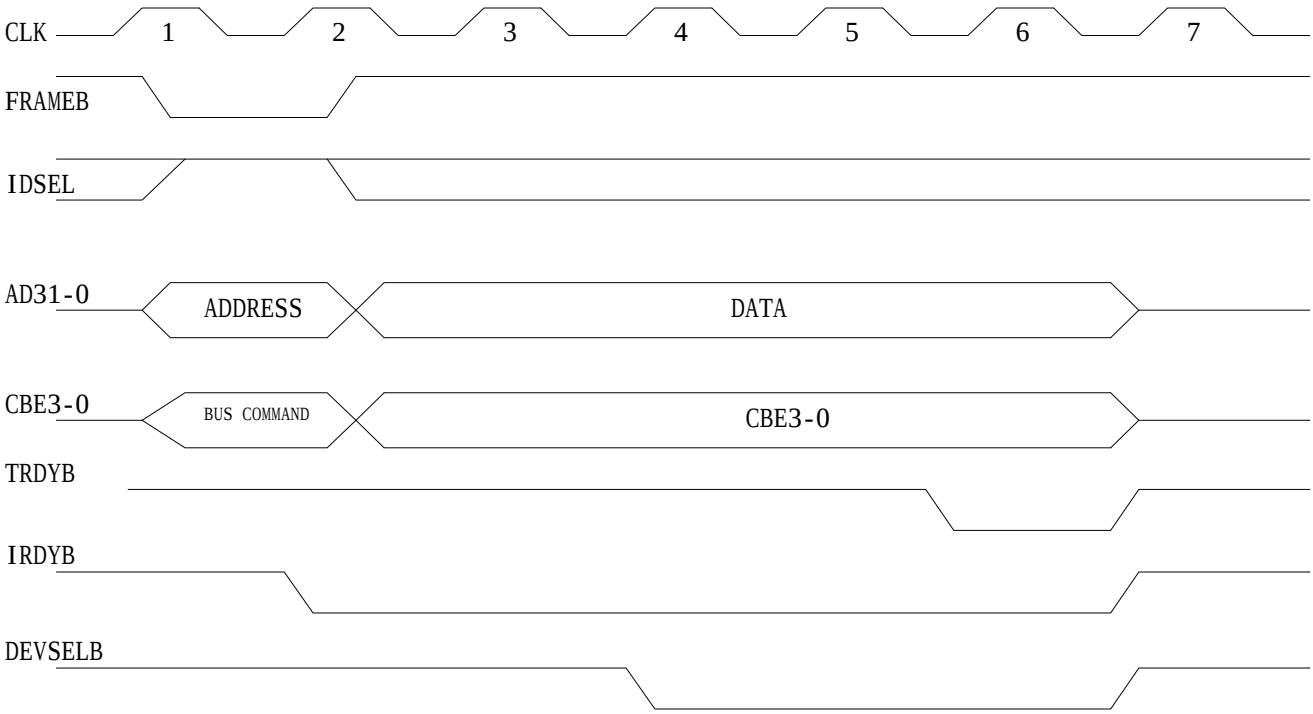
Target Write



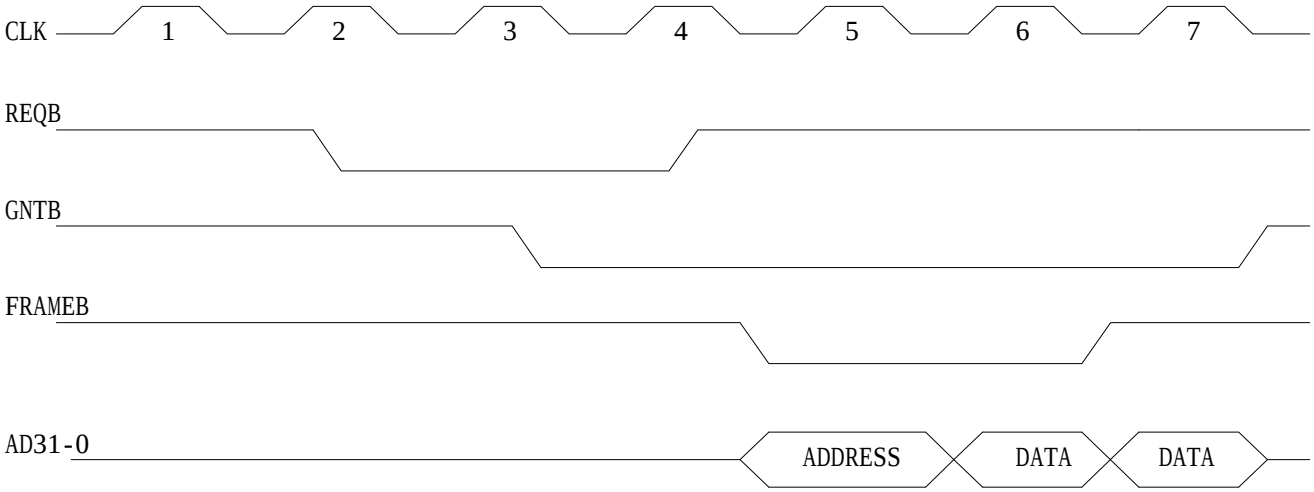
Configuration Read



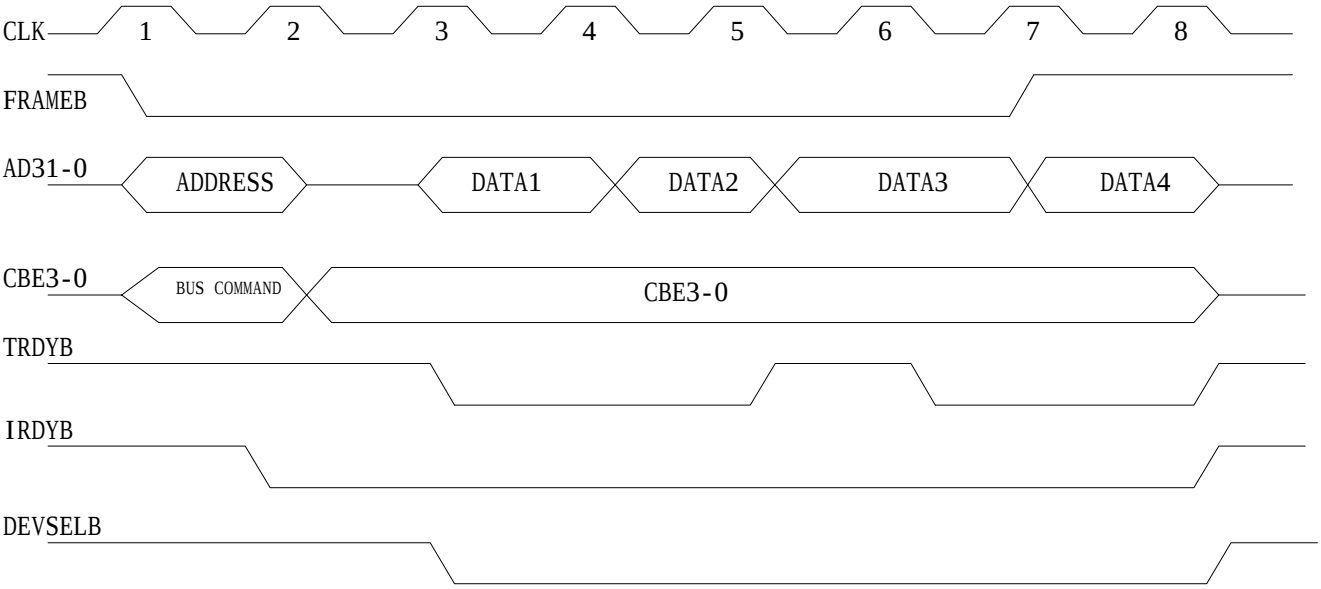
Configuration Write



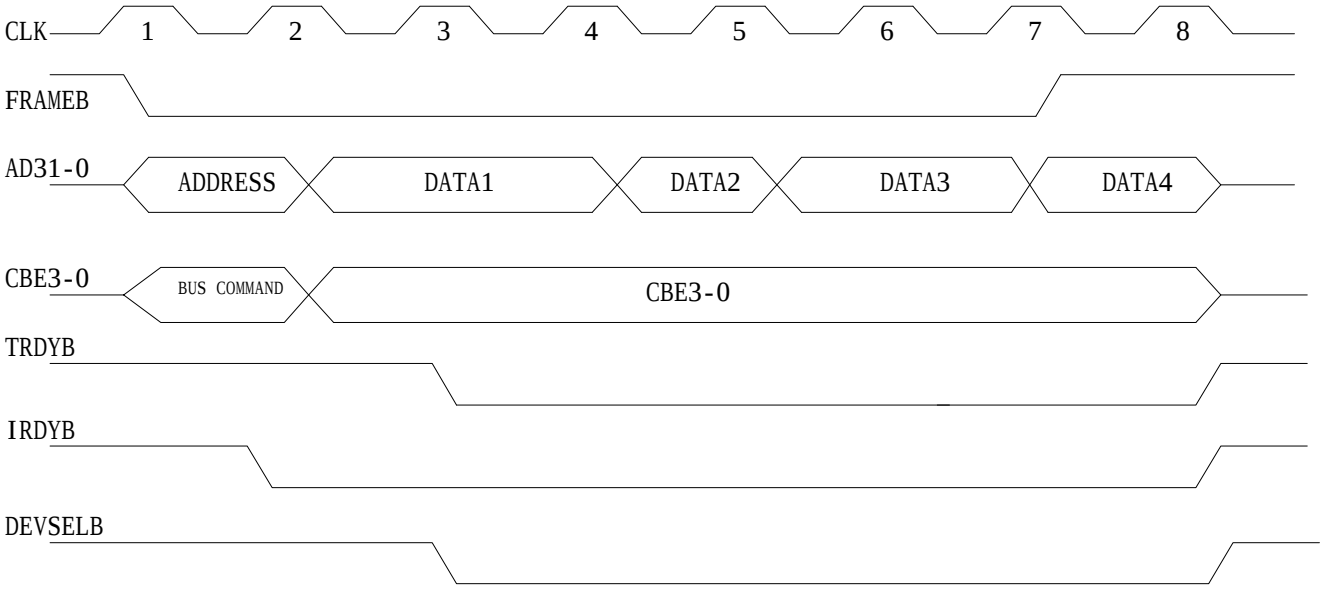
BUS Arbitration



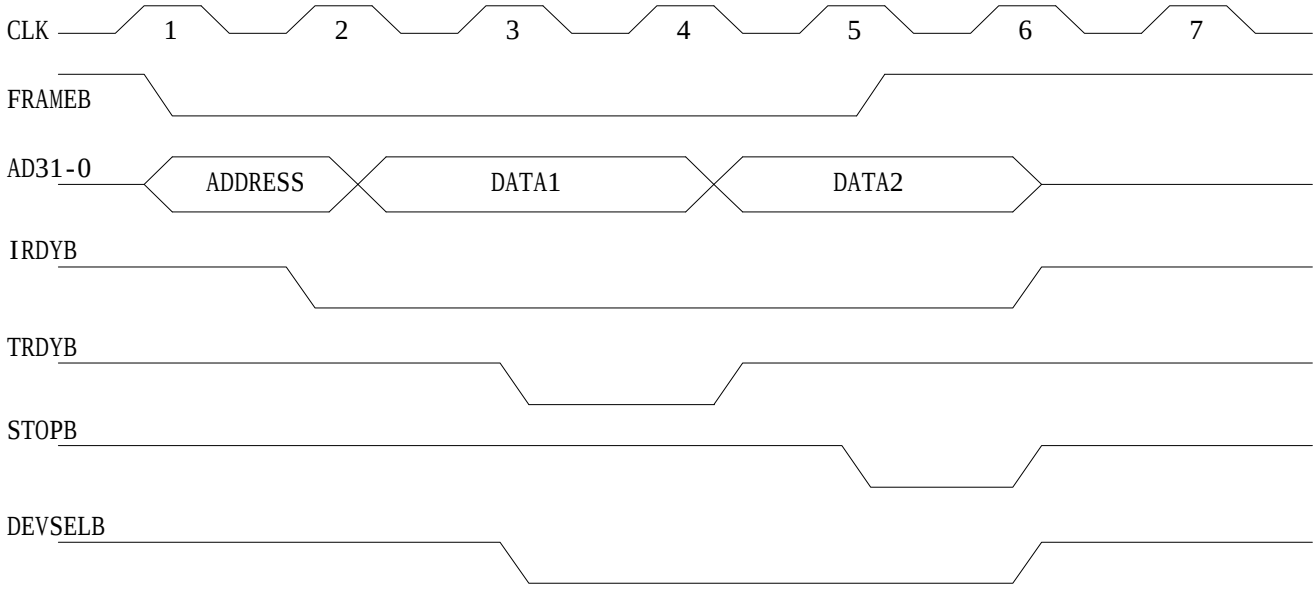
Memory Read



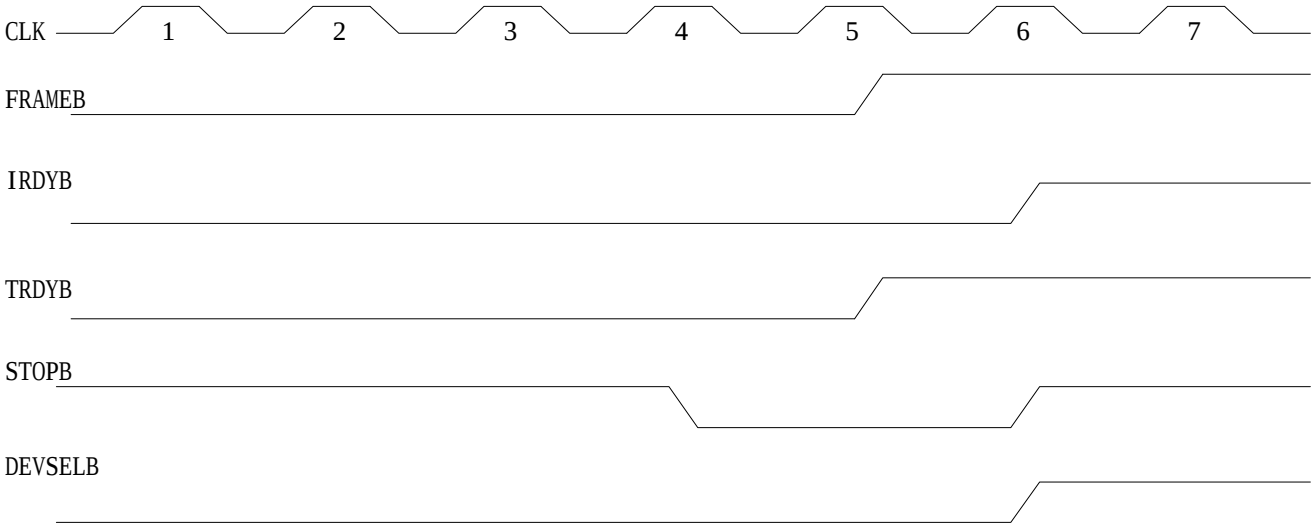
Memory Write



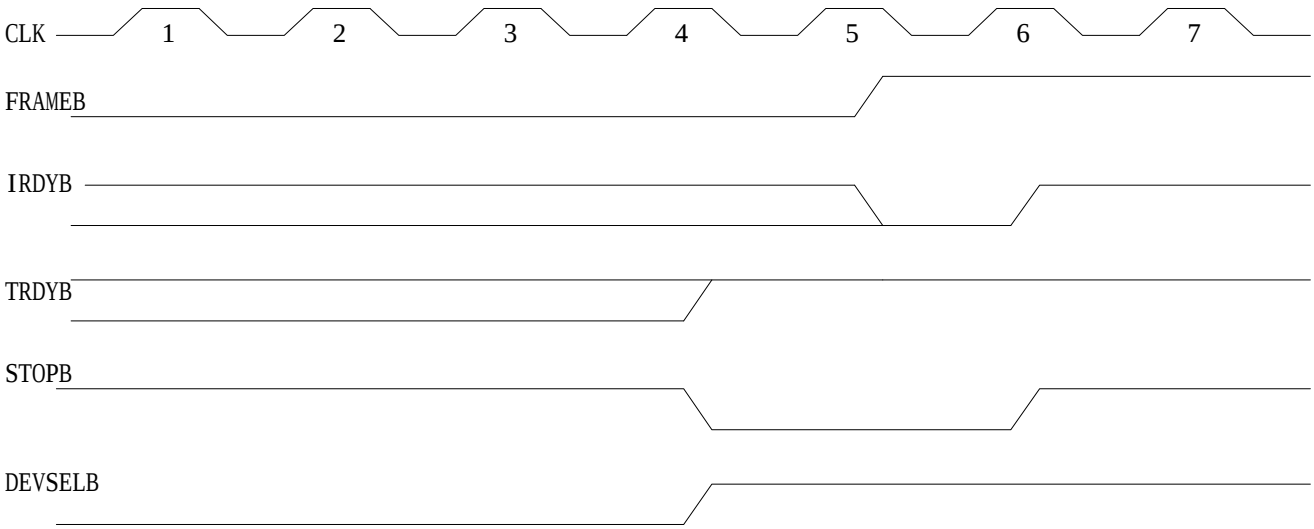
Target Initiated Termination - Retry



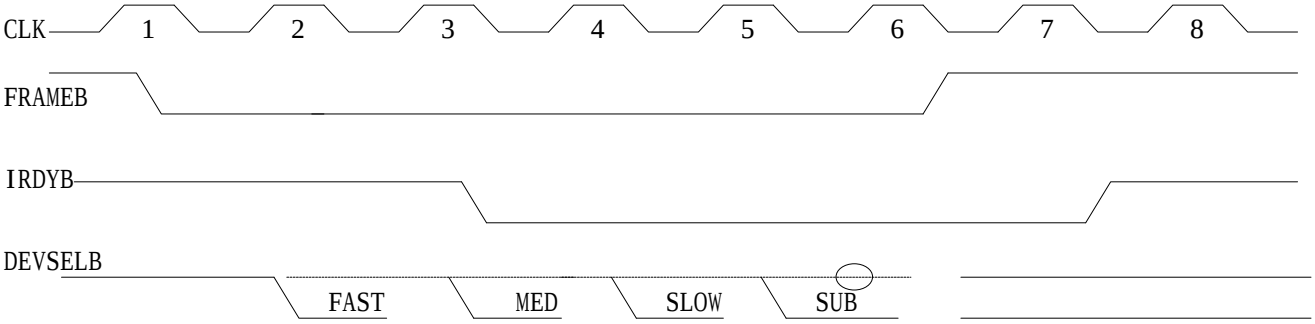
Target Initiated Termination - Disconnect



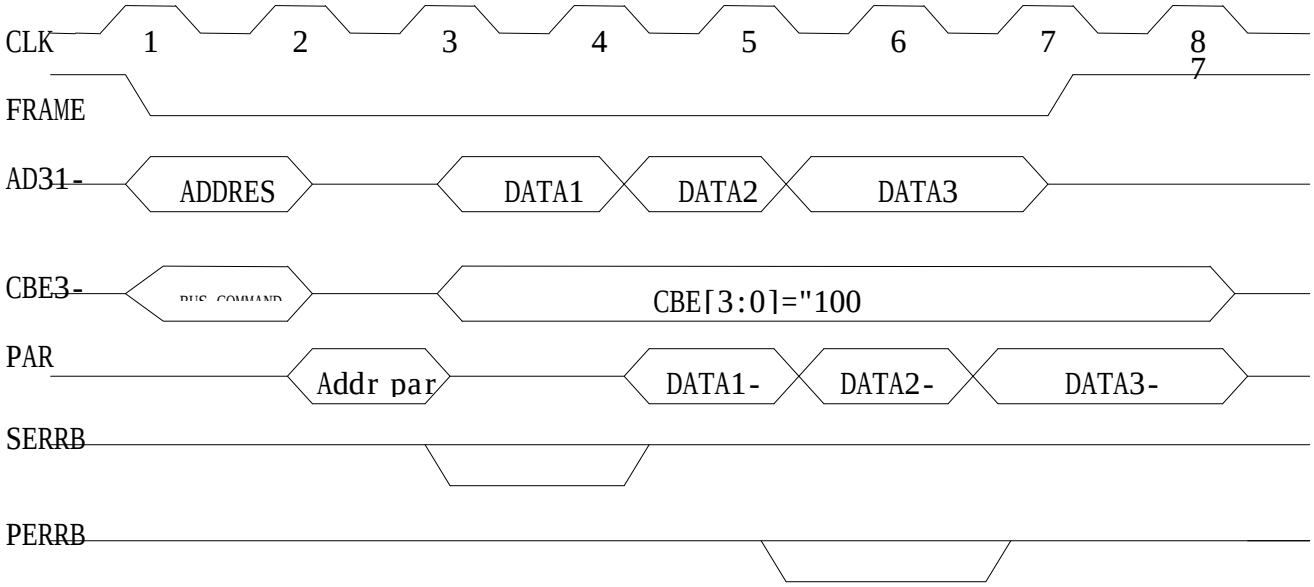
Target Initiated Termination - Abort



Master Initiated Termination - Abort



Parity Operation - one example



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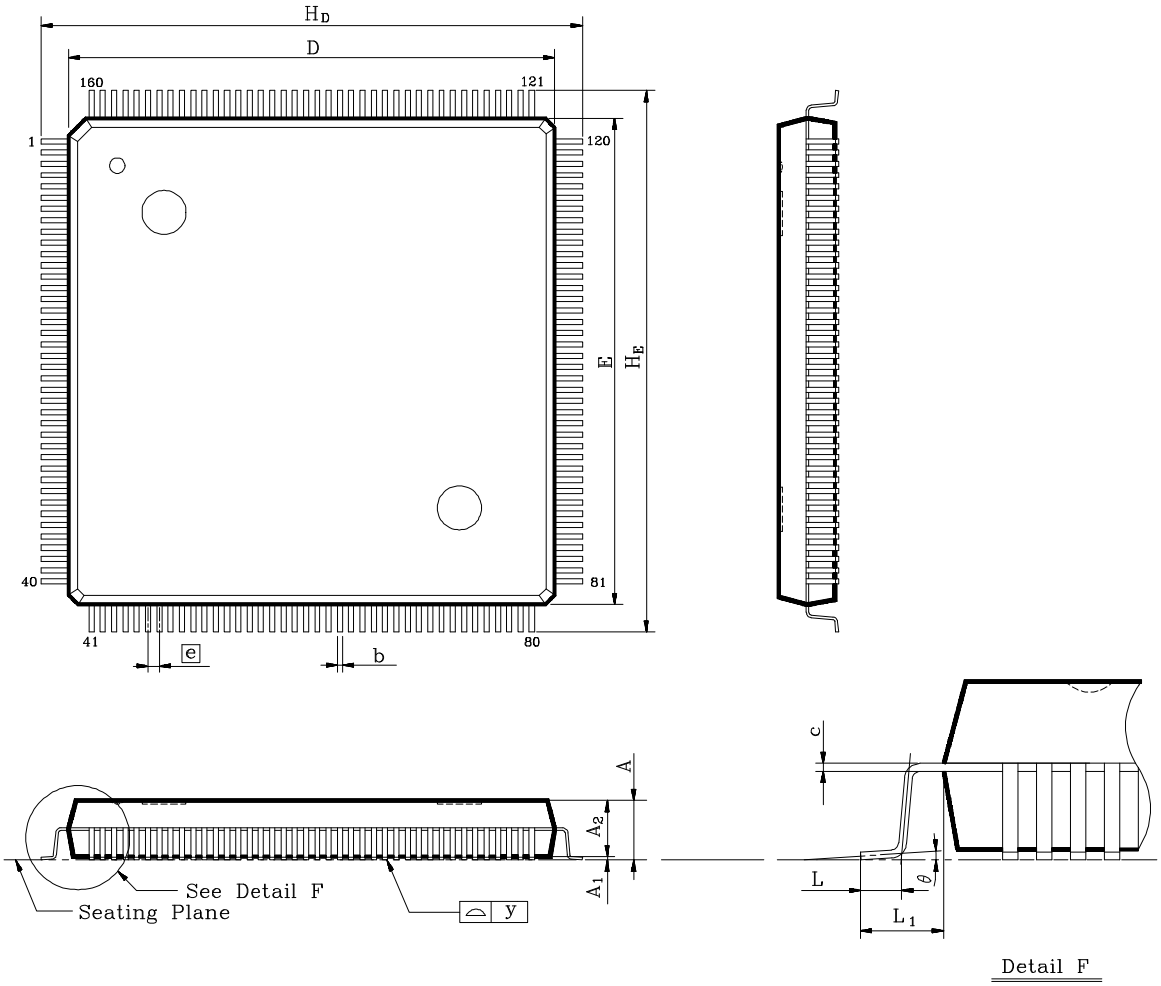

Symbol	Dimension in inch			Dimension in mm		
	Min	Typ	Max	Min	Typ	Max
A	¡ Ð	¡ Ð	0.152	¡ Ð	¡ Ð	3.85
A1	0.004	¡ Ð	¡ Ð	0.10	¡ Ð	¡ Ð
A2	0.119	0.128	0.136	3.02	**3.24**	3.46
b	0.007	0.012	0.017	0.18	**0.30**	0.42
c	0.002	0.006	0.010	0.04	**0.15**	0.26
D	1.093	1.102	1.112	27.75	**28.00**	28.25
E	1.093	1.102	1.112	27.75	**28.00**	28.25
e	0.020	0.026	0.031	0.50	**0.65**	0.80
HD	1.217	1.228	1.240	30.90	**31.20**	31.50
HE	1.217	1.228	1.240	30.90	**31.20**	31.50
L	0.023	0.031	0.039	0.60	**0.80**	1.00
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	-	-	0.004	-	-	0.10
q	0°	-	12°	0°	-	12°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : 160L QFP (28x28 mm**2) FOOTPRINT 3.2 mm PACKAGE OUTLINE DRAWING			
LEAD FRAME MATERIAL:			
APPROVE		DWGNO	Q160
		REVNO.	
		SCALE	
CHECK	Ricardo Chen	DATE	
		SHTNO.	
REALTEK SEMICONDUCTOR CORP.			