Tiny Package, High Efficiency, Step-Up DC/DC Converter

General Description

The RT9275 is a compact, high efficiency, and low voltage step-up DC/DC converter with an Adaptive Current Mode PWM control loop, includes an error amplifier, ramp generator, comparator, switch pass element and driver in which providing a stable and high efficient operation over a wide range of load currents.

The low start-up input voltage below 1V makes RT9275 suitable for 1 to 4 battery cells applications. Both internal 2.5A switch and driver for driving external power devices (NMOS or NPN) are provided. It is incorporating with soft-start function, Under Voltage protection function.

RT9275 is available in SOT-23-6 package.

Ordering Information

RT9275□□

- Package Type
  - E : SOT-23-6
- Operating Temperature Range
  - P : Pb Free with Commercial Standard
  - G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

Features

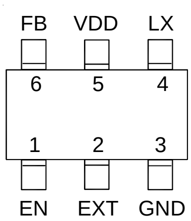
- **1V Low Start-up Input Voltage at 1mA Load**
- **Zero Shutdown Mode Supply Current**
- **90% Efficiency**
- **400kHz Switching Frequency**
- **Providing Flexibility for Using Internal and External Power Switches**
- **Build Soft-Start function internally**
- **Under-Voltage Protection**
- **Small SOT-23-6 Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- PDA
- DSC
- LCD Panel
- RF-Tags
- MP3
- Portable Instrument
- Wireless Equipment

Pin Configurations

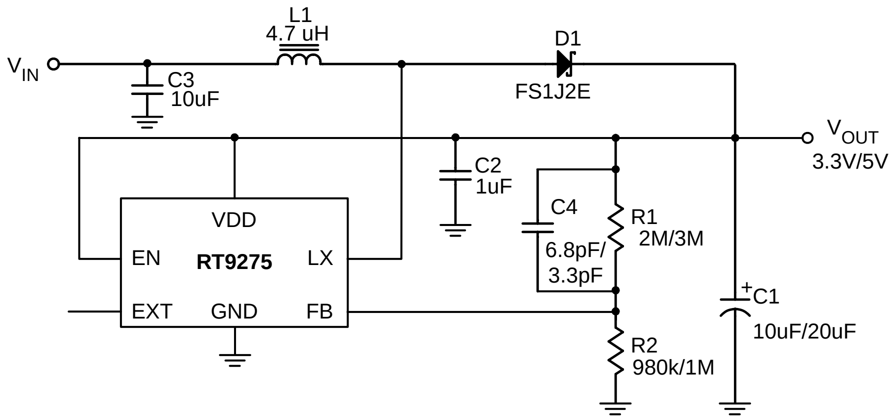
(TOP VIEW)



SOT-23-6

Note : There is no pin1 indicator on top mark for SOT-23-6 type, and pin 1 will be lower left pin when reading top mark from left to right.

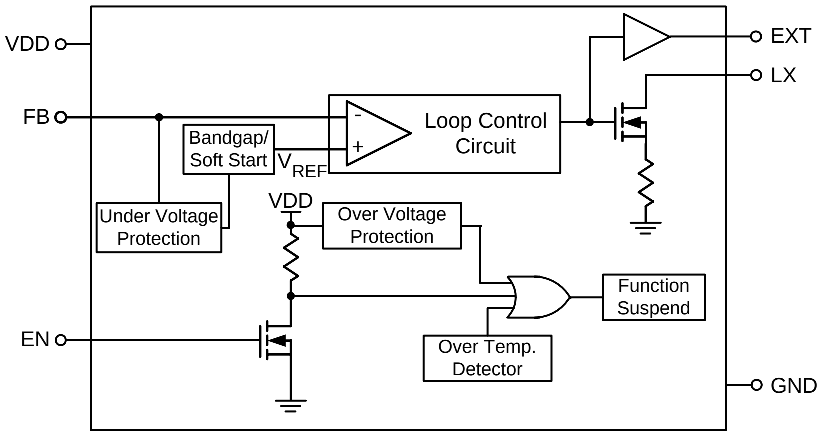
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Chip Enable (Active High)
2	EXT	Output pin for driving external NMOS
3	GND	Ground
4	LX	Pin for switching
5	VDD	Input positive power pin of RT9275
6	FB	Feedback input pin. Internal reference voltage for the error amplifier is 1.25V.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage ---------- 7V
- LX Pin Switch Voltage ---------- –0.3V to 7V
- Other I/O Pin Voltages ---------- –0.3V to 7V
- LX Pin Switch Current ---------- 2.5A
- EXT Pin Driver Current ---------- 200mA
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.4W
- Package Thermal Resistance (Note 3)
  SOT-23-6, θ_{JA} ---------- 250°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to +150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Electrical Characteristics

(V_{IN} = 1.5V, V_{OUT} = V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Start-UP Voltage	V_{ST}	I_L = 1mA	--	0.9	1.0	V
Operating VDD Range	V_{DD}	V_{DD} pin voltage	2	--	6	V
No Load Current I (V_{IN}) (Note 4)	$I_{NO\ LOAD}$	V_{IN} = 1.5V, V_{OUT} = 3.3V	--	160	200	μA
Continuous Switching Current	I_{SWITCH}	V_{IN} = EN = 3.3V, V_{FB} = GND	0.2	0.3	0.5	mA
Switch-off Current I (V_{DD})	$I_{SWITCH\ OFF}$	V_{IN} = 6V	--	50	75	μA
Shutdown Current I (V_{IN})	I_{OFF}	EN = 0V, V_{IN} = 4.5V	--	0.01	1	μA
Feedback Reference Voltage	V_{REF}	Close Loop, V_{DD} = 3.3V	1.225	1.25	1.275	V
Output Voltage Temperature Coefficient (refer to V_{FB})	T_S	T_A = –40°C to 85°C	--	50	--	ppm/°C
Switching Frequency	F_S	V_{DD} = 3.3V	300	400	500	kHz
Frequency Temperature Coefficient	Δf	T_A = –40°C to 85°C		0.3		%/°C
Maximum Duty	D_{MAX}	V_{DD} = 3.3V	85	90	--	%
LX ON Resistance		V_{DD} = 3.3V	--	0.3	1.1	Ω
Current Limit Setting (Note 5)	I_{LIM}	V_{DD} = 3.3V	1.5	2.0	2.5	A
EXT ON Resistance to V_{DD}		V_{DD} = 3.3V	--	5	8.5	Ω
EXT ON Resistance to GND		V_{DD} = 3.3V	--	5	8.5	Ω
Line Regulation (refer to V_{FB})	ΔV_{LINE}	V_{DD} = 3.5 ~ 6V, I_L = 1mA	--	1.5	10	mV/V
Load Regulation (Note 6)	ΔV_{LOAD}	V_{IN} = 2.5V, I_L = 1 ~ 100mA	--	0.25	--	mV/mA
V_{DD} Over Voltage Protection			6.3	6.8	7.3	V
EN Pin Trip Level		V_{DD} = 3.3V	0.4	0.8	1.2	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Soft Start time	T_{SS}		3.0	6.0	12	ms
Under Voltage Protection – Threshold Voltage	V_{TH-UVP}		0.75	0.85	0.95	V
Thermal Shutdown	T_{SD}		--	165	--	°C
Thermal Shutdown Hysterises	ΔT_{SD}		--	10	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

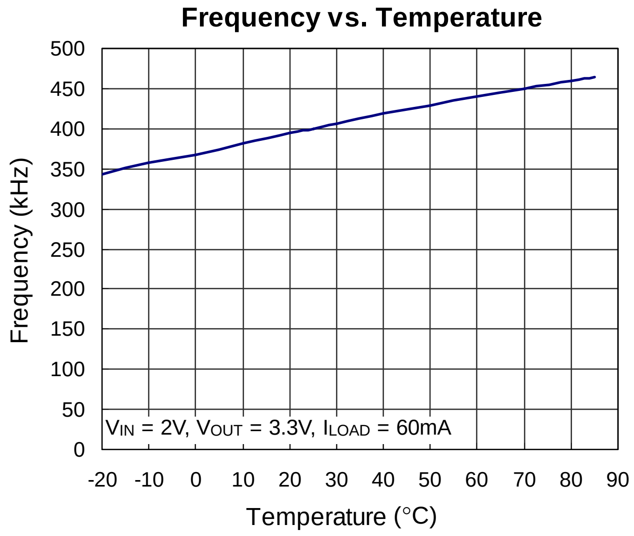
Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

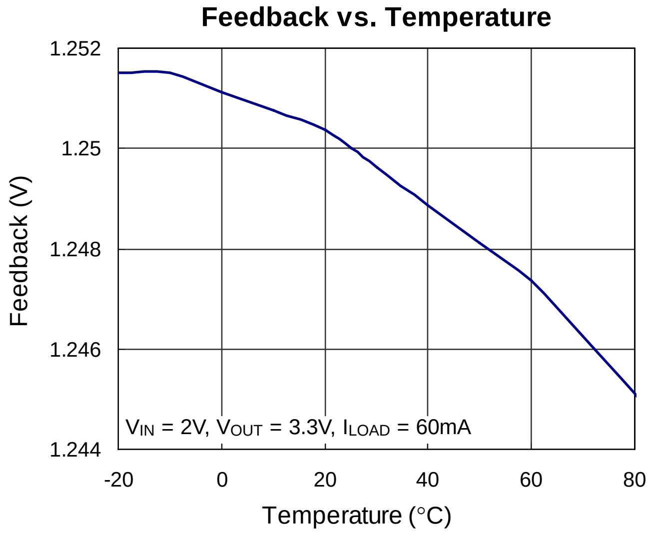
Note 4. No Load Current is highly dependent on practical system design and component selection that cannot be covered by production testing. Typical No Load Current is verified by typical application circuit with recommended components. No Load Current performance is guaranteed by Switch Off Current and Continuous Switching Current.

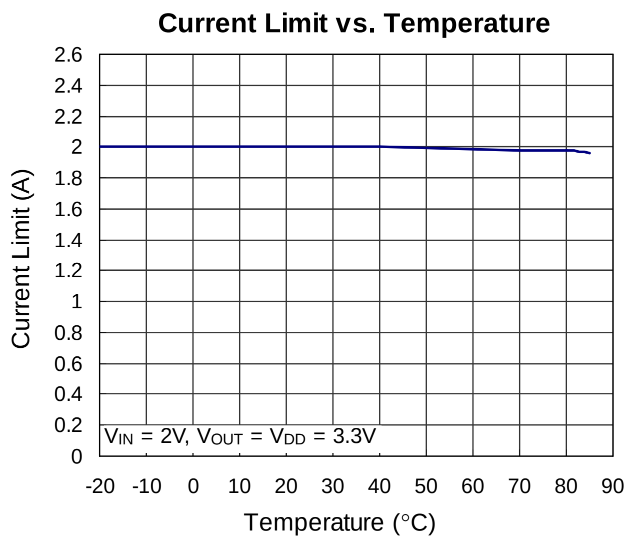
Note 5. Current Limit is guaranteed by design at T_A = 25°C.

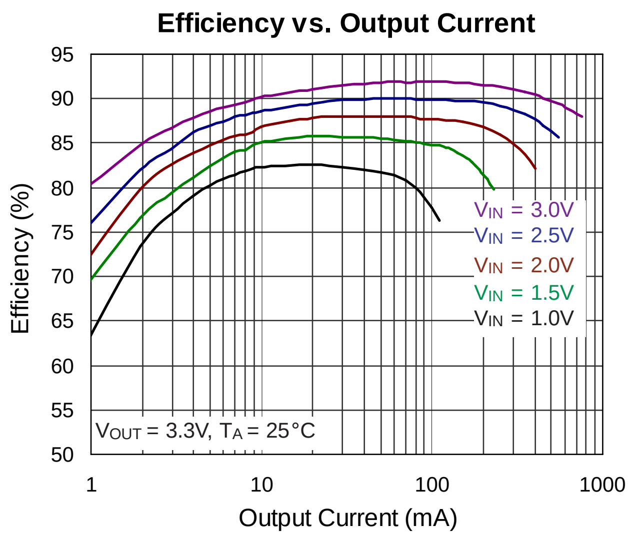
Note 6. Load Regulation is not tested at production due to practical instrument limitation. Load Regulation performance is dominantly dependent on DC loop gain and LX ON Resistance that are guaranteed by "Line Regulation" and "LX ON Resistance" tests in production.

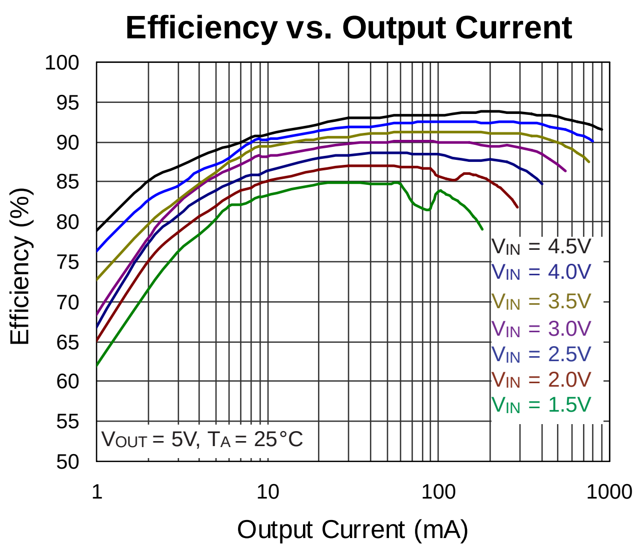
Typical Operating Characteristics

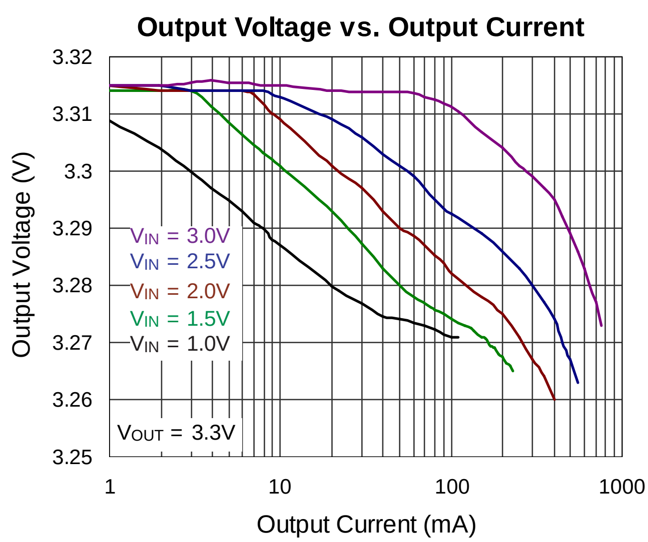




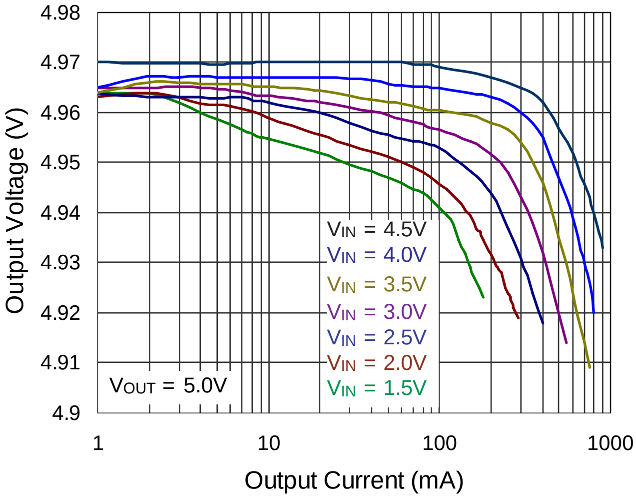




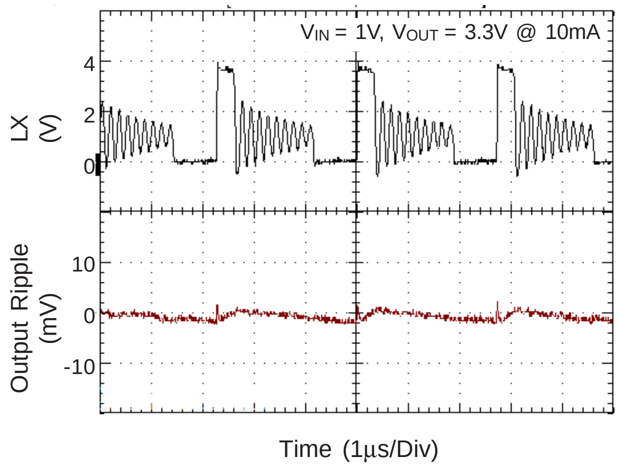




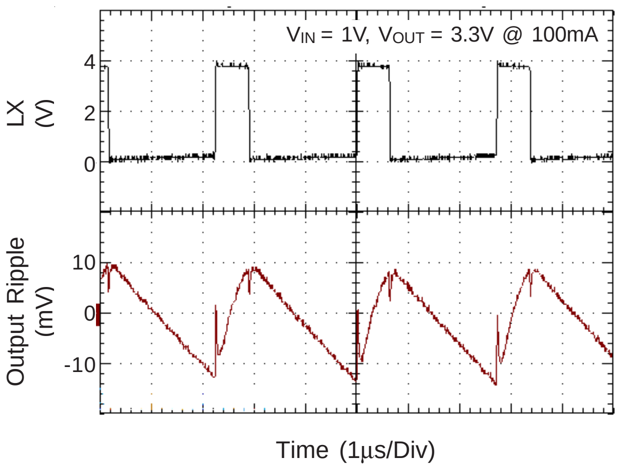
Output Voltage vs. Output Current



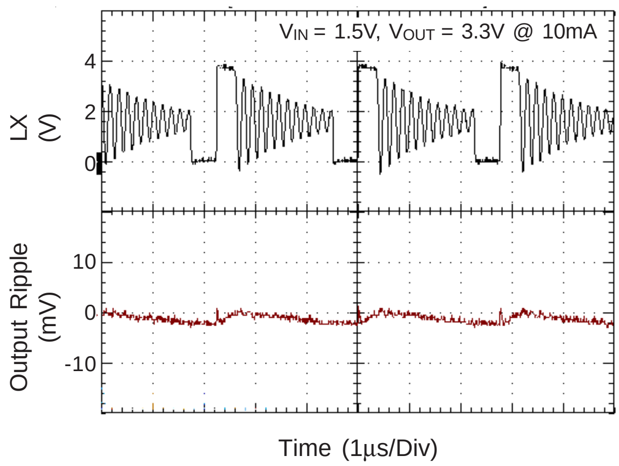
LX & Output Ripple



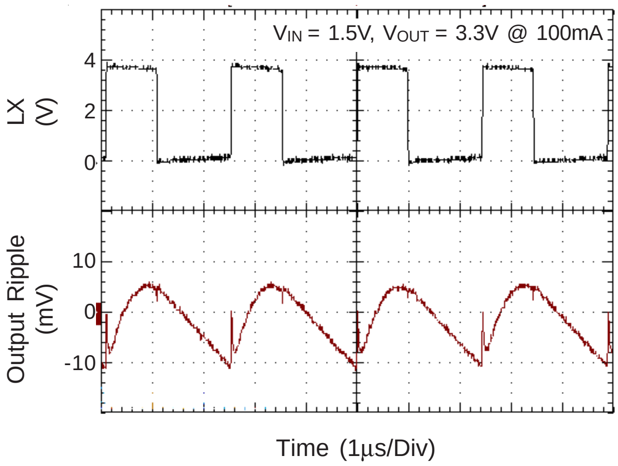
LX & Output Ripple



LX & Output Ripple



LX & Output Ripple



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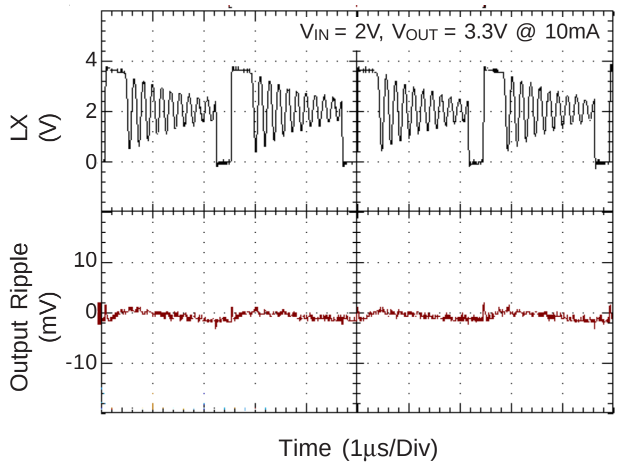
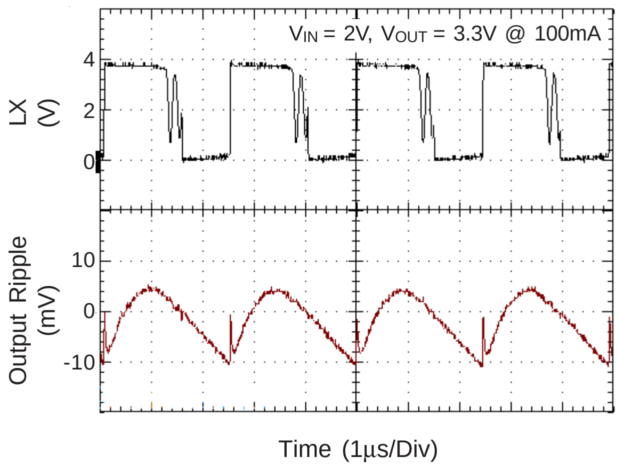


LX & Output Ripple



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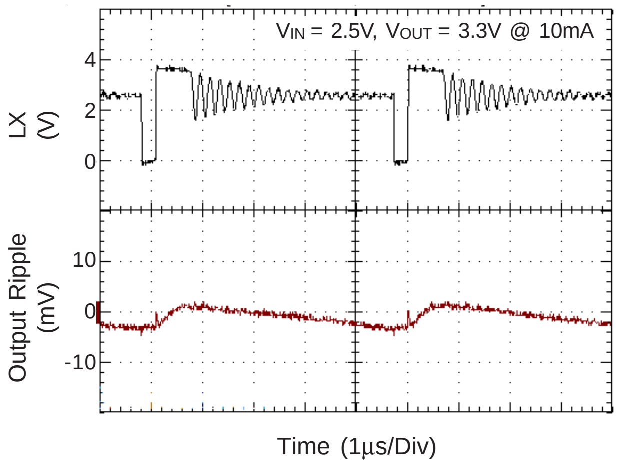
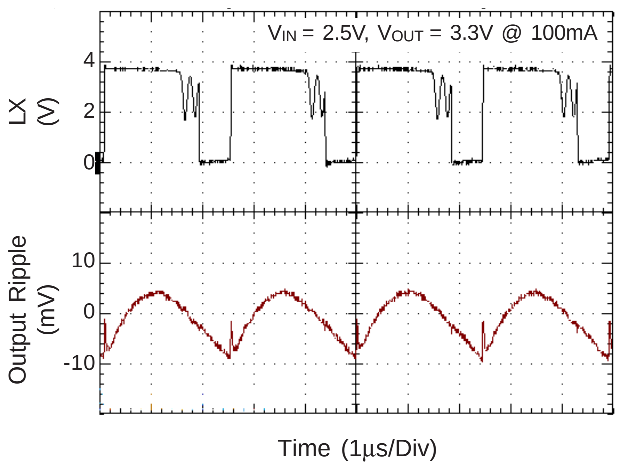
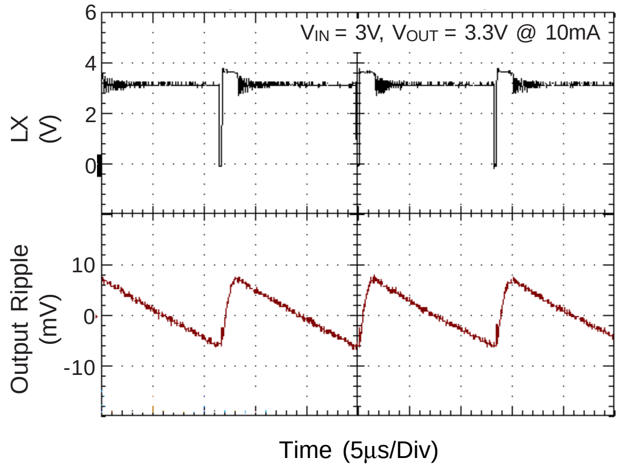


LX & Output Ripple



LX & Output Ripple



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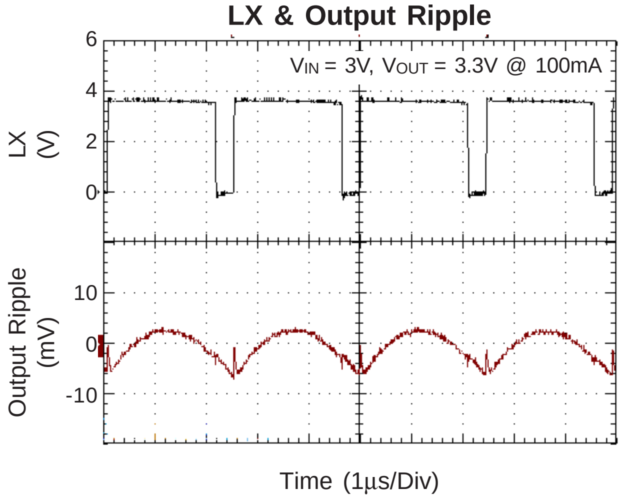

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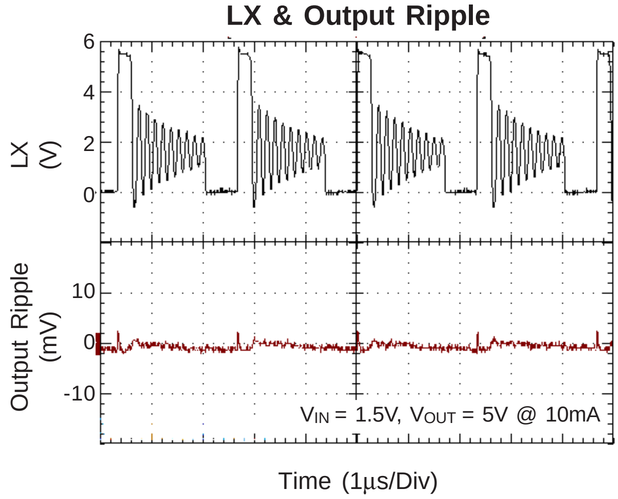

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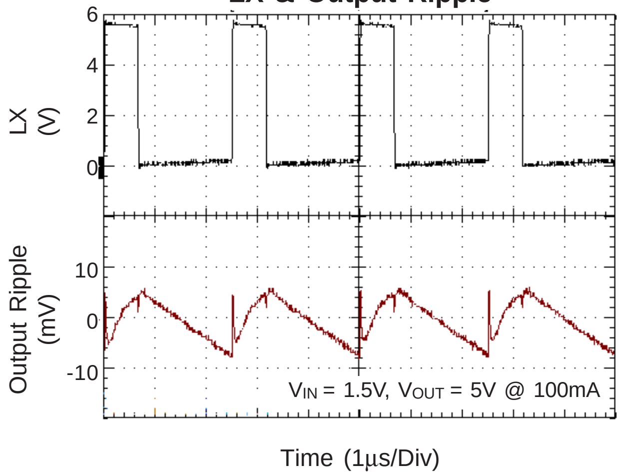

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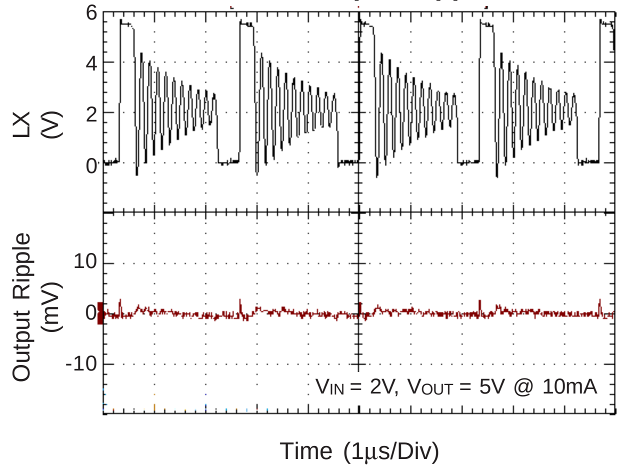

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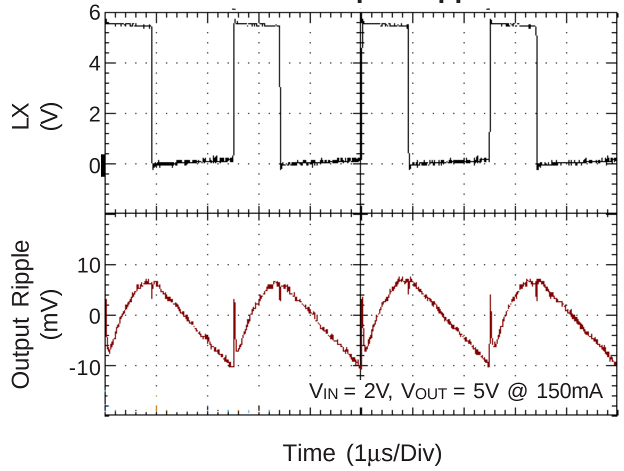
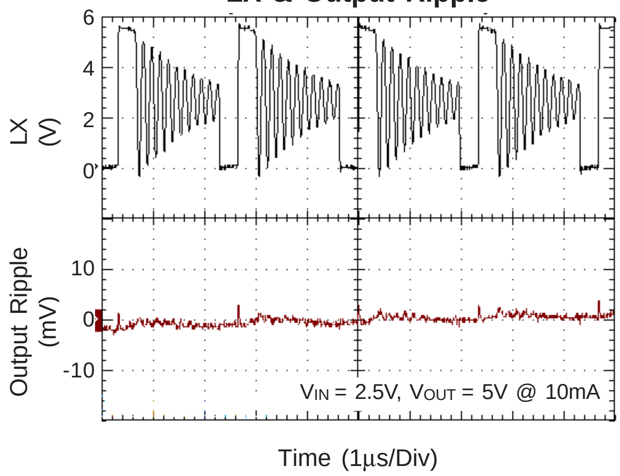
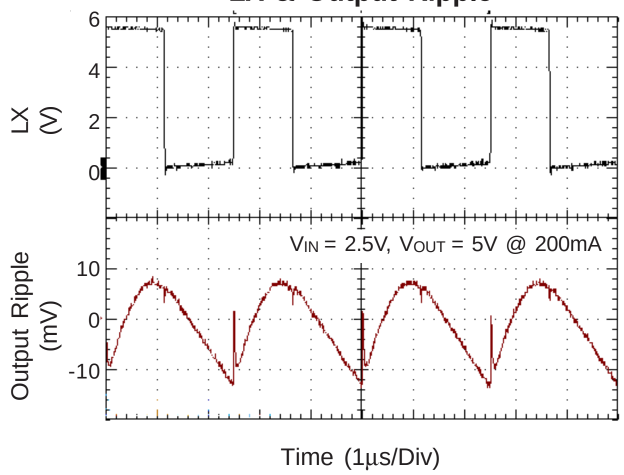


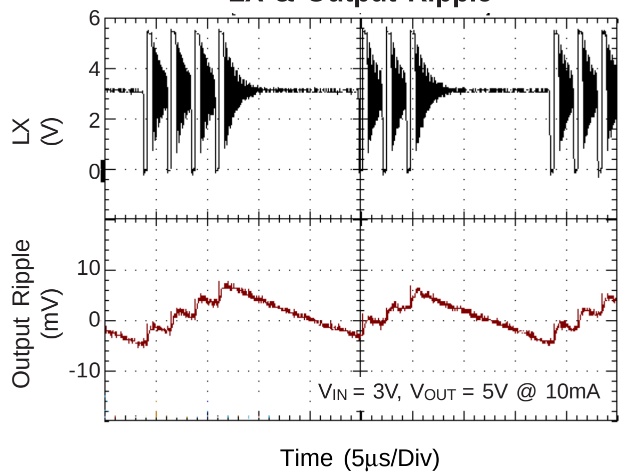
LX & Output Ripple

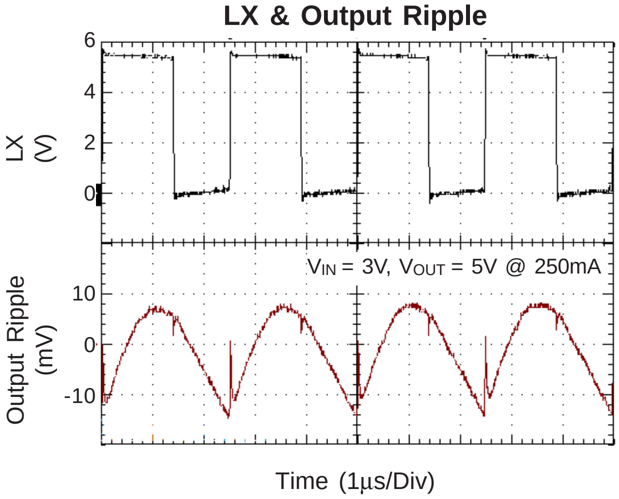


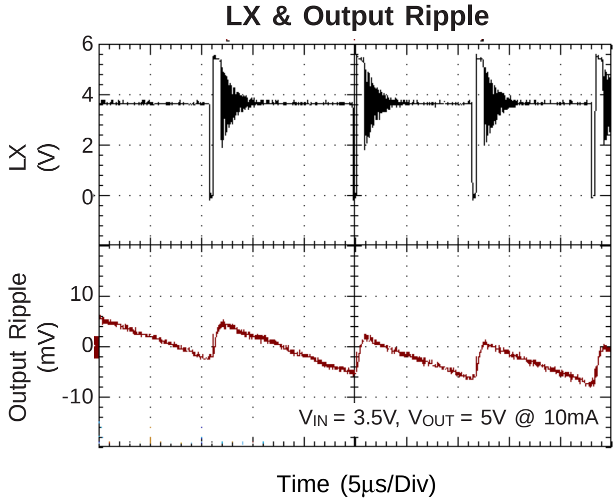
LX & Output Ripple

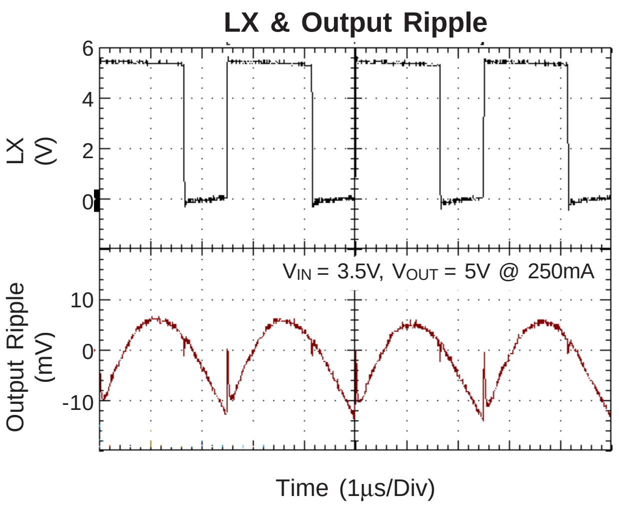


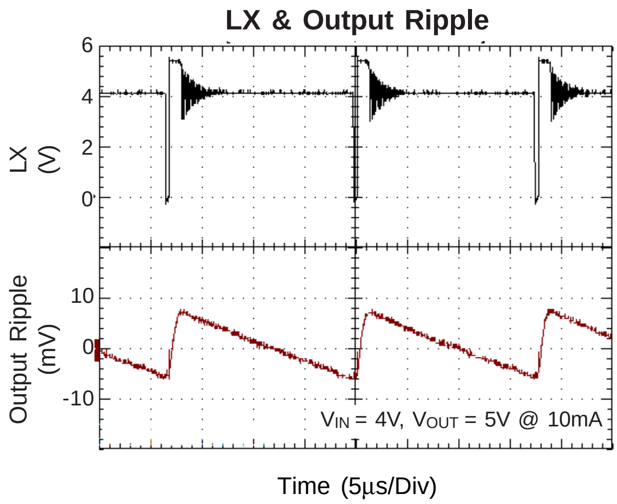
LX & Output Ripple

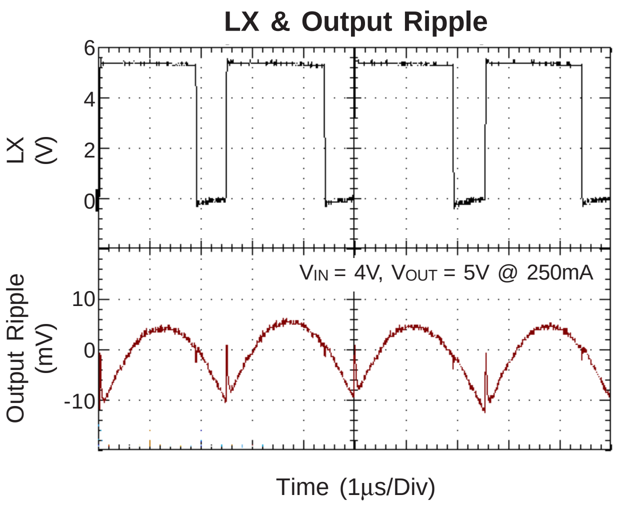


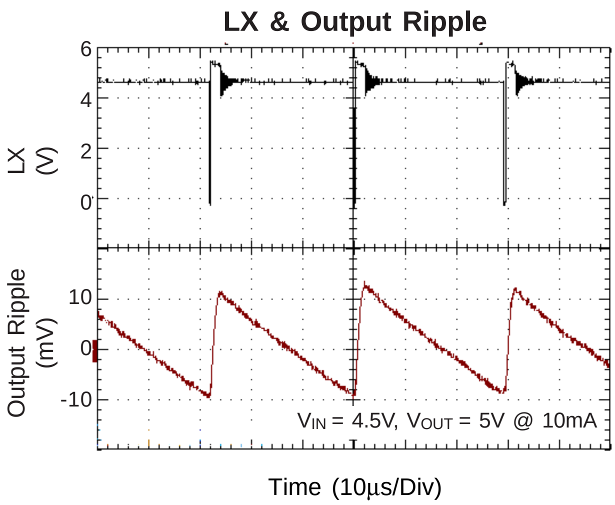

LX & Output Ripple
LX (V)
Output Ripple (mV)
VIN = 3V, VOUT = 5V @ 250mA
Time (1μs/Div)

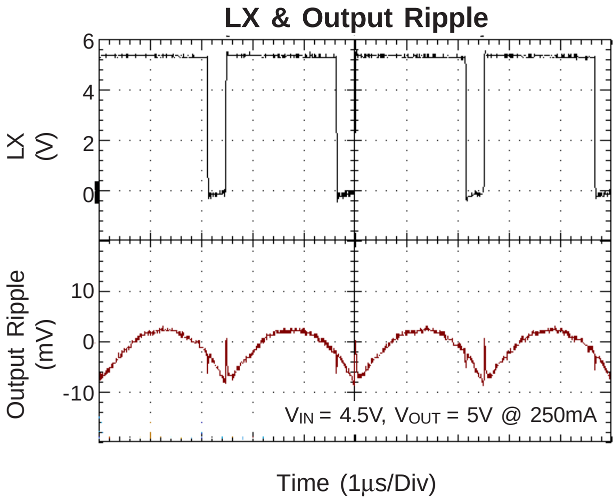

LX & Output Ripple
LX (V)
Output Ripple (mV)
VIN = 3.5V, VOUT = 5V @ 10mA
Time (5μs/Div)

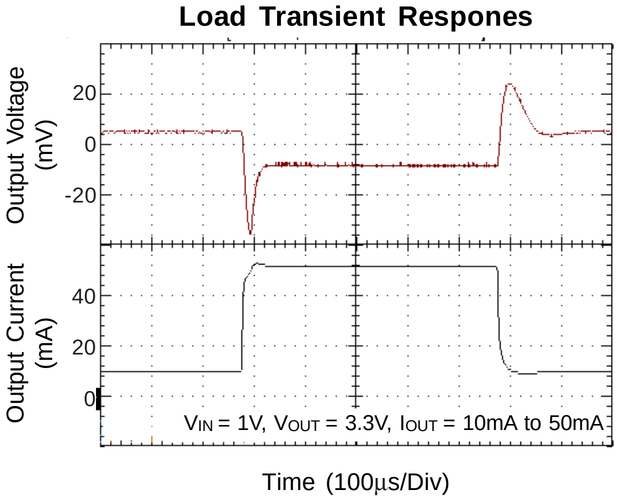

LX & Output Ripple
LX (V)
Output Ripple (mV)
VIN = 3.5V, VOUT = 5V @ 250mA
Time (1μs/Div)

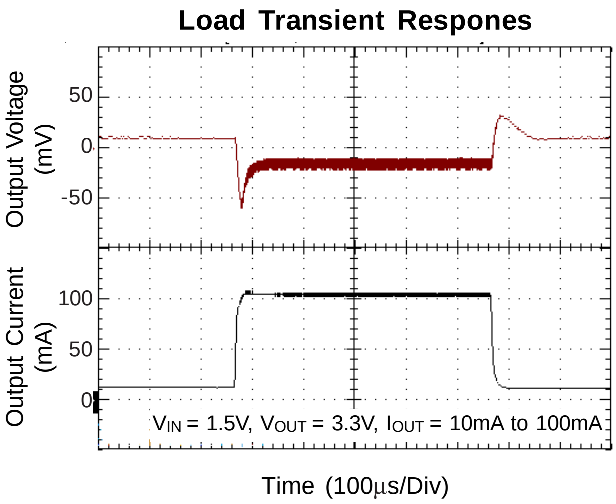

LX & Output Ripple
LX (V)
Output Ripple (mV)
VIN = 4V, VOUT = 5V @ 10mA
Time (5μs/Div)

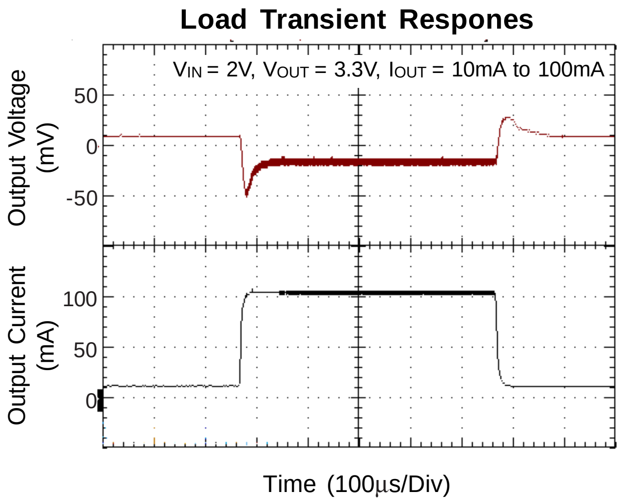

LX & Output Ripple
LX (V)
Output Ripple (mV)
VIN = 4V, VOUT = 5V @ 250mA
Time (1μs/Div)

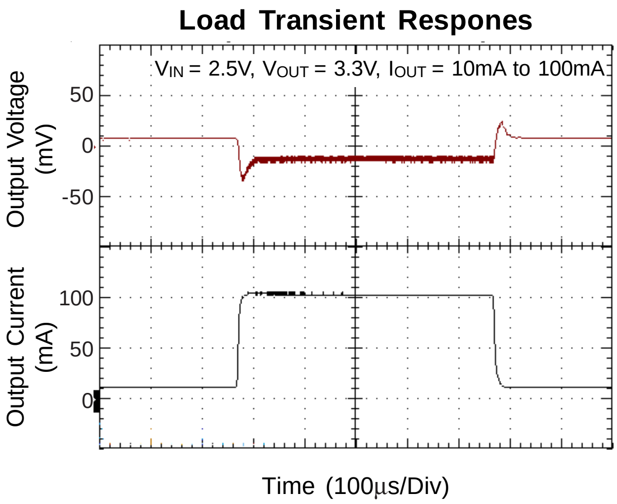

LX & Output Ripple
LX (V)
Output Ripple (mV)
VIN = 4.5V, VOUT = 5V @ 10mA
Time (10μs/Div)

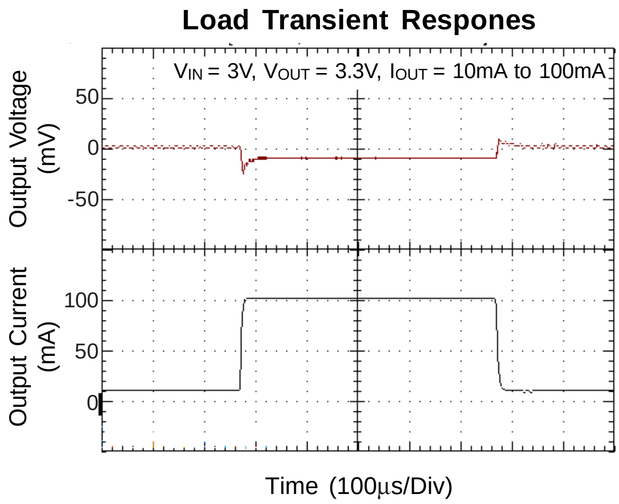

LX & Output Ripple
LX
(V)
6
4
2
0
Output Ripple
(mV)
10
0
-10
VIN = 4.5V, VOUT = 5V @ 250mA
Time (1μs/Div)


Load Transient Respones
Output Voltage
(mV)
20
0
-20
Output Current
(mA)
40
20
0
VIN = 1V, VOUT = 3.3V, IOUT = 10mA to 50mA
Time (100μs/Div)

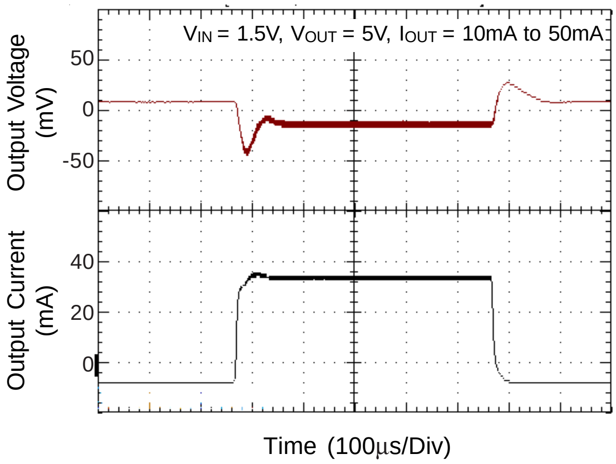

Load Transient Respones
Output Voltage
(mV)
50
0
-50
Output Current
(mA)
100
50
0
VIN = 1.5V, VOUT = 3.3V, IOUT = 10mA to 100mA
Time (100μs/Div)


Load Transient Respones
VIN = 2V, VOUT = 3.3V, IOUT = 10mA to 100mA
Output Voltage
(mV)
50
0
-50
Output Current
(mA)
100
50
0
Time (100μs/Div)

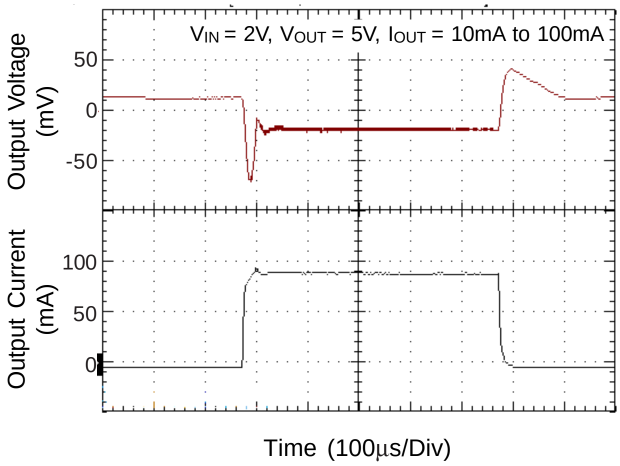

Load Transient Respones
VIN = 2.5V, VOUT = 3.3V, IOUT = 10mA to 100mA
Output Voltage
(mV)
50
0
-50
Output Current
(mA)
100
50
0
Time (100μs/Div)


Load Transient Respones
VIN = 3V, VOUT = 3.3V, IOUT = 10mA to 100mA
Output Voltage
(mV)
50
0
-50
Output Current
(mA)
100
50
0
Time (100μs/Div)

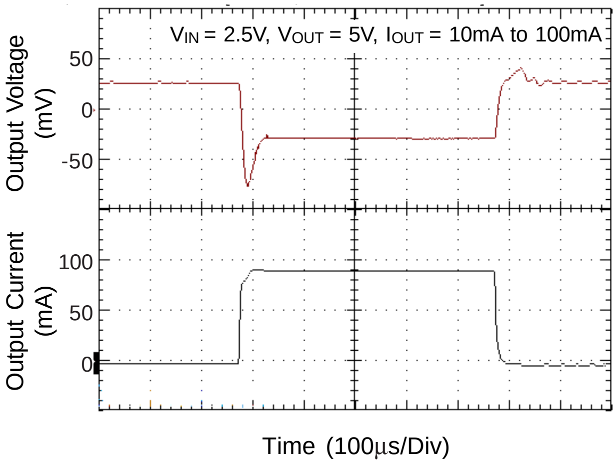
Load Transient Respones



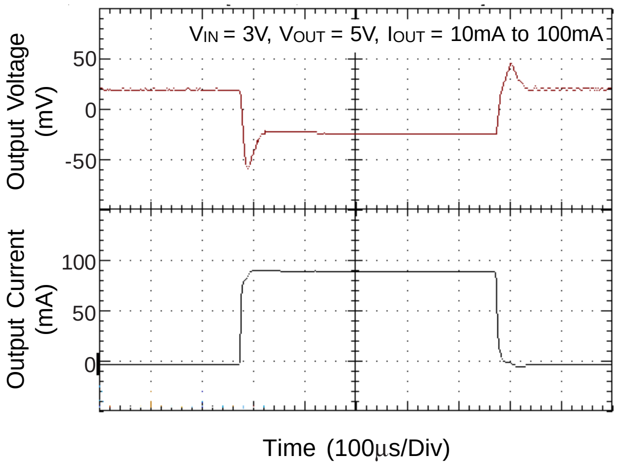
Load Transient Respones



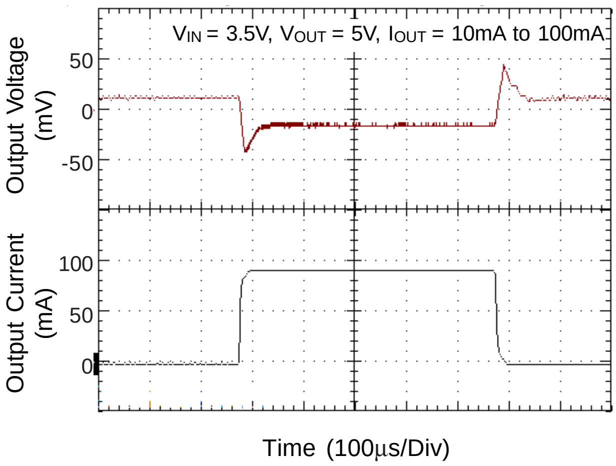
Load Transient Respones



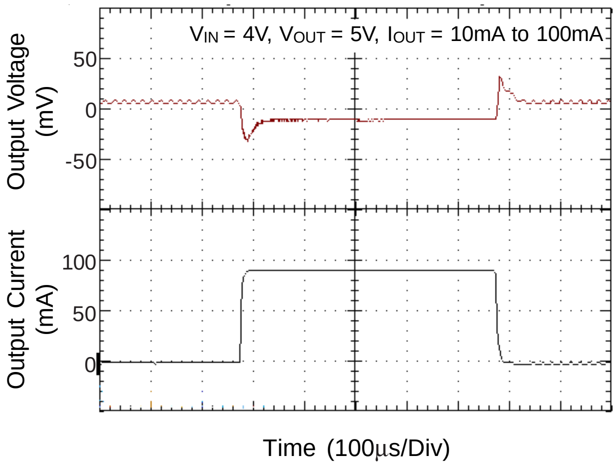
Load Transient Respones

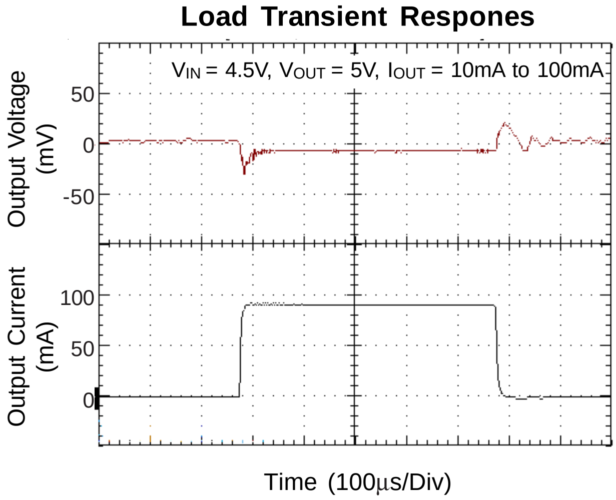


Load Transient Respones



Load Transient Respones




Load Transient Respones
VIN = 4.5V, VOUT = 5V, IOUT = 10mA to 100mA
Output Voltage (mV)
50
0
-50
Output Current (mA)
100
50
0
Time (100μs/Div)

Application Information

Output Voltage Setting

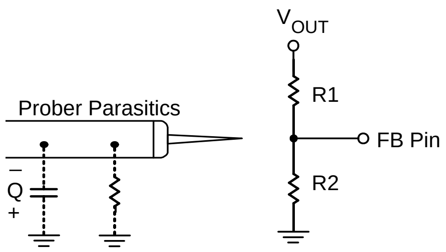
Referring to Typical Application Circuits, the output voltage of the switching regulator (V_{OUT}) can be set with Equation (1).

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times 1.25V \qquad (1)$$

Feedback Loop Design

Referring to Typical Application Circuits. The selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

- Follow Equation (1)
- Higher R reduces the quiescent current (Path current = 1.25V/R2), however resistors beyond 5MΩ are not recommended.
- Lower R gives better noise immunity, and is less sensitive to interference, layout parasitics, FB node leakage, and improper probing to FB pins.



- A proper value of feed forward capacitor parallel with R1 can improve the noise immunity of the feedback loops, especially in an improper layout. An empirical suggestion is

$$\frac{1}{2\pi R1C4} = 10 \text{ to } 20kHz$$

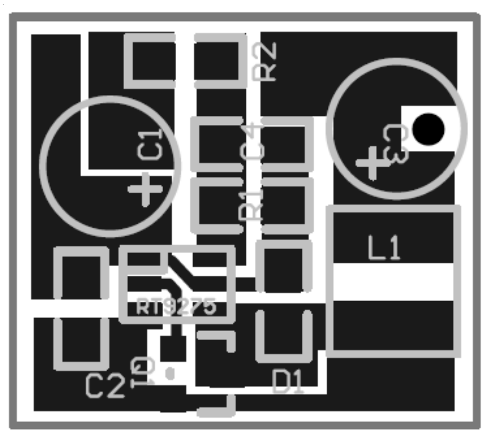
For applications without standby or suspend modes, lower values of R1 and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 and R2 are needed. Such "high impedance feedback loops" are sensitive to any interference, which require careful layout and avoid any interference, e.g. probing to FB pin.

Layout Guide

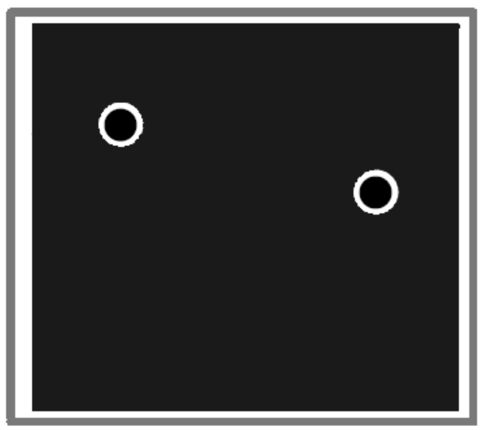
- A full GND plane without gap break.
- V_{DD} to GND noise bypass – Short and wide connection for the 1μF MLCC capacitor between Pin5 and Pin3.
- V_{IN} to GND noise bypass – Add a capacitor close to L1 inductor, when V_{IN} is not an idea voltage source.
- Minimized FB node copper area and keep far away from noise sources.
- Minimized parasitic capacitance connecting to LX and EXT nodes, which may cause additional switching loss.

Board Layout Example (2-Layer Board)

(Refer to Typical Application Circuit for the board)

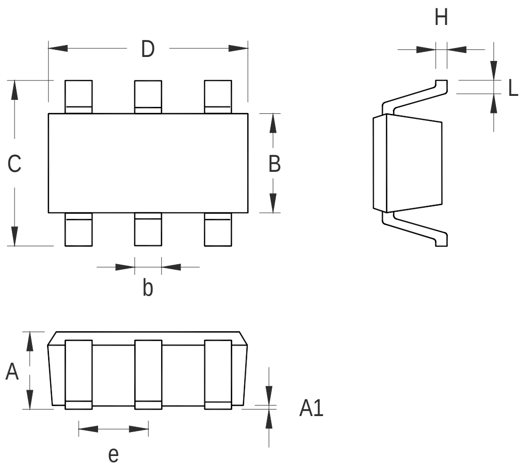


- Top Layer -



- Bottom Layer -

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.009	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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