

1.5A/3A Bus Termination Regulator

General Description

The RT9173/A regulator is designed to convert voltage supplies ranging from 1.8V to 6V into a desired output voltage which adjusted by two external resistors, voltage divider. The regulator is capable of sourcing or sinking up to 1.5A/3A of current while regulating an output voltage to within 2% or less.

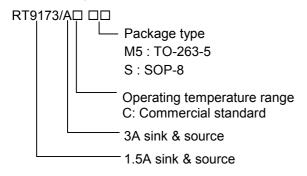
The RT9173/A, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs. The voltage output of the regulator can be used as a termination voltage for DDR SDRAM.

Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of the output fault conditions.

Applications

- Computers
- Disk Drives
- CD-ROM
- · Supply Splitter
- Graph Card

Ordering Information



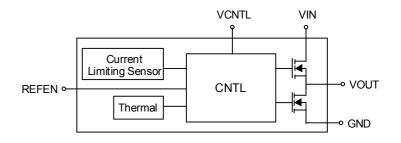
Features

- Support Both DDR 1 (1.25VTT) and DDR 2 (0.9VTT) Requirements
- Power TO-263-5 and SOP-8 Packages
- Capable of Sourcing and Sinking Current 1.5A/3A
- Current-limiting Protection
- Thermal Protection
- Integrated Power MOSFETs
- Generates Termination Voltages for SSTL-2
- High Accuracy Output Voltage at Full-load
- Adjustable VOUT by External Resistors
- Minimum External Components
- Shutdown for Standby or Suspend Mode Operation with High-impedance Output

Pin Configurations

Part Number	Pin Configurations		
RT9173ACM5 (Plastic TO-263-5)	TOP VIEW 1. VIN 2. GND 3. VCNTL (1) 4. REFEN 5. VOUT	ГАВ)	
RT9173CS (Plastic SOP-8)	TOP VIEW VIN 1 3 VCNTL GND 2 7 VCNTL REFEN 3 6 VCNTL VOUT 4 5 VCNTL	-	

Function Block Diagram





Pin Description

Pin Name	Pin Function			
VIN	Power Input			
GND	Ground			
VCNTL	Gate Drive Voltage			
REFEN	Reference Voltage Input and Chip Enable			
VOUT	Output Voltage			

Absolute Maximum Ratings

•	Input Voltage	7V
•	Power Dissipation	Internally Limited
•	ESD Rating	2KV
•	Storage Temperature Range	-65°C to 150°C
•	Lead Temperature (Soldering, 5 sec.)	260°C
•	Package Thermal Resistance	
	TO-263,θ _{JC}	7.7°C/W
	TO-263,θ _{JA}	19.4°C/W
	SOP-8, θ _{JC}	15.7°C/W
	SOP-8, θ_{JA} Note	45°C/W

Note: θ_{JA} is measured with the component mounted on an evaluation PC board in free air that the required area of copper is 300mm^2 or larger.

Electrical Characteristics

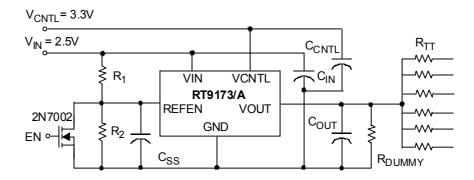
(Limits in standard typeface are for T_A = 25°C, unless otherwise specified:

 V_{IN} = 2.5V, V_{CNTL} = 3.3V, V_{REFEN} = 1.25V, C_{OUT} = 10 μ F (Ceramic))

Parameter		Symbol	Test Conditions	Min	Тур	Max	Units	
Output Offset Voltage		Vos	Fig.1	-20	0	20	mV	
Load Degulation		ا ا	$I_L: 0 \rightarrow 1.5A$, Fig.1	1	0.8	2	%	
Load Regulation		ΔV_{LOAD}	$I_L: 0A \rightarrow -1.5A$		0.8	2		
Input Voltage Range		V_{IN}	Keep V _{CNTL} ≥ V _{IN} on operation	1.8	2.5		V	
(DDR 1)		V _{CNTL}	power on and power off sequences		3.3	6	V	
Current In Shutdown Mode		I _{SHDN}	V_{REFEN} < 0.2V, R_L = 180 Ω , Fig.2		50	90	μΑ	
Short Circuit Protection								
Current limit	RT9173		Fig.3,4	2.1	-		_	
Current limit	RT9173A	I _{LIMIT}	Fig.3,4	3.0	1		Α	
Over Temperature Protection								
Thermal Shutdown Temperature		T _{SD}	$3.3V \le V_{CNTL} \le 5V$		150		°C	
Thermal Shutdown Hysteresis			Guaranteed by design		50		°C	
Shutdown Function								
Shutdown Threshold Trigger			Output = High, Fig.5	0.8	1		\	
			Output = Low, Fig.5		-	0.2	V	



Typical Application Circuit



 $R_1 = R_2 = 100 \text{K}\Omega$, $R_{TT} = 50 \Omega / 33 \Omega / 25 \Omega$

 $C_{OUT,min}$ = $10\mu F$ (Ceramic) + $1000\mu F$ under the worst case testing condition R_{DUMMY} = $1k\Omega$ as for VOUT discharge when VIN is not present but VCNTL is present C_{SS} = $1\mu F$, C_{IN} = $470\mu F$ (Low ESR), C_{CNTL} = $47\mu F$

Test Circuit

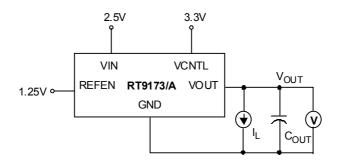


Fig.1 Output Voltage Tolerance, ΔV_{OUT}

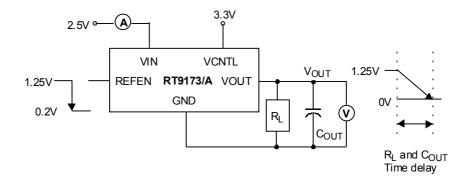


Fig.2 Current in Shutdown Mode, I_{SHCLN}

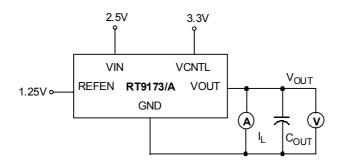


Fig.3 Current Limit for High Side, I_{CLHIGH}

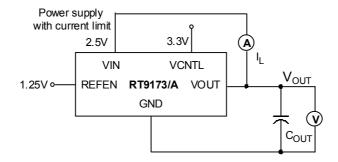


Fig.4 Current Limit for Low Side, ICLLOW

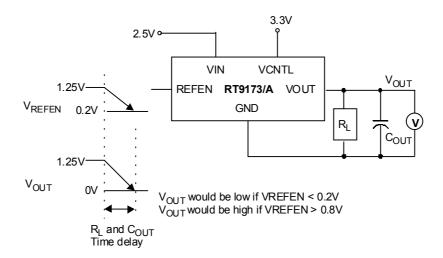
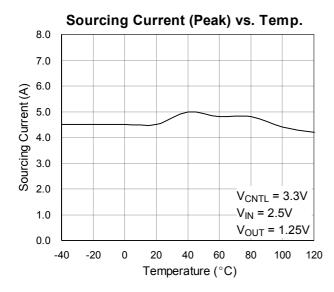
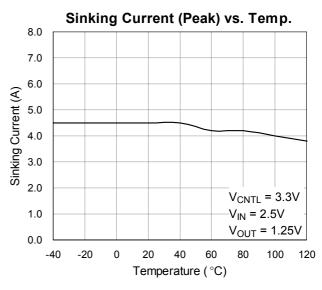


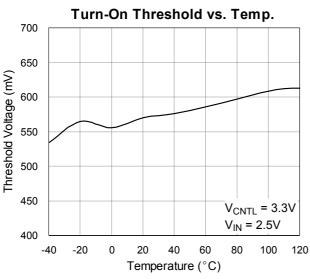
Fig.5 REFEN Pin Shutdown Threshold, VTRIGGER

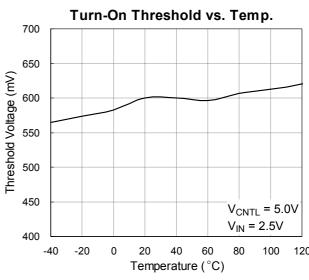


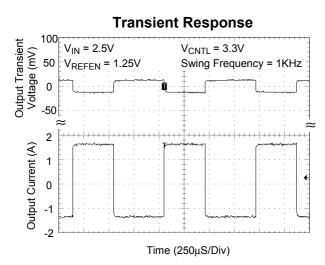
Typical Operating Characteristics

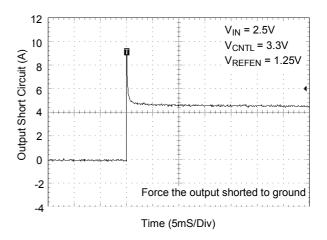














Applications Information

Internal parasitic diode

Avoid forward-bias internal parasitic diode, VOUT to VCNTL, and VOUT to VIN, the VOUT should not be forced some voltage respect to ground on this pin while the VCNTL or VIN is disappeared.

Consideration while designs the resistance of voltage divider

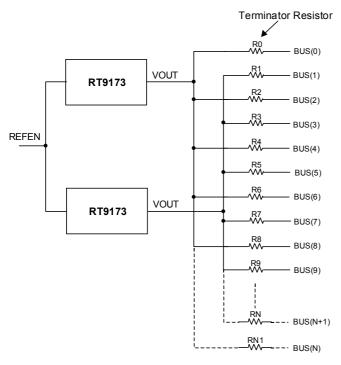
Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on REFEN is below 0.2V.

In addition to item 1, the capacitor and voltage divider form the low-pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.

How to reduce power dissipation on Notebook PC or the dual channel DDR SDRAM application?

In notebook application, using RichTek's Patent "Distributed Bus Terminator Topology" with choosing RichTek's product is encouraged.

Distributed Bus Terminating Topology



Thermal Consideration

RT9173/A regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continuous normal load conditions however, the maximum junction temperature rating of 125°C must not be exceeded.

Higher continuous currents or ambient temperature require additional heatsinking. Heat sinking to the IC package must consider the worst case power dissipation which may occur.

It should also be note that with the VCNTL equal to 5V, the point of thermal shutdown will be degraded by approx. 20°C compared to the VCNTL equipped with 3.3V. It is highly recommended that to use the 3.3V rail acted as the VCNTL so as to minimize the thermal concern of the RT9173CS in the SOP-8 package.

Layout Consideration

The RT9173CS regulator is packaged in plastic SOP-8 package. This small footprint package is unable to convectively dissipate the heat generated when the regulator is operating at high current levels. In order to control die operating temperatures, the PC board layout should allow for maximum possible copper area at the VCNTL pins of the RT9173CS.

The multiple VCNTL pins on the SOP-8 package are internally connected, but lowest thermal resistance will result if these pins are tightly connected on the PC board. This will also aid heat dissipation at high power levels.

If the large copper around the IC is unavailable, a buried layer may be used as a heat spreader, Use vias to conduct the heat into the buried or backside of PCB layer. The vias should be small enough to retain solder when the board is wave-soldered. (See Fig.6 shown on next page).

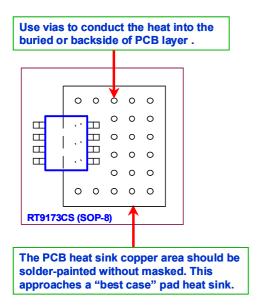
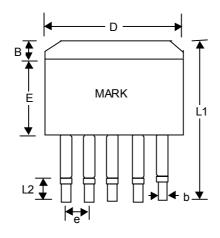


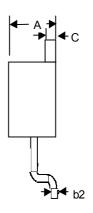
Fig. 6 Layout Consideration

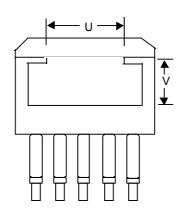
To prevent this maximum junction temperature from being exceeded, the appropriate power plane heat sink *MUST* be used. Higher continuous currents or ambient temperature require additional heatsinking.



Package Information

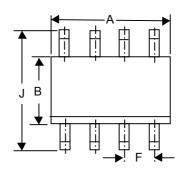


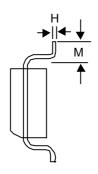


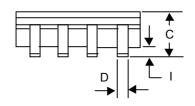


O. mala al	Dimensions I	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
D	9.652	10.668	0.380	0.420	
В	1.143	1.676	0.045	0.066	
Е	8.128	9.652	0.320	0.380	
А	4.064	4.826	0.160	0.190	
С	1.143	1.397	0.045	0.055	
U	6.223 Ref.		0.245 Ref.		
V	7.620 Ref.		0.300 Ref.		
L1	14.605	15.875	0.575	0.625	
L2	2.286	2.794	0.090	0.110	
b	0.660	0.914	0.026	0.036	
b2	0.305	0.584	0.012	0.023	
е	1.524	1.829	0.060	0.072	

5-Lead TO-263 Plastic Surface Mount Package







Cumab al	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	4.801	5.004	0.189	0.197	
В	3.810	3.988	0.150	0.157	
С	1.346	1.753	0.053	0.069	
D	0.330	0.508	0.013	0.020	
М	0.406	1.270	0.016	0.050	
F	1.194	1.346	0.047	0.053	
Ī	0.102	0.254	0.004	0.010	
J	5.791	6.198	0.228	0.244	
Н	0.178	0.254	0.007	0.010	

8-Lead SOP Plastic Package

RT9173/A



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