

# RFM12N35, RFM12N40

12A, 350V and 400V, 0.500 Ohm,  
N-Channel Power MOSFETs

September 1998

## Features

- 12A, 350V and 400V
- $r_{DS(ON)} = 0.500\Omega$

## Ordering Information

PART NUMBER	PACKAGE	BRAND
RFM12N35	TO-204AA	RFM12N35
RFM12N40	TO-204AA	RFM12N40

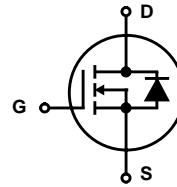
NOTE: When ordering, use the entire part number.

## Description

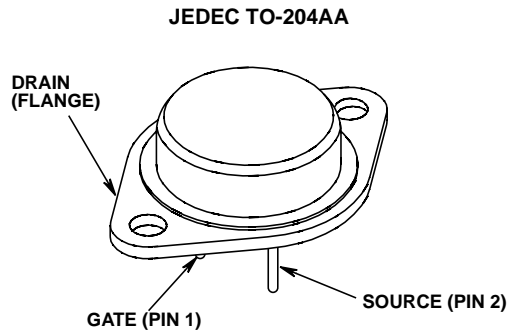
These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17434.

## Symbol



## Packaging



## RFM12N35, RFM12N40

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFM12N35	RFM12N40	UNITS	
Drain to Source Voltage (Note 1) . . . . .	$V_{DS}$	350	400	V
Drain to Gate Voltage ( $R_{GS} = 1M\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	350	400	V
Continuous Drain Current . . . . .	$I_D$	12	12	A
Pulsed Drain Current (Note 3) . . . . .	$I_{DM}$	24	24	A
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$	$\pm 20$	V
Maximum Power Dissipation . . . . .	$P_D$	150	150	W
Linear Derating Factor . . . . .		1.2	1.2	W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFM12N35	$BV_{DSS}$	$I_D = 250\text{mA}, V_{GS} = 0\text{V}$	350	-	-	V
			RFM12N40	400	-	-
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ , (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0$ $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0,$ $T_C = 125^\circ\text{C}$	-	-	1	$\mu\text{A}$
			-	-	25	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 12\text{A}, V_{GS} = 10\text{V}$ , (Figures 6, 7)	-	-	0.500	$\Omega$
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 6\text{A}, V_{GS} = 10\text{V}$ $I_D = 12\text{A}, V_{GS} = 10\text{V}$	-	-	3	V
			-	-	6.0	V
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx 6\text{A}, V_{DS} = 200\text{V}, R_G = 50\Omega,$ $V_{GS} = 10\text{V}, R_L = 33\Omega,$ (Figures 10, 11, 12)	-	30	50	ns
Rise Time	$t_r$		-	105	150	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	480	750	ns
Fall Time	$t_f$		-	140	200	ns
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$ (Figures 9)	-	-	3000	pF
Output Capacitance	$C_{OSS}$		-	-	900	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	-	400	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.83	$^\circ\text{C/W}$

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$I_{SD} = 6\text{A}$	-	-	1.4	V
Diode Reverse Recovery Time	$t_{rr}$	$I_{SD} = 4\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	950	-	ns

NOTE:

- Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Repetitive rating: pulse width is limited by maximum junction temperature.

**Typical Performance Curves** Unless Otherwise Specified

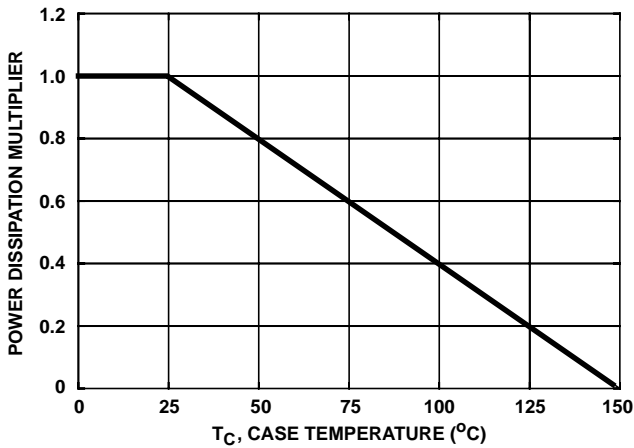


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

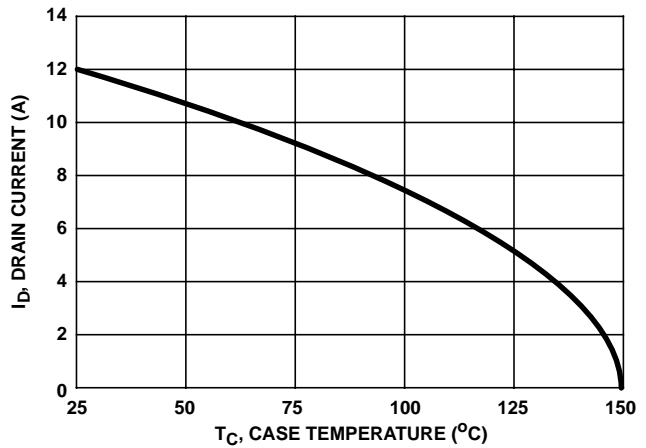


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

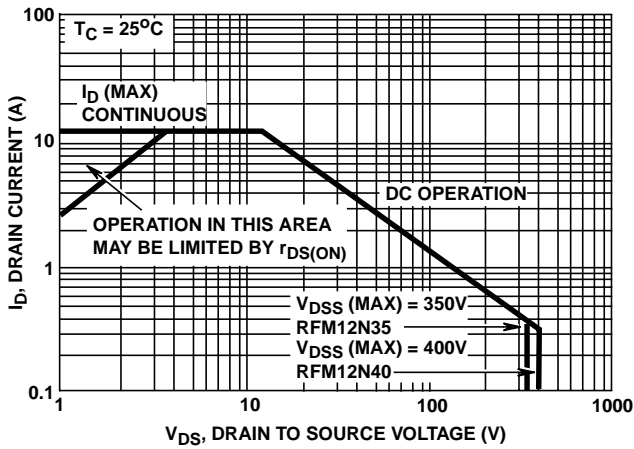


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

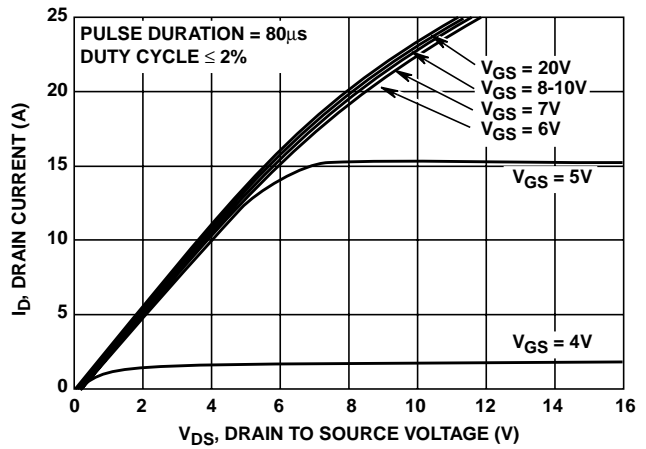


FIGURE 4. SATURATION CHARACTERISTICS

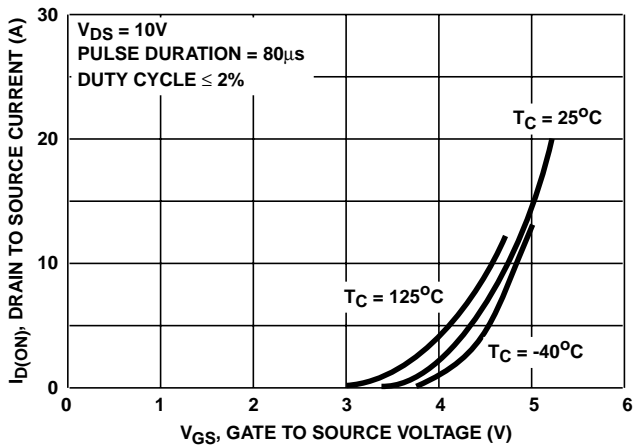


FIGURE 5. TRANSFER CHARACTERISTICS

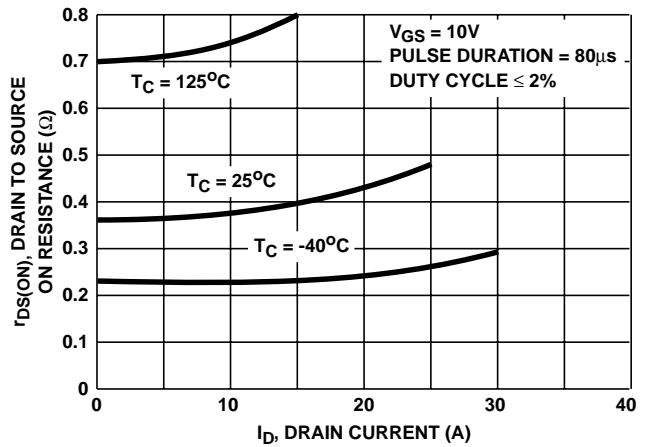


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

**Typical Performance Curves** Unless Otherwise Specified (Continued)

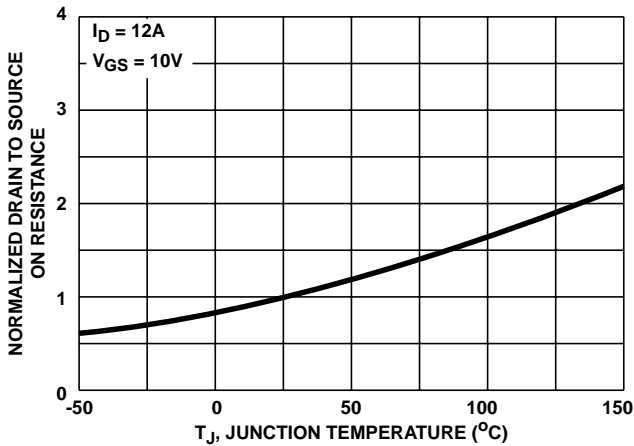


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

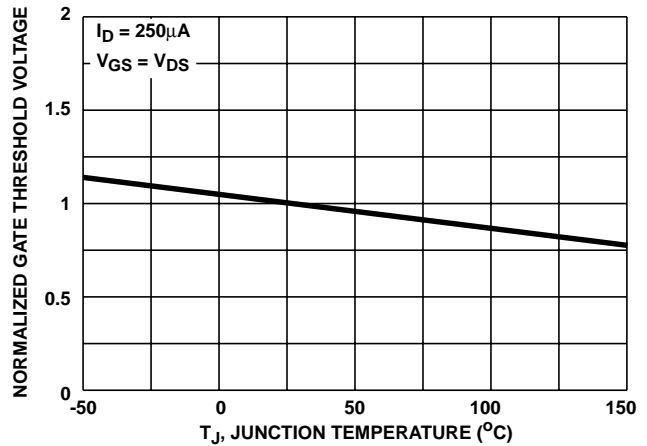


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

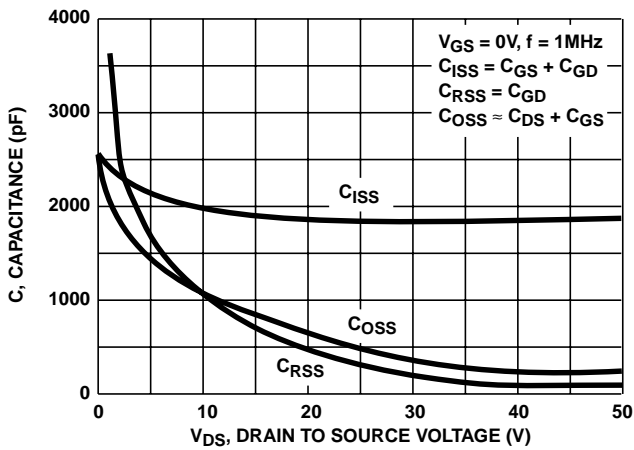
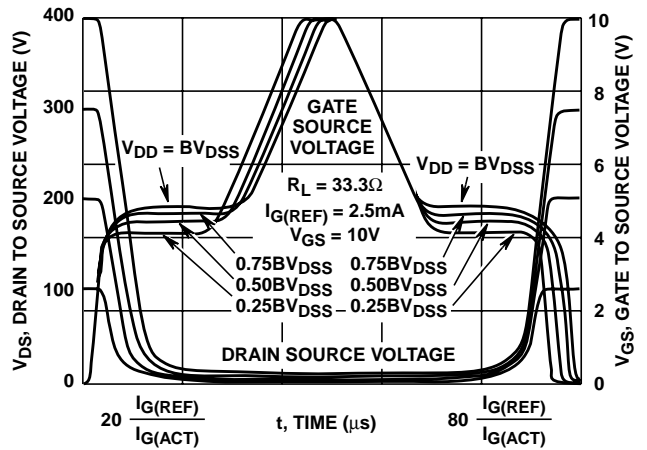


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and 7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

**Test Circuits and Waveforms**

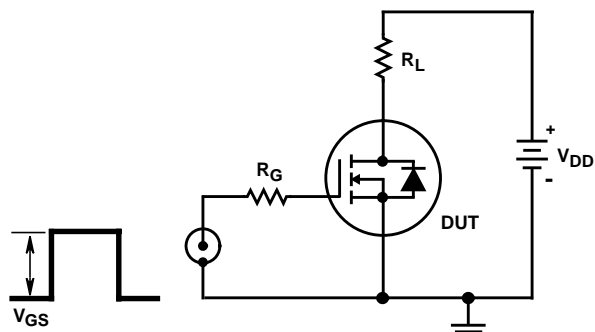


FIGURE 11. SWITCHING TIME TEST CIRCUIT

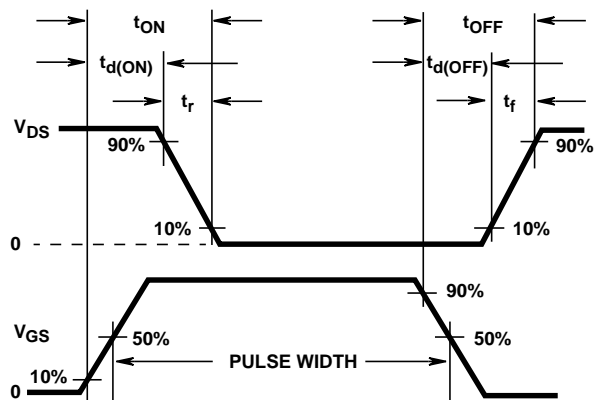


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS