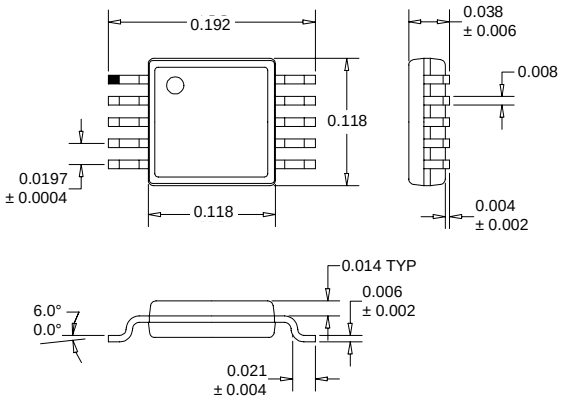
3V 900MHZ UPCONVERTER/ DRIVER AMPLIFIER

Typical Applications

- TDMA/AMPS Cellular Systems
- CDMA/AMPS Cellular Systems
- Portable Battery Powered Equipment

Product Description

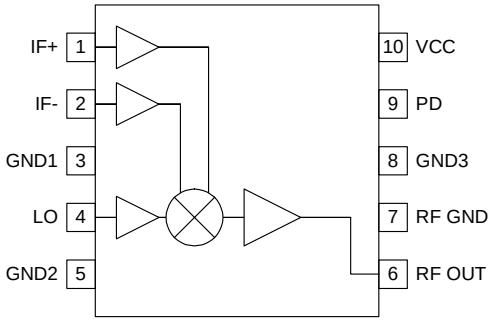
The RF2640 is a complete upconverter and power amplifier driver designed for TDMA and CDMA applications. The device features balanced IF inputs, single-ended LO input and RF output for ease of interface. Packaged in an industry standard MSOP-10 package, the device provides a low-cost solution while easing board space limitations.



Package Style: MSOP-10

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Single Supply 3.0V Operation
- +8.5dBm Output P1dB
- +19dBm Output IP3
- Power Down Control
- 23dB Conversion Gain

Ordering Information

RF2640	3V 900MHz Upconverter/ Driver Amplifier
RF2640 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
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Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

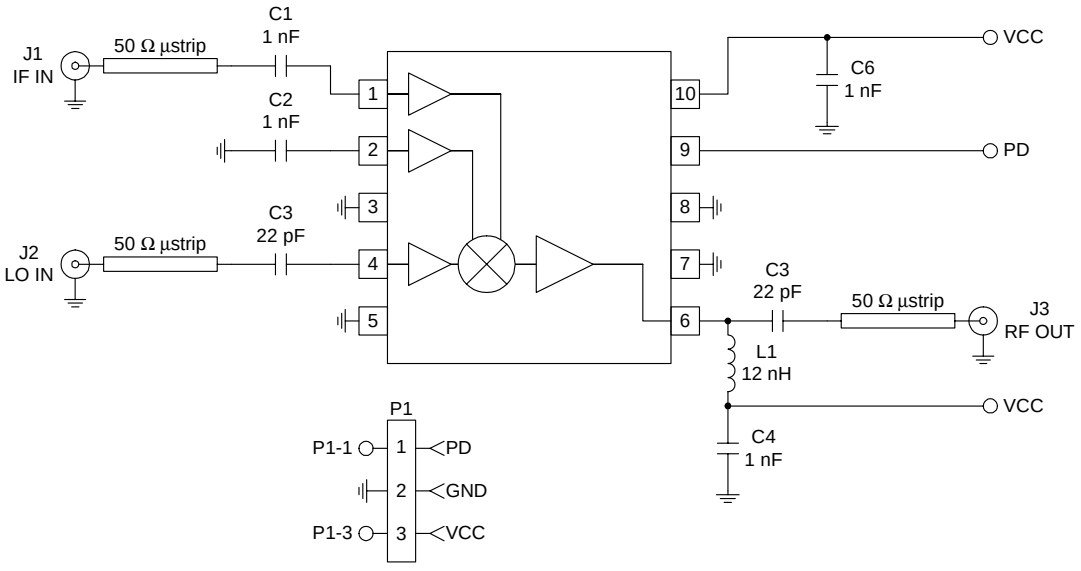
Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Input RF Power	+3	dBm
Operating Ambient Temperature	-30 to +80	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

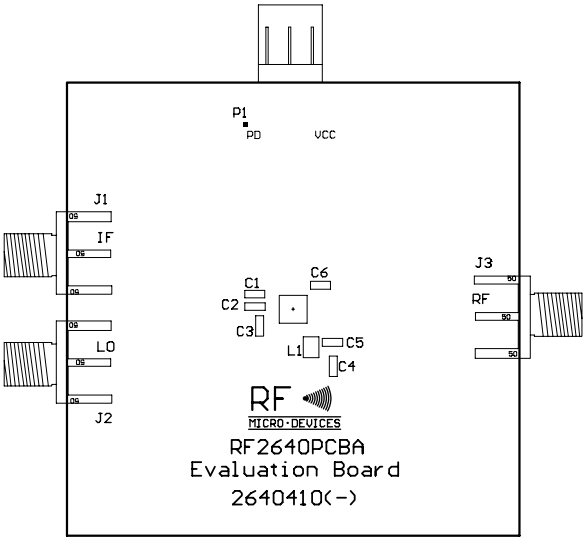
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.7V, RF Out=836MHz, LO=1016MHz @ -8dBm, IF=180MHz @ -30dBm
RF Output Frequency Range	824		849	MHz	
Conversion Gain	22	23.5	26	dB	
Noise Figure		12		dB	Single Sideband
Output P1dB		+8.5		dBm	
Output IP3	+17	+18.5		dBm	
Output VSWR		1.25:1			50Ω
IF Input					
IF Frequency		180		MHz	
IF Input Level	-60		-15	dBm	
Single-Ended Input Impedance		70		Ω	
IF to RF Isolation		45		dB	
LO Input					
LO Frequency Range	1004		1029	MHz	
LO Level	-10	-8	-6	dBm	
LO to RF Output Leakage			-18	dBm	IF Input<-24dBm
LO Input VSWR		1.25:1			50Ω
Power Supply					
Voltage	2.7		3.3	V	
Current Consumption		45	65	mA	Device is active (ON); V_{PD}=1.8V
			10	µA	Device is inactive (OFF); V_{PD}=0.6V
Power Down Voltage	0.0		0.6	V	Device is inactive (OFF); V_{PD}=0.6V
	1.2		1.8	V	Device is active (ON); V_{PD}=1.8V
Power Down Current			0.1	mA	Device is active (ON); V_{PD}=1.8V

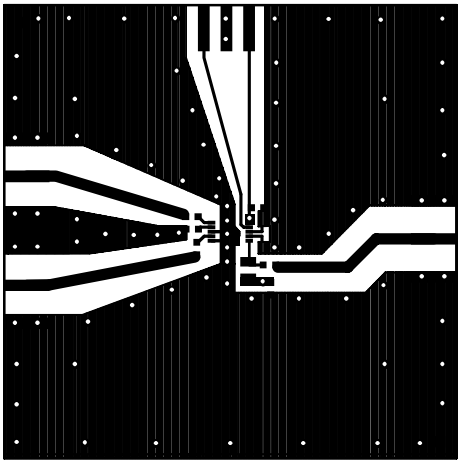
Pin	Function	Description	Interface Schematic
1	IF+	Balanced IF input pin. This pin is internally DC-biased and should be DC-blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC-coupled to ground. The single-ended input impedance is 50Ω.	
2	IF-	Same as pin 1, except complementary input.	
3	GND1	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
4	LO+	Single-ended LO input pin. This pin is internally DC-biased and should be DC-blocked if connected to a device with a DC level present. The single-ended input impedance is 50Ω.	
5	GND2	Same as pin 3, except complementary input.	
6	RF OUT	RF Output Pin. The output impedance is 50Ω.	
7	RF GND	This pin requires a small inductance to ground to optimize the gain and third order intercept point. See Evaluation Board Layout. The trace length on the board is approximately 65mils.	
8	GND3	Same as pin 7.	
9	PD	Power down control. When logic “high” (between 1.2V and 1.8V) the device is active and all circuits are operating. When logic “low” (between 0.0V and 0.6V) the device is inactive and all circuits are turned off.	
10	VCC	Supply Voltage pin. External bypassing is required. External RF, LO, and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	

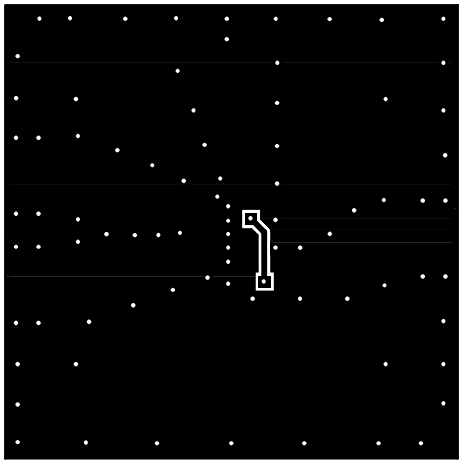
Evaluation Board Schematic
RF=836MHz, LO=1016MHz
(Download Bill of Materials from www.rfmd.com.)

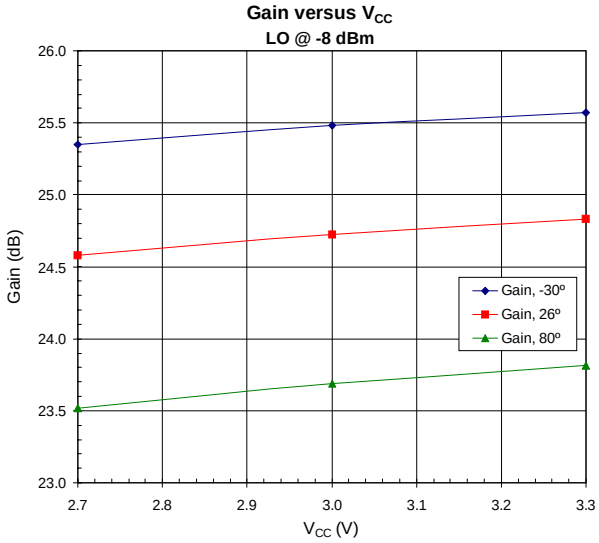


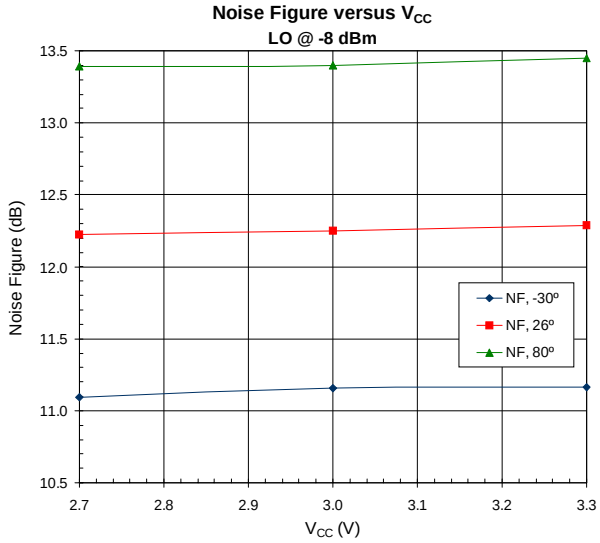
Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.031”, Board Material FR-4

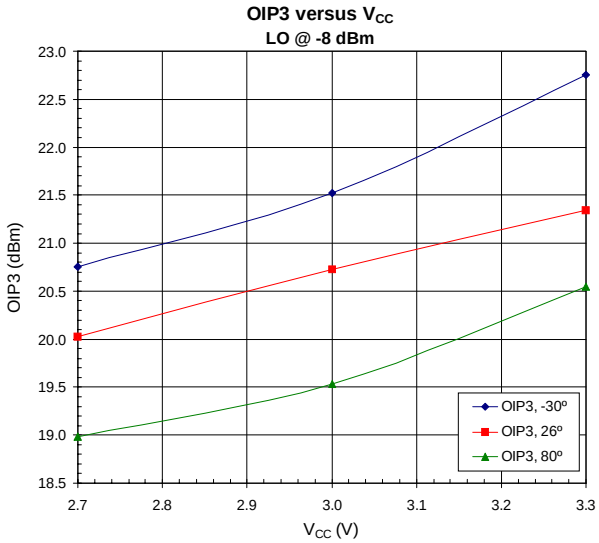


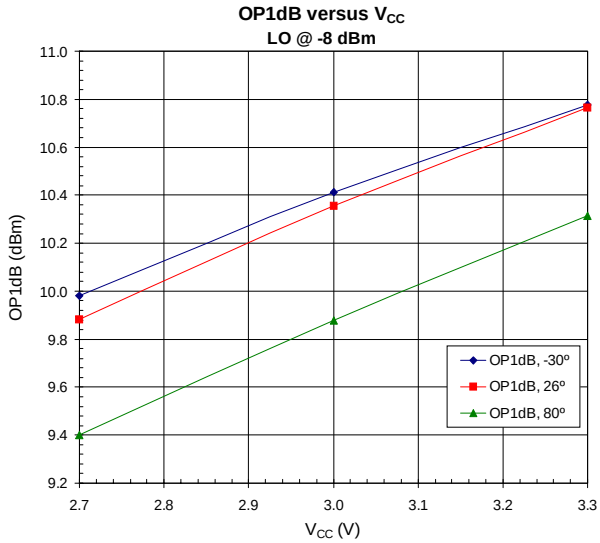


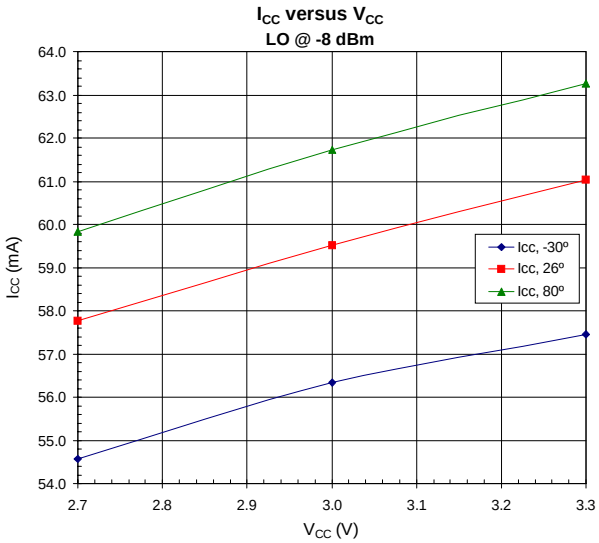


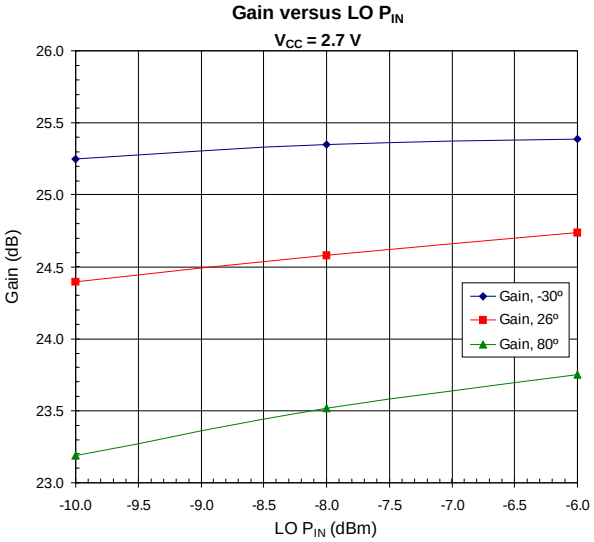

Gain versus V_{CC}
LO @ -8 dBm
Gain (dB)
V_{CC} (V)
Gain, -30º
Gain, 26º
Gain, 80º

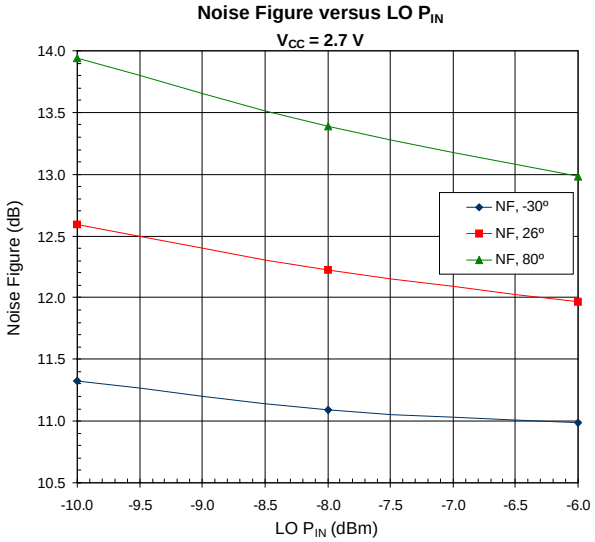

Noise Figure versus V_{CC}
LO @ -8 dBm
Noise Figure (dB)
V_{CC} (V)
NF, -30º
NF, 26º
NF, 80º

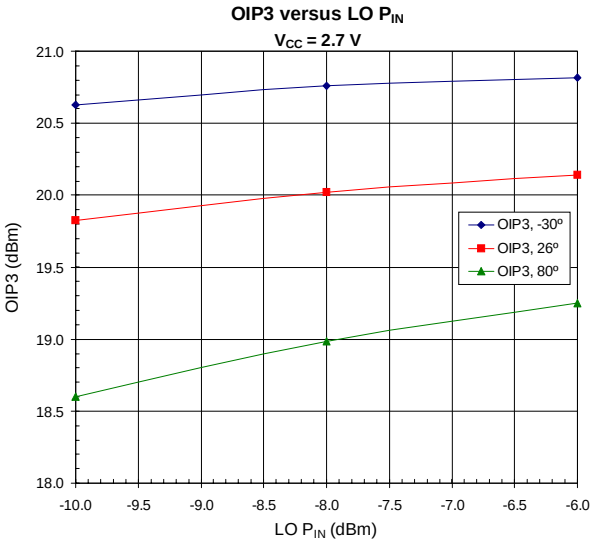

OIP3 versus V_{CC}
LO @ -8 dBm
OIP3 (dBm)
V_{CC} (V)
OIP3, -30º
OIP3, 26º
OIP3, 80º

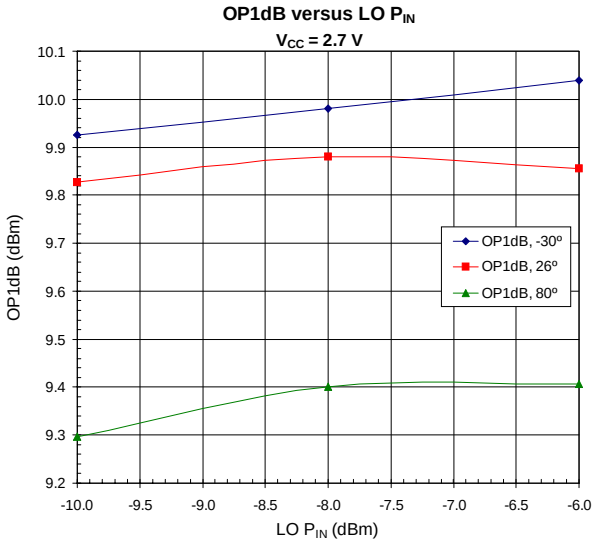

OP1dB versus V_{CC}
LO @ -8 dBm
OP1dB (dBm)
V_{CC} (V)
OP1dB, -30º
OP1dB, 26º
OP1dB, 80º


I_{CC} versus V_{CC}
LO @ -8 dBm
I_{CC} (mA)
V_{CC} (V)
Icc, -30º
Icc, 26º
Icc, 80º


Gain versus LO P_{IN}
V_{CC} = 2.7 V
Gain (dB)
LO P_{IN} (dBm)
Gain, -30º
Gain, 26º
Gain, 80º


Noise Figure versus LO P_{IN}
V_{CC} = 2.7 V
Noise Figure (dB)
LO P_{IN} (dBm)
NF, -30º
NF, 26º
NF, 80º


OIP3 versus LO P_{IN}
V_{CC} = 2.7 V
OIP3 (dBm)
LO P_{IN} (dBm)
OIP3, -30º
OIP3, 26º
OIP3, 80º


OP1dB versus LO P_{IN}
V_{CC} = 2.7 V
OP1dB (dBm)
LO P_{IN} (dBm)
OP1dB, -30º
OP1dB, 26º
OP1dB, 80º