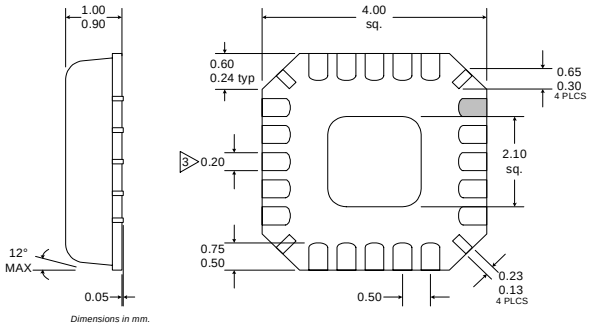
W-CDMA AND PCS LOW NOISE AMPLIFIER/MIXER DOWNCONVERTER

Typical Applications

- W-CDMA Handsets
- PCS Handsets
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

The RF2469 is a receiver front-end designed for the receive section of W-CDMA and PCS applications. It is designed to amplify and downconvert RF signals while providing 23dB of stepped gain control range and features digital control of the LNA gain and mixer gain. A further feature of the chip is adjustable IIP3 of the LNA and mixer using an off-chip current setting resistor. Noise Figure, IP3, and other specs are designed to be compatible with W-CDMA and PCS communications. The IC is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process and packaged in a 20-pin, leadless chip carrier with an exposed die flag.

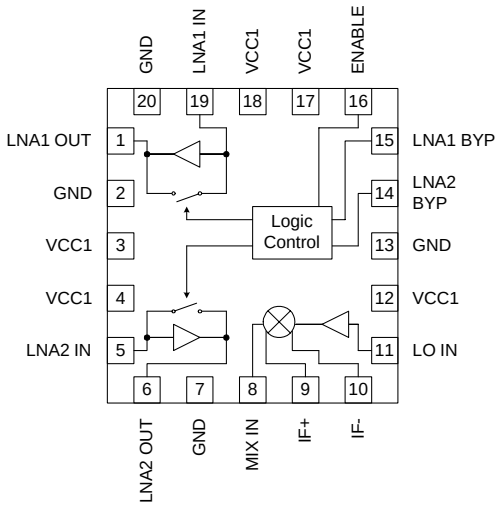


NOTES:
1. Shaded lead is Pin 1.
2. Pin 1 identifier must exist on top surface of package by identification mark or feature on the package body. Exact shape and size is optional.
3. Dimension applies to plated terminal: to be measured between 0.02 mm and 0.25 mm from terminal end.
4. Package Warpage: 0.05 mm max.
5. Die Thickness Allowable: 0.305 mm max.

Package Style: LCC, 20-Pin, 4x4

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Complete Receiver Front-End
- Stepped LNA/Mixer Gain Control
- Adjustable LNA/Mixer Bias Current
- 23dB Maximum Cascade Gain
- 2.5dB Noise Figure at Maximum Cascade Gain

Ordering Information

RF2469	W-CDMA and PCS Low Noise Amplifier/Mixer Downconverter
RF2469 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

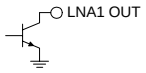
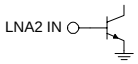
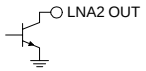
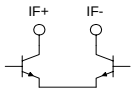
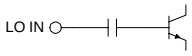
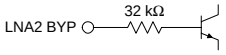
Parameter	Rating	Unit
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

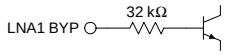
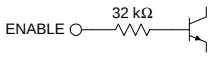
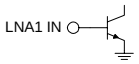
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.78V, RF=2140MHz, LO=2330MHz @ -10dBm
RF Frequency Range		2110 to 2170		MHz	
LO Frequency Range		2300 to 2360		MHz	
IF Frequency Range		190		MHz	
LNA 1					1st LNA current setting resistor (R1) is 1.1kΩ. 1st LNA current and IIP3 are adjustable via R1.
Gain	9	10	11	dB	
Noise Figure		1.45	1.6	dB	
Input IP3	+7.0	+10.0		dBm	
Input VSWR		<2:1			
Output VSWR		<2:1			
P1dB		-3		dB	See LNA P1dB Compression Point section.
Current		4.5		mA	
LNA 1 Bypass					
Gain	-5	-2	0	dB	
Noise Figure		2	2.4	dB	
Input IP3	+20.0	+25.0		dBm	
Input VSWR		<2:1			
Output VSWR		<2:1			
Current		1.6		mA	
Local Oscillator Input					Single-ended. Optimum LO Drive -10dBm to -5dBm.
Input Level		-10		dBm	
LO to IF Isolation		+38		dB	
Mixer/LNA2 BYP High					T=25°C, V_{CC}=2.78V, RF=2140MHz, LO=2330MHz@-10dBm, LNA2BYP=1, EN=1
Gain	15	17		dB	
Noise Figure		4.5		dB	
Input IP3	-7.0	-3.0		dBm	LNA 2 current setting resistor (R2) is 2.4kΩ
Input IP2	+11.0	+14.0		dBm	LNA 2 current and IIP3 are adjustable via R2
Mixer/LNA2 BYP Low					T=25°C, V_{CC}=2.78V, RF=2140MHz, LNA2BYP=0, EN=1
Gain	4	6		dB	
Noise Figure		10.5		dB	
Input IP3	+2.0	+4.0		dBm	LNA 2 current setting resistor (R2) is 2.4kΩ
Input IP2	+19.0	+22.0		dBm	LNA 2 current and IIP3 are adjustable via R2

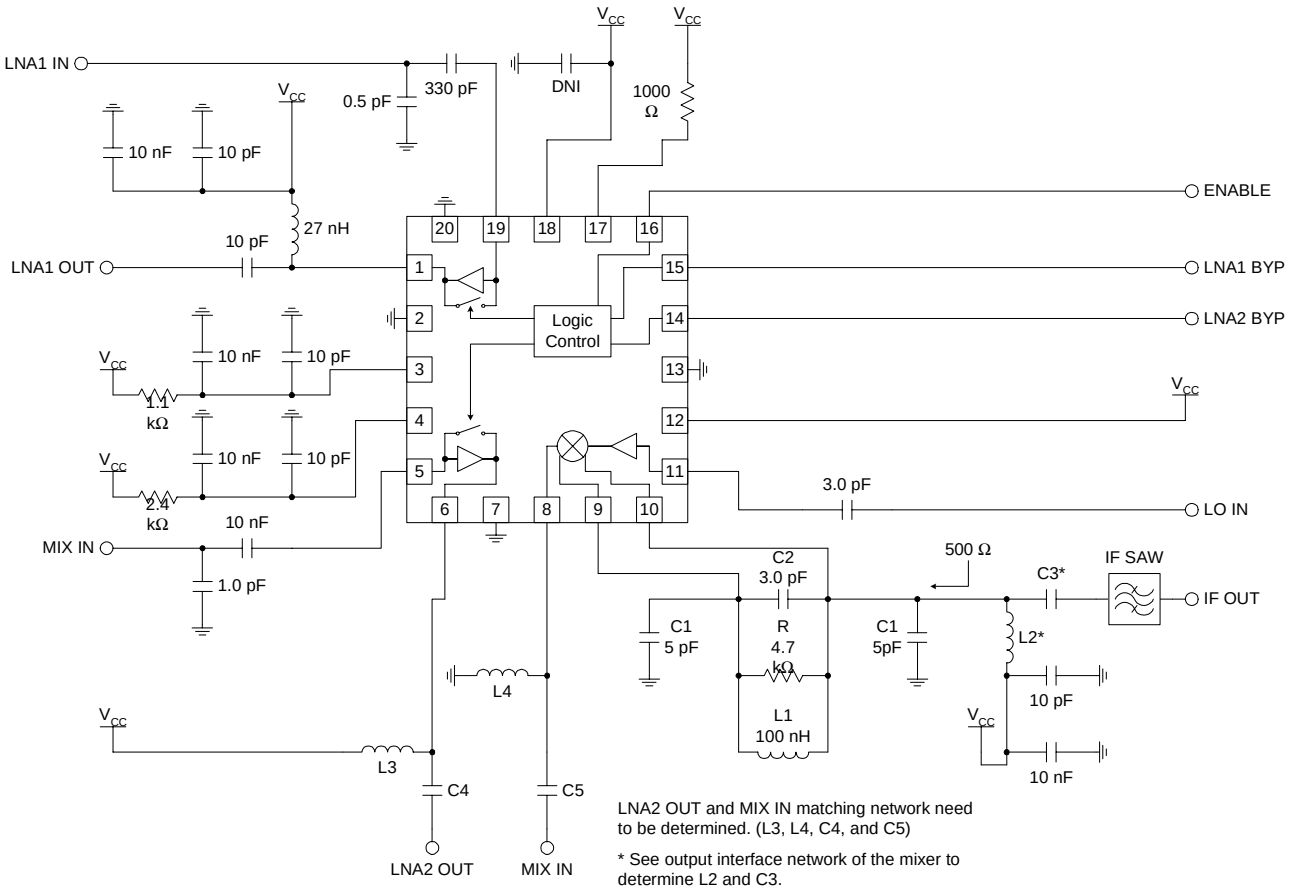
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Cascade - Condition 1					LNA1 BYP high, LNA2 BYP high, ENABLE high. Assuming 2.5dB filter loss.
Gain		24.5		dB	
Noise Figure		2.55		dB	
Input IP3		-10.5		dBm	
Current Consumption*		18.6	23	mA	
Cascade - Condition 2					LNA1 BYP high, LNA2 BYP low, ENABLE high. Assuming 2.5dB filter loss.
Gain		13.5		dB	
Noise Figure		5.2		dB	
Input IP3		-3.5		dBm	
Current Consumption*		17	17.5	mA	
Cascade - Condition 3					LNA1 BYP low, LNA2 BYP high, ENABLE high. Assuming 2.5dB filter loss.
Gain		12.5		dB	
Noise Figure		9		dB	
Input IP3		+1.4		dBm	
Current Consumption*		14	15	mA	
Cascade - Condition 4					LNA1 BYP low, LNA2 BYP low, ENABLE High. Assuming 2.5dB filter loss.
Gain		1.50		dB	
Noise Figure		15		dB	
Input IP3		+8.2		dBm	
Current Consumption*		12.5	13.5	mA	
Power Supply					
Voltage	2.7	2.75	3.3	V	

*RF2469 is a very flexible device. Customers may choose different current consumption (see Low Current Configuration section).

Pin	Function	Description	Interface Schematic
1	LNA1 OUT	LNA output pin. This is an open-collector output. Externally matched to 50Ω.	
2	GND	This pin is connected to the ground plane.	
3	VCC1	Supply voltage for LNA1. An external resistor is placed in series with this pin to adjust the current and IIP3 of LNA1. A nominal value of 1.1kΩ sets the LNA1 current to 4.5mA with a minimum IIP3 of +7dBm. External RF bypassing is required. The trace length between the bypass caps and the pin should be minimized. Connect ground sides of caps directly to ground.	
4	VCC1	Supply voltage for LNA2. An external resistor is placed in series with this pin to adjust the current and IIP3 of LNA2. A nominal value of 2.4kΩ sets the LNA2 current to 1.6mA. External RF bypassing is required. The trace length between the bypass caps and the pin should be minimized. Connect ground sides of caps directly to ground.	
5	LNA2 IN	RF input to LNA2. This pin is internally DC-biased and, if it is connected to a device with DC present, should be DC-blocked with a capacitor suitable for the frequency of operation.	
6	LNA2 OUT	LNA output pin. This is an open-collector output. In normal operation, this pin is externally cascaded with pin 8 (MIX IN).	
7	GND	Ground connection. For best performance, keep traces physically short and connect directly to ground plane.	
8	MIX IN	Mixer RF input pin. This pin requires a DC path to ground. In normal operation, this pin is externally cascaded with pin 6 (LNA2 OUT). The external match ensures a conjugate match between pin 6 and pin 8 while providing a DC path to ground for pin 8 and a DC-block between pin 8 and pin 6.	
9	IF+	IF output pin. The output is balanced. A current combiner external network performs a differential to single-ended conversion and sets the output impedance. There must be a DC path from V_{CC} to this pin. This is normally achieved with the current combiner network. A DC blocking cap must be present if the IF filter input has a DC path to ground.	
10	IF-	Same as pin 9, except complementary output.	See pin 9.
11	LO IN	Mixer LO single-ended input. The pin is internally DC-blocked. External matching sets impedance.	
12	VCC1	Supply voltage for LO buffer. External RF bypassing is required. The trace length between the bypass caps and the pin should be minimized. Connect ground sides of caps directly to ground.	
13	GND	This pin is connected to the ground plane.	
14	LNA2 BYP	Logic control for LNA2 gain. A logic high (≥2.4V) places LNA2 in the high gain mode. A logic low (≤0.3V) place LNA2 in the bypass mode.	

Pin	Function	Description	Interface Schematic
15	LNA1 BYP	Logic control for LNA1 gain. A logic high (≥2.4V) places LNA1 in the high gain mode. A logic low (≤0.3V) place LNA1 in the bypass mode.	
16	ENABLE	A logic control for mixer and LO buffer. A logic high (≥2.4V) turn the mixer and LO buffer on. A logic low (≤0.3V) disable the mixer and LO buffer.	
17	VCC1	Supply voltage for the mixer. An external resistor is place in series with this pin to adjust the mixer current. A nominal value of 1000Ω set the mixer current to ~10mA. External RF bypassing is required. The trace length between the bypass caps and the pin should be minimized. Connect ground sides of caps directly to ground.	
18	VCC1	Supply voltage for IC. External RF bypassing is required. The trace length between the bypass caps and the pin should be minimized. Connect ground sides of caps directly to ground.	
19	LNA1 IN	RF input to LNA1. This pin is internally DC-biased and, if it is connected to a device with DC present, should be DC-blocked with a capacitor suitable for the frequency of operation.	
20	GND	Ground connection. For best performance, keep traces physically short and connect directly to ground plane.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

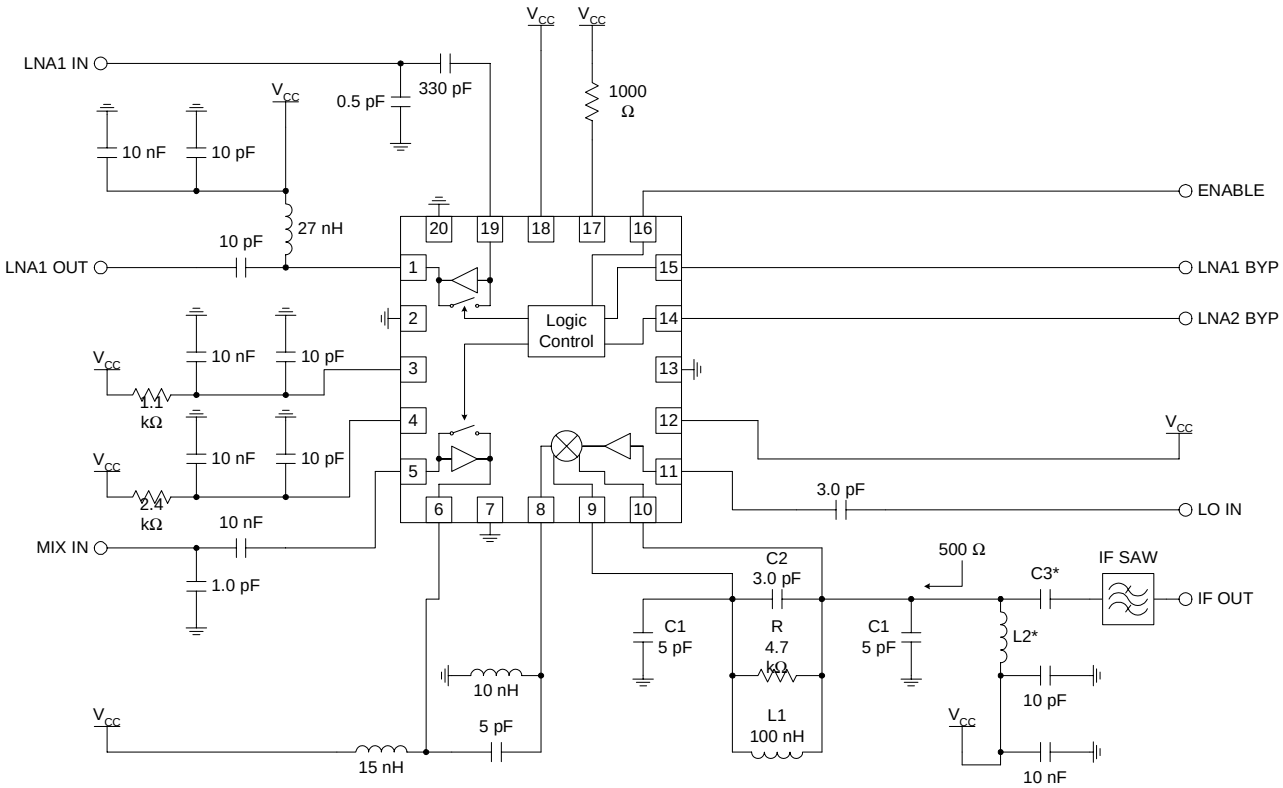
LNA1, LNA2 and Mixer Application Schematic (RF=2140MHz, IF=190MHz)



LNA2 OUT and MIX IN matching network need to be determined. (L3, L4, C4, and C5)

* See output interface network of the mixer to determine L2 and C3.

LNA1, LNA2 Cascade with Mixer Application Schematic (RF=2140MHz, IF=190MHz)



*See output interface network of the mixer to determine L2 and C3.

Output Interface Network of the Mixer

L1, C1, C2, and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C_1 + 2C_2 + C_{EQ})}}$$

Where C_{EQ} is the equivalent stray capacitance and capacitance looking into pins 9 and 10. An average value to use for C_{EQ} is 2.5pF.

R can then be used to set the output impedance according to the following equation:

$$R = \left(\frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P}\right)^{-1}$$

where R_{OUT} is the desired output impedance and R_P is the parasitic equivalent parallel resistance of L1.

C_2 should first be set to 0 and C1 should be chosen as high as possible, while maintaining an R_P of L1 that allows for the desired R_{OUT}. If the self-resonant frequencies of the selected C1 produce unsatisfactory linearity performance, their values may be reduced and compensated for by including C2 capacitor with a value chosen to maintain the desired F_{IF} frequency.

L2 and C3 serve dual purposes. L2 serves as an output bias choke, and C3 serves as a series DC block.

In addition, L2 and C3 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to R_{OUT}. Otherwise, L2 is chosen to be large (suggested 120nH) and C3 is chosen to be large (suggested 22nF) if a DC path to ground is present in the IF filter, or omitted if the filter is DC-blocked.

LNA P1dB Compression Point

For large signal input, this type of LNA will not have a fixed DC bias current. The LNA will tend to self-bias when the input signal level starts increasing above small signal conditions. This particular characteristic will move the DC bias current to a higher DC bias current. Obviously, increasing the bias current will increase the linearity of the LNA.

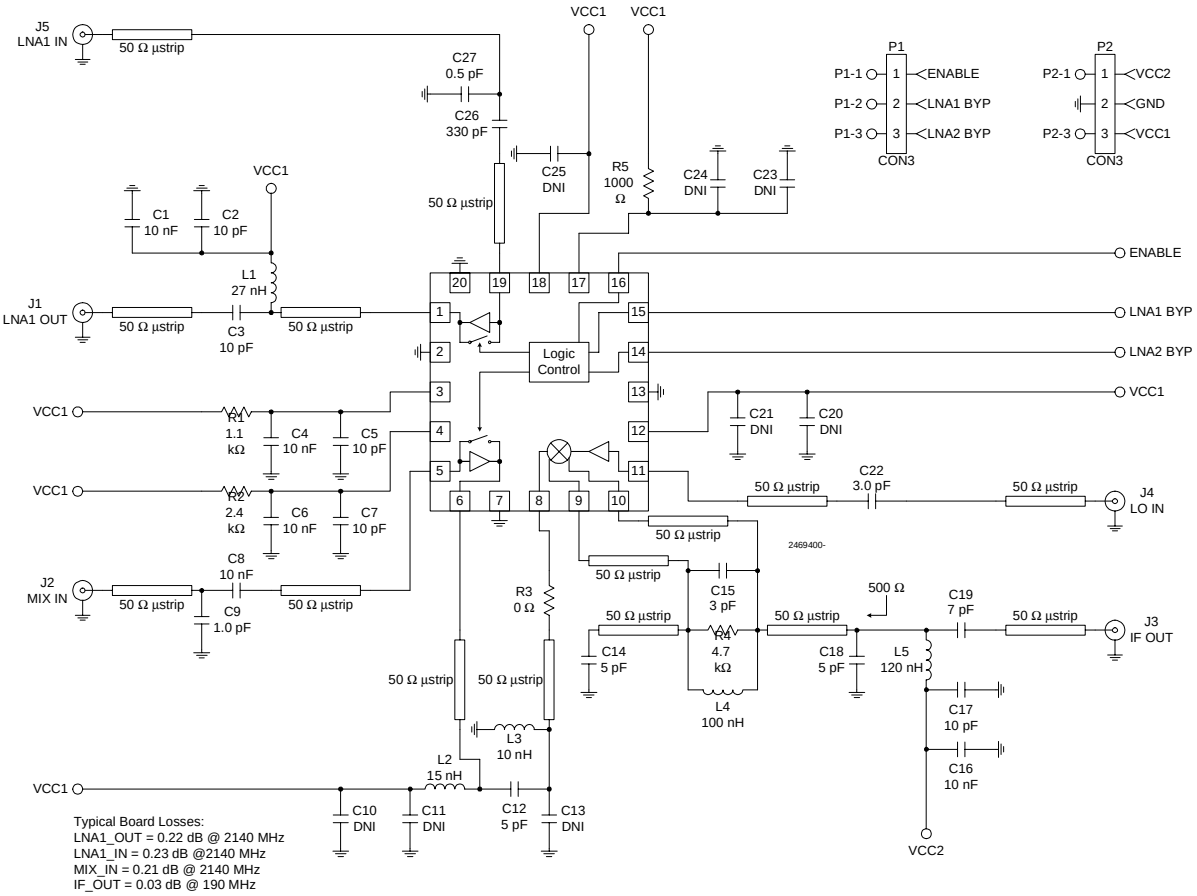
To accurately measure the P1dB, the measurement technique must force the bias current in the LNA to be a constant, while preserving the collector output voltage of the LNA. In order to due this, a separate supply voltage must be used for the bias voltage of the LNA (pin 3) and the open collector supply (pin 1). As the input signal level is increased, the bias voltage must be dropped while monitoring the DC current in the LNA to ensure that it remains constant. Incidentally, the P1dB compression measured with this technique is consistent with the standard approximation relating P1dB to IIP3 (i.e., Input P1dB=IIP3(dBm)-10). Since the IIP3 measurements are done under small signal conditions (the input tones are low power levels), this approximation provides a good figure for P1dB under a constant DC bias condition. For the RF2469, with an IIP3 of approximately +8dBm, the Input P1dB is approximately -2dBm.

However, for many applications, forcing the bias current in the LNA to be constant is not a practical solution. Leaving the LNA to self-bias will not produce any damage to the part and the P1dB performance under this condition will be:

Frequency (MHz)	Gain (dB)	Input P1dB	Output P1dB	LNA Current (mA)
2140	10.5	5.25	14.92	~23

Evaluation Board Schematic
(RF=2140MHz, IF=190MHz)

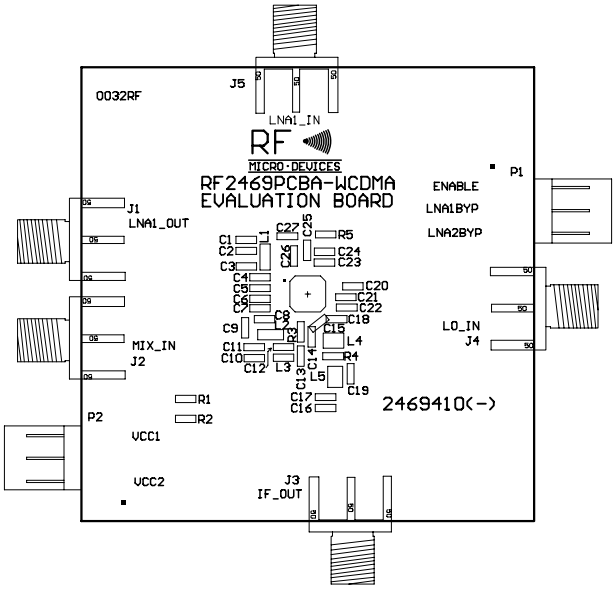
(Download Bill of Materials from www.rfmd.com.)



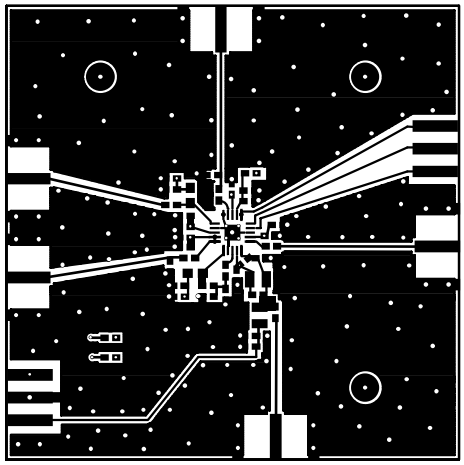
Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.031”, Board Material FR-4, Multi-Layer

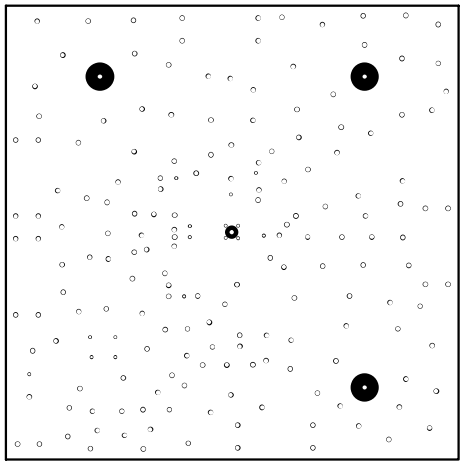
Assembly



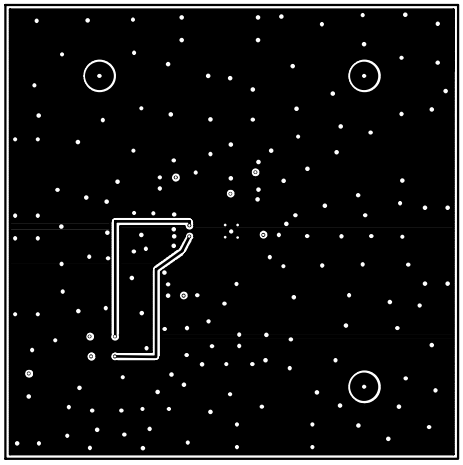
Top



Power Plane



Back



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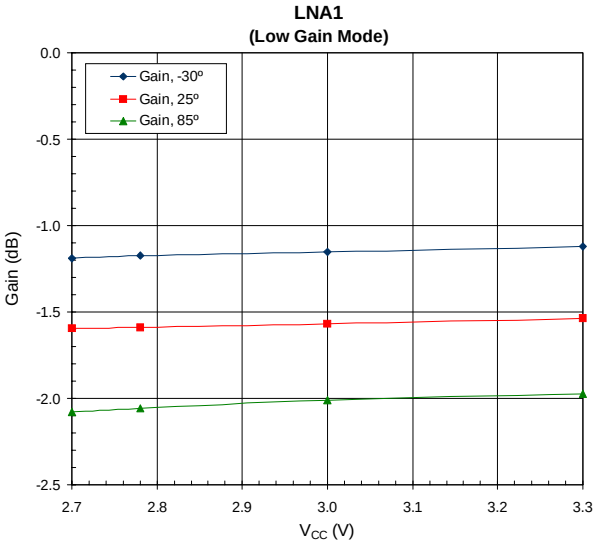
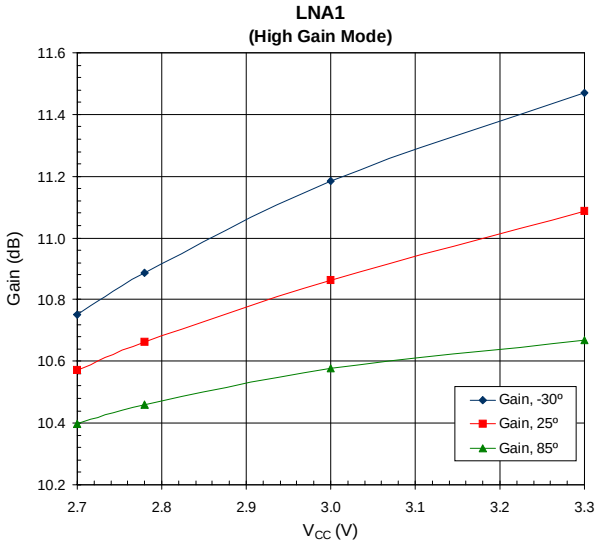
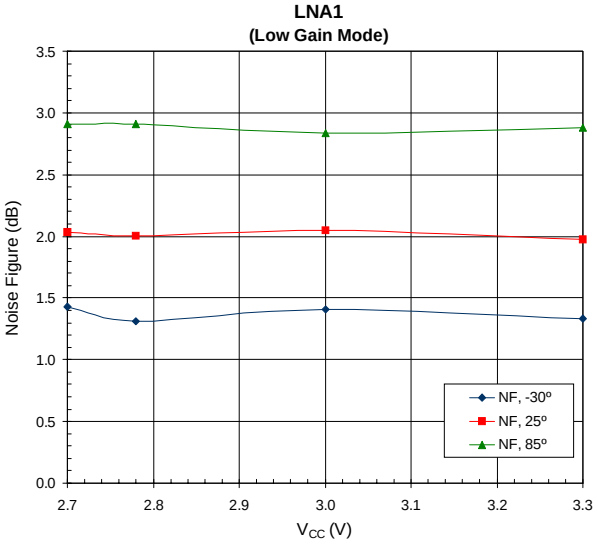
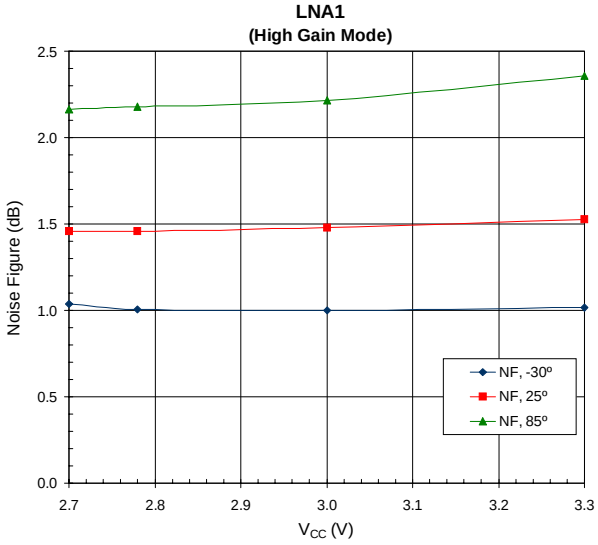
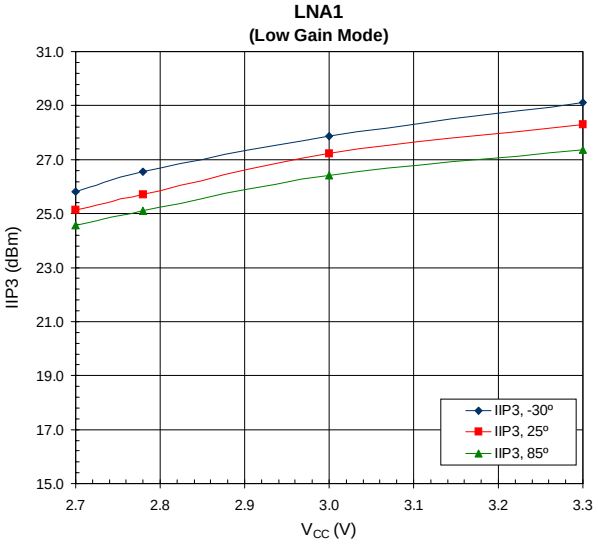
FRONT-ENDS

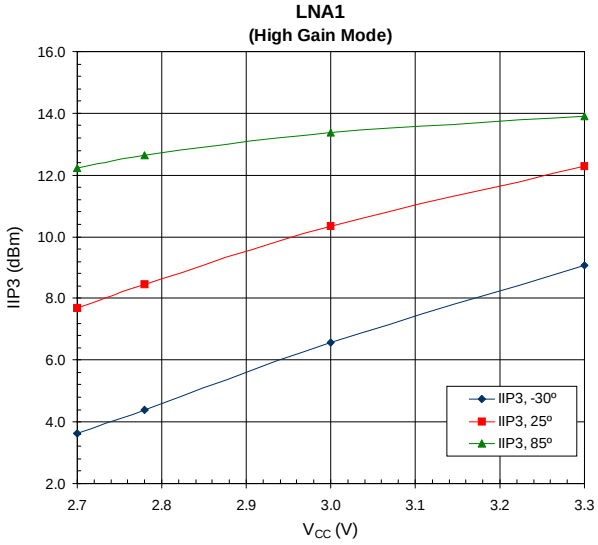

LNA1
(Low Gain Mode)
Gain (dB)
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
Gain, -30º
Gain, 25º
Gain, 85º
2.7
2.8
2.9
3.0
3.1
3.2
3.3
VCC (V)

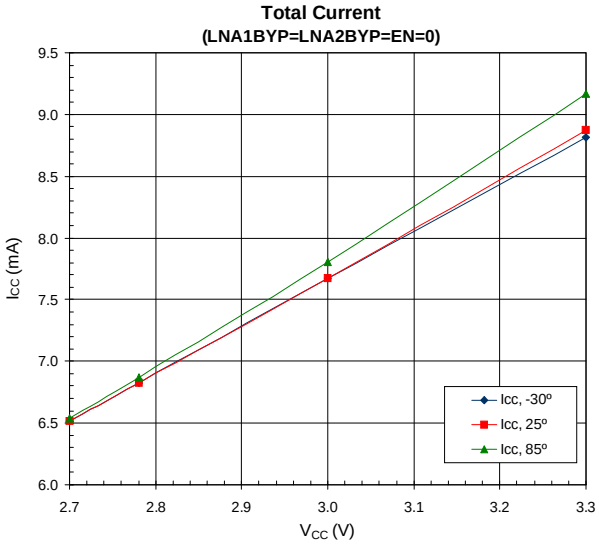

LNA1
(High Gain Mode)
Gain (dB)
11.6
11.4
11.2
11.0
10.8
10.6
10.4
10.2
Gain, -30º
Gain, 25º
Gain, 85º
2.7
2.8
2.9
3.0
3.1
3.2
3.3
VCC (V)

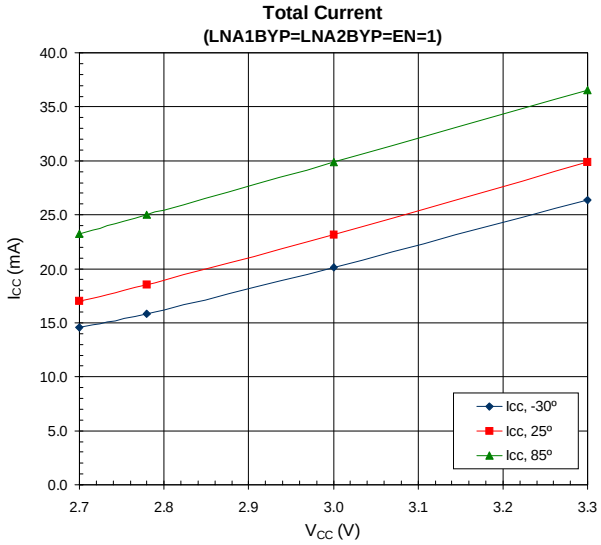

LNA1
(Low Gain Mode)
Noise Figure (dB)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
NF, -30º
NF, 25º
NF, 85º
2.7
2.8
2.9
3.0
3.1
3.2
3.3
VCC (V)


LNA1
(High Gain Mode)
Noise Figure (dB)
2.5
2.0
1.5
1.0
0.5
0.0
NF, -30º
NF, 25º
NF, 85º
2.7
2.8
2.9
3.0
3.1
3.2
3.3
VCC (V)

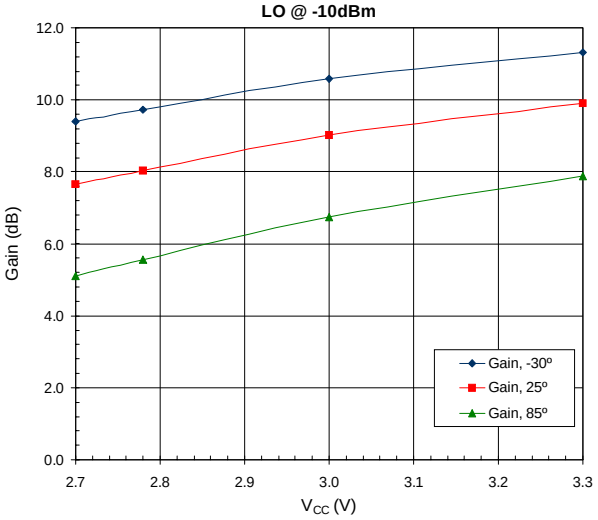

LNA1
(Low Gain Mode)
IIP3 (dBm)
31.0
29.0
27.0
25.0
23.0
21.0
19.0
17.0
15.0
IIP3, -30º
IIP3, 25º
IIP3, 85º
2.7
2.8
2.9
3.0
3.1
3.2
3.3
VCC (V)


LNA1
(High Gain Mode)
IIP3 (dBm)
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
IIP3, -30º
IIP3, 25º
IIP3, 85º
2.7
2.8
2.9
3.0
3.1
3.2
3.3
VCC (V)

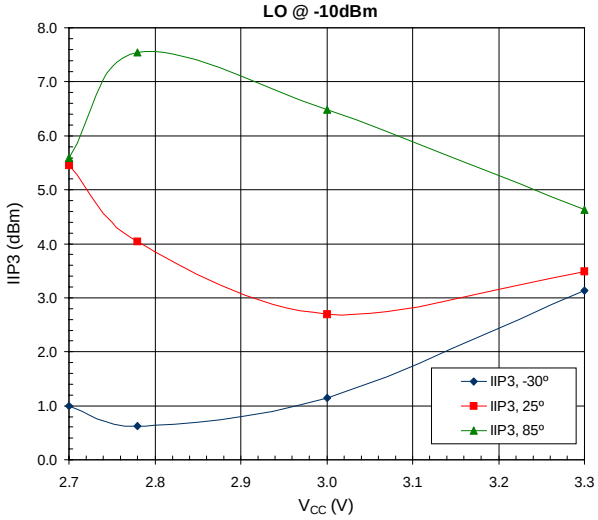

Total Current
(LNA1BYP=LNA2BYP=EN=0)
ICC (mA)
VCC (V)
Icc, -30º
Icc, 25º
Icc, 85º


Total Current
(LNA1BYP=LNA2BYP=EN=1)
ICC (mA)
VCC (V)
Icc, -30º
Icc, 25º
Icc, 85º

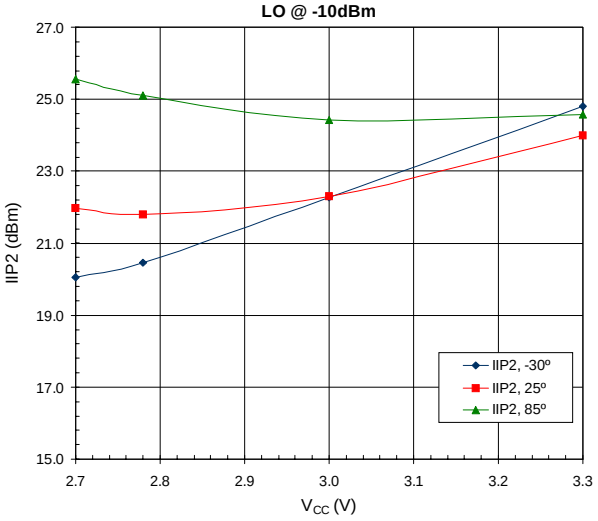
Mixer/LNA2, Low Gain Mode (LNA2BYP=0), LO @ -10dBm



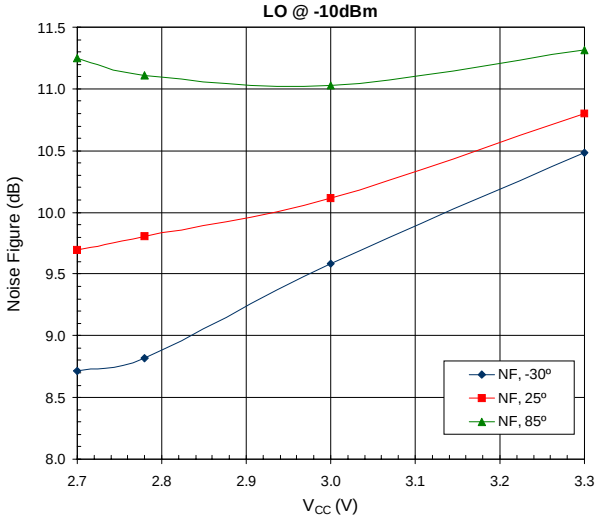
Mixer/LNA2, Low Gain Mode (LNA2BYP=0), LO @ -10dBm



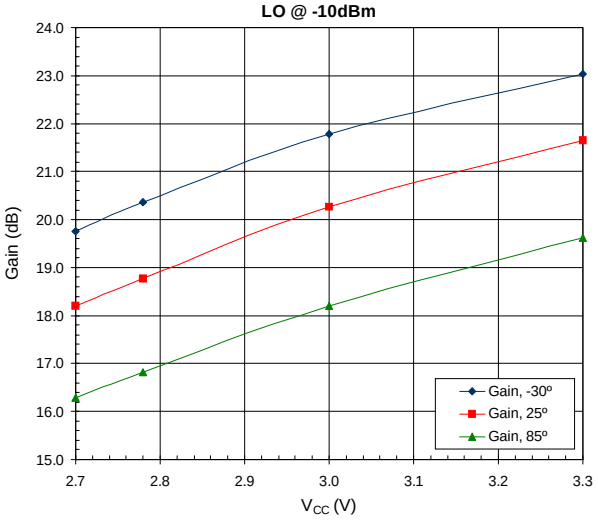
Mixer/LNA2, Low Gain Mode (LNA2BYP=0), LO @ -10dBm



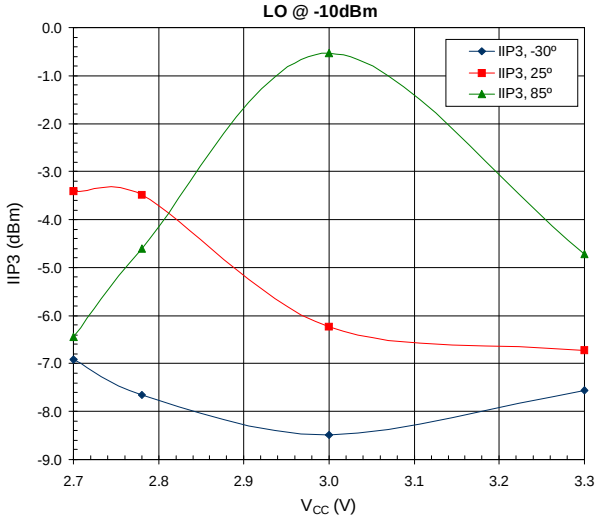
Mixer/LNA2 IF, Low Gain Mode (LNA2BYP=0), LO @ -10dBm



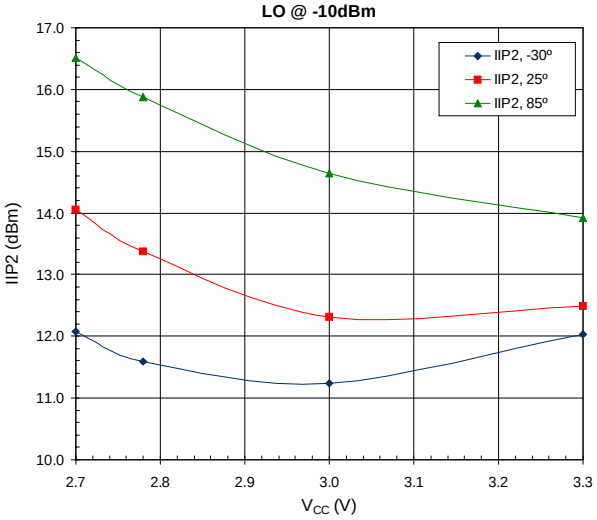
Mixer/LNA2, High Gain Mode (LNA2BYP=1), LO @ -10dBm



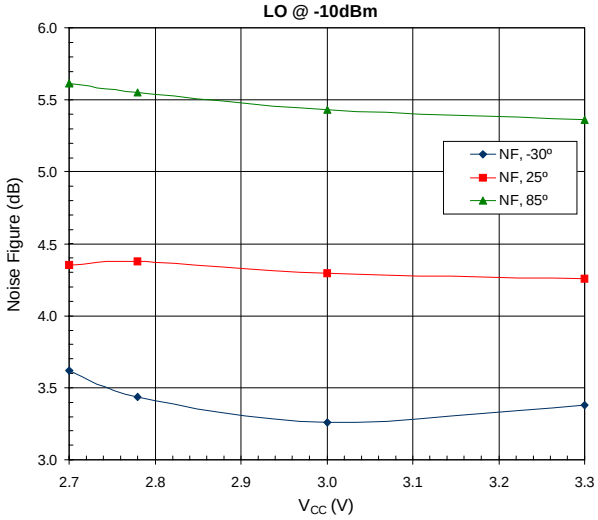
Mixer/LNA2, High Gain Mode (LNA2BYP=1), LO @ -10dBm



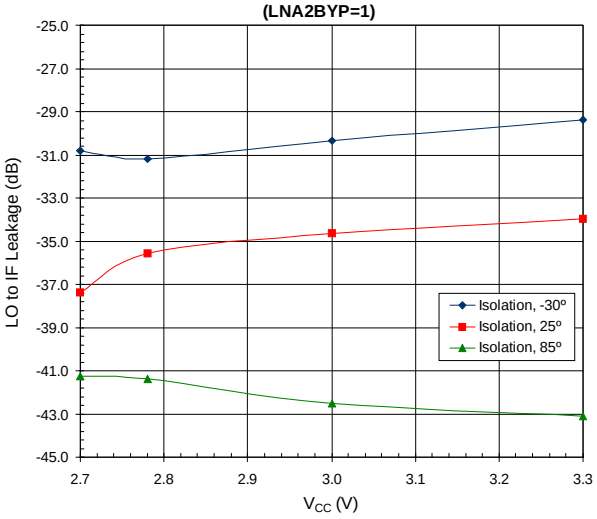
Mixer/LNA2, High Gain Mode (LNA2BYP=1), LO @ -10dBm



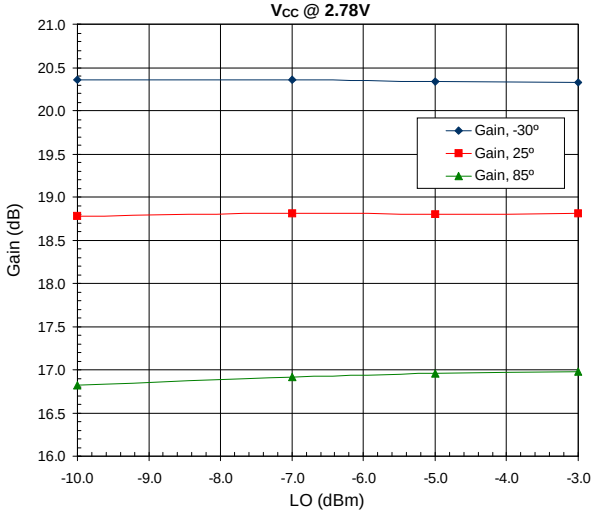
Mixer/LNA2, High Gain Mode (LNA2BYP=1), LO @ -10dBm



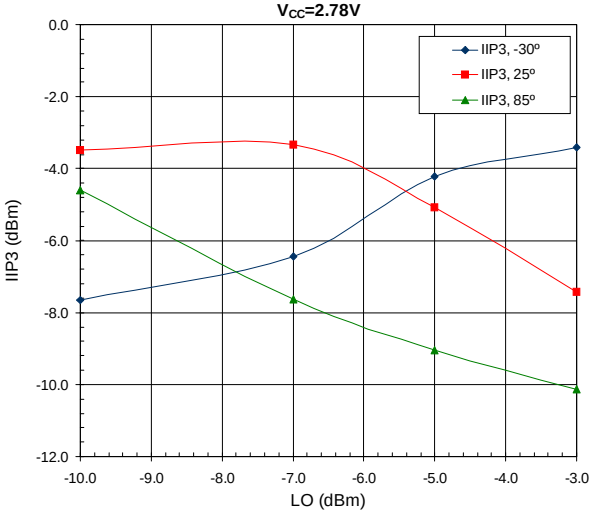
Mixer/LNA2 LO to IF Leakage (LNA2BYP=1)



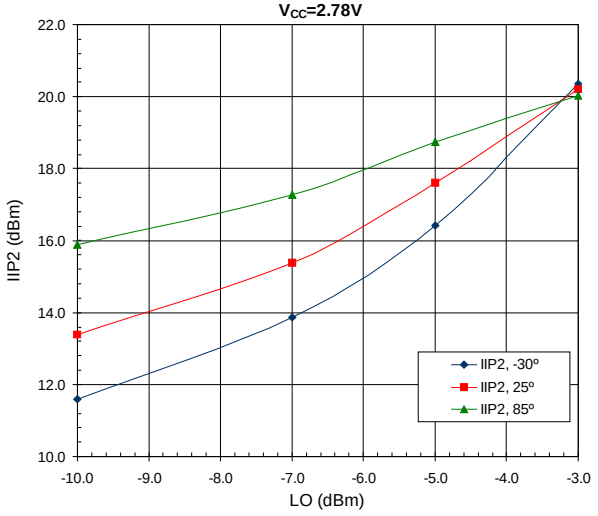
Mixer/LNA2, High Gain Mode (LNA2BYP=1), VCC @ 2.78V



Mixer/LNA2 IF, High Gain Mode (LNA2BYP=1), VCC=2.78V



Mixer/LNA2 IF, High Gain Mode (LNA2BYP=1), VCC=2.78V



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FRONT-ENDS

Low Current Configuration

External resistors can set different bias currents for LNA1 (pin 3), LNA2 (pin 4, also called the preamplifier of the mixer), and mixer (pin 17). Customers have the flexibility to choose the most suitable bias current, and therefore the performance, of the IC. The charts on the following page reflect different bias currents for the RF2469.

The currents were calculated using the following equations.

LNA1 current (R1)=Total Current (LNA1=EN=1, LNA2=0)-Total Current (EN=1, LNA1=LNA2=0)+1.6
1.6 is the bypass current of LNA1
Mixer/LNA2 current (R2)=Total Current (LNA1=0, LNA2=EN=1)-Total Current (LNA1=LNA2=0, EN=1)+1.4+10.2
1.4 is the bypass current of LNA2; 10.2 is the mixer (LO buffer included)
Mixer Only current (R5)=Total Current (EN=LNA2=1, LNA1=0)-4.5
4.5 is the bypass current of the LNA1 (1.6mA)+LNA2 high mode current (2.9mA)

RFMD chose a low current configuration of the RF2469, by using R1=3kΩ, R2=3.6kΩ, and R5=1kΩ in the evaluation board, and the following lab results over temperature were obtained.

LNA1 High Mode

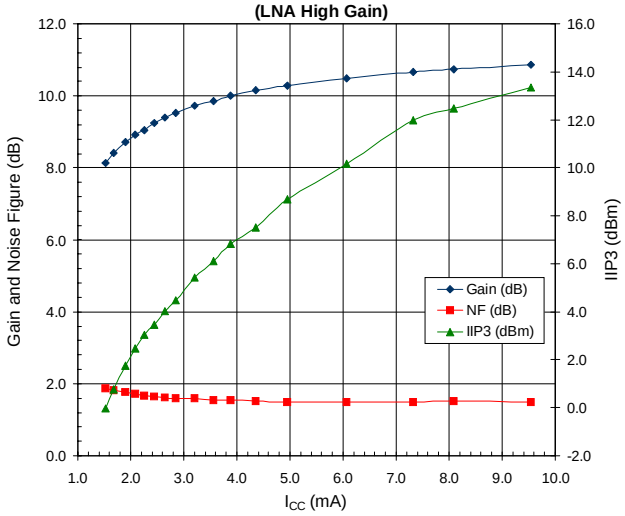
Temp (°C)	Frequency (MHz)	P_{IN} (dBm)	V_{CC} (V_{DC})	Gain (dB)	IIP3 (dBm)	Noise Figure (dB)	Total Current
-30	2140	-25	2.78	+7.97	-3.78	+1.72	+11.33
+25	2140	-25	2.78	+8.81	+2.32	+1.95	+12.36
+85	2140	-25	2.78	+9.70	+7.71	+2.37	+16.45

Total Current (mA) is when LNA1BYP=LNA2BYP2=EN=1.

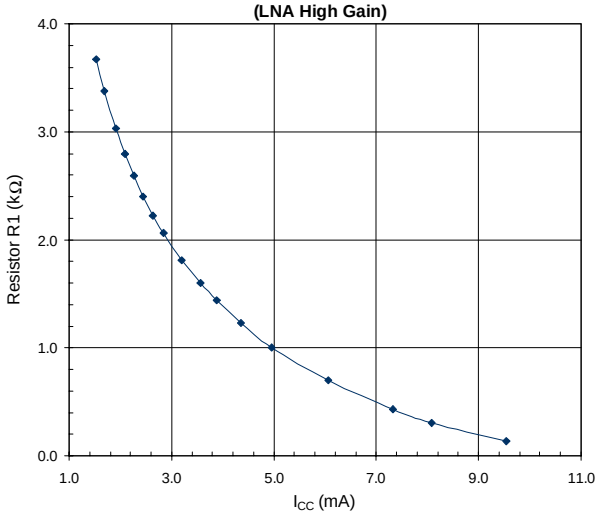
Mixer/LNA2 BYP High Mode

Temp (°C)	Frequency (MHz)	P_{IN} (dBm)	LO Frequency (MHz)	P_{IN} LO (dBm)	V_{CC} (V_{DC})	Gain (dB)	IIP3 (dBm)	Noise Figure (dB)
-30	2140	-25	2330	-10	2.78	+18.73	-8.16	+3.98
+25	2140	-25	2330	-10	2.78	+17.74	+5.13	+4.54
+85	2140	-25	2330	-10	2.78	+16.67	-3.66	+5.19

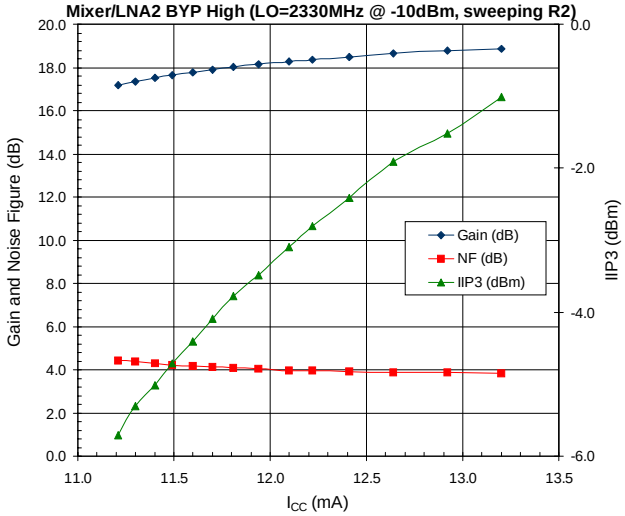
LNA Gain, Noise Figure and IIP3 versus I_{CC} - LNA1 Only
(LNA High Gain)



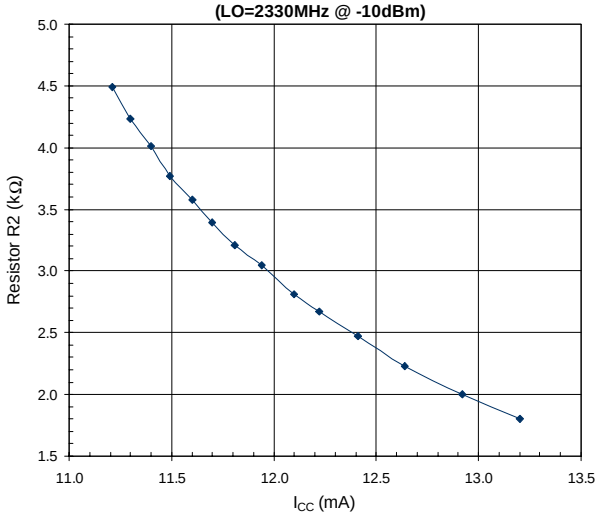
Resistor (R1) versus I_{CC} (mA) - LNA Only
(LNA High Gain)



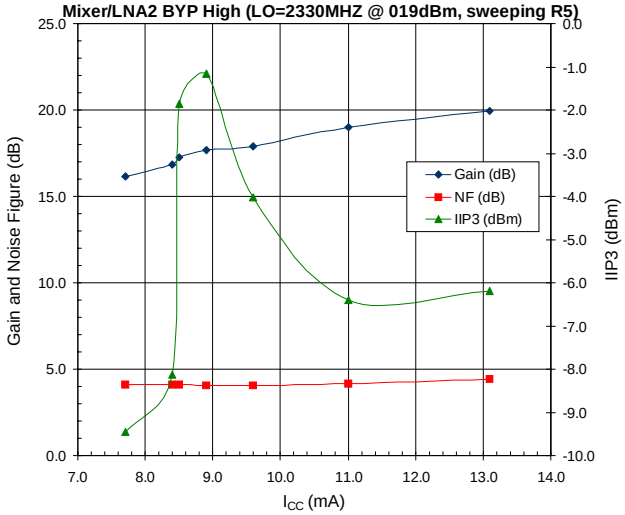
Mixer Gain, Noise Figure and IIP3 versus I_{CC} - Mixer/LNA2 BYP High (LO=2330MHz @ -10dBm, sweeping R2)



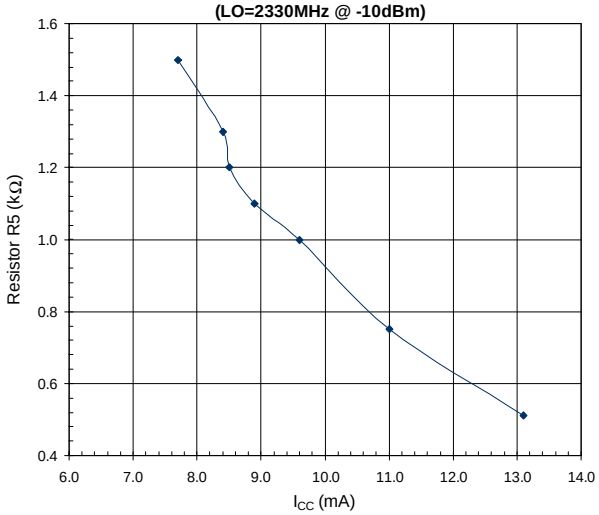
Resistor (R2) versus I_{CC} - Mixer/LNA2 BYP High
(LO=2330MHz @ -10dBm)



Mixer Gain, Noise Figure and IIP3 versus I_{CC} - Mixer/LNA2 BYP High (LO=2330MHZ @ 019dBm, sweeping R5)



Resistor (R5) versus I_{CC} - Mixer/LNA2 BYP High
(LO=2330MHz @ -10dBm)



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FRONT-ENDS