

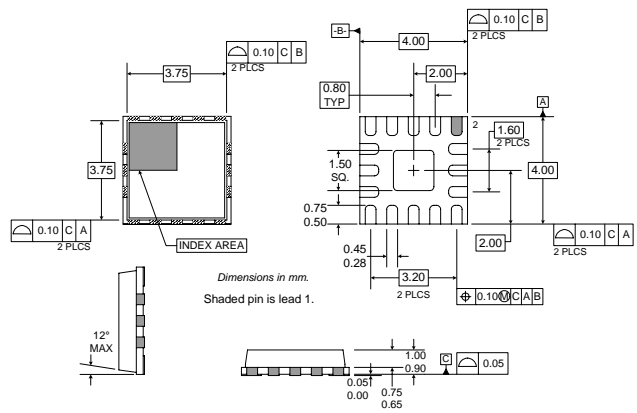
**RoHS Compliant & Pb-Free Product**

Typical Applications

- 3V CDMA/AMPS Cellular Handsets
- 3V JCDMA Cellular Handsets
- 3V CDMA2000 Cellular Handsets
- 3V TDMA/GAIT Cellular Handsets
- 3V CDMA 450MHz Band Handsets
- Portable Battery-Powered Equipment

Product Description

The RF2192 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Hetero-junction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA/AMPS and CDMA2000 handheld digital cellular equipment, spread-spectrum systems, and other applications in the 800MHz to 960MHz band. The RF2192 has a low power mode to extend battery life under low output power conditions. The device is packaged in a 16-pin, 4mmx4mm QFN.



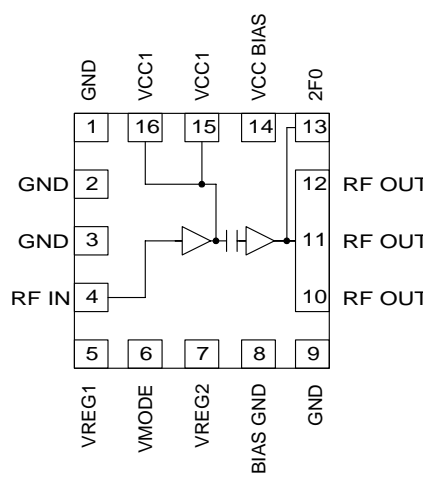
Optimum Technology Matching® Applied

- |                                     |  |                                       |
|-------------------------------------|--|---------------------------------------|
| <input type="checkbox"/> Si BJT     | <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> GaAs MESFET  |
| <input type="checkbox"/> Si Bi-CMOS | <input type="checkbox"/> SiGe HBT            | <input type="checkbox"/> Si CMOS      |
| <input type="checkbox"/> InGaP/HBT  | <input type="checkbox"/> GaN HEMT            | <input type="checkbox"/> SiGe Bi-CMOS |

Package Style: QFN, 16-Pin, 4 x 4

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 37% Linear Efficiency
- Low Power Mode
- 45 mA idle current
- 47% Peak Efficiency 31 dBm Output



Functional Block Diagram

Ordering Information

RF2192 3V 900MHz Linear Power Amplifier  
 RF2192PCBA-41X Fully Assembled Evaluation Board

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# RF2192

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V <sub>DC</sub>
Supply Voltage (P <sub>OUT</sub> ≤31dBm)	+5.2	V <sub>DC</sub>
Mode Voltage (V <sub>MODE</sub> )	+4.2	V <sub>DC</sub>
Control Voltage (V <sub>REG</sub> )	+3.0	V <sub>DC</sub>
Input RF Power	+10	dBm
Operating Case Temperature	-30 to +110	°C
Storage Temperature	-40 to +150	°C



**Caution!** ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Usable Frequency Range</b>	400		960	MHz	
<b>High Power State-US-CDMA (V<sub>MODE</sub> Low)</b>					Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> = 2.85V, V <sub>MODE</sub> =0V to 0.5V, Freq=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain	27	30		dB	
Second Harmonic		-33		dBc	
Third Harmonic		<-60		dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency		37		%	P <sub>OUT</sub> =29dBm
Adjacent Channel Power Rejection		-48	-44	dBc	ACPR @ 885kHz
		-58	-56	dBc	ACPR @ 1980kHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
Noise Power		-133	6:1	dBm/Hz	No oscillations. >-70dBc At 45MHz offset
<b>Low Power State-US-CDMA (V<sub>MODE</sub> High)</b>					Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V, V <sub>MODE</sub> =1.8V to 3V, Freq=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain	19	22		dB	
Second Harmonic		-33		dBc	
Third Harmonic		<-60		dBc	
Maximum Linear Output Power (CDMA Modulation)	16	20		dBm	
Max I <sub>CC</sub>		150		mA	P <sub>OUT</sub> =+16dBm (all currents included)
Adjacent Channel Power Rejection		-48	-46	dBc	ACPR @ 885kHz
		<-60	-58	dBc	ACPR @ 1980kHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>High Power State CDMA 2000 1x (V<sub>MODE</sub> LOW)</b>					
Frequency Range	824		849	MHz	Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V. V <sub>MODE</sub> =0V to 0.5V, Freq=824MHz to 849MHz (unless otherwise specified)
Linear Gain		29		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	26.5			dBm	
Adjacent Channel Power Rejection		-47		dBc	
		<-60		dBc	
Pilot+FCH 9600+SCHO 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	29			dBm	
Adjacent Channel Power Rejection		-47		dBc	
		<-60		dBc	
<b>Low Power State CDMA 2000 1x (V<sub>MODE</sub> HIGH)</b>					
Frequency Range	824		849	MHz	Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V. V <sub>MODE</sub> =1.8V to 3V, Freq=824MHz to 849MHz
Linear Gain		22		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	
Adjacent Channel Power Rejection		-48		dBc	
		<-85		dBc	
Efficiency		15		%	
Pilot+FCH 9600+SCHO 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	
Adjacent Channel Power Rejection		<-50		dBc	
		<-65		dBc	
<b>FM Mode</b>					
Frequency Range	824		849	MHz	Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V, V <sub>MODE</sub> =0V to 0.5V, Freq=824MHz to 849MHz (unless otherwise specified)
Gain		30		dB	
Second Harmonic		-33		dBc	
Third Harmonic		<-60		dBc	
Max CW Output Power	31	32		dBm	
Total Efficiency (AMPS mode)		47		%	
Input VSWR		2:1			
Output VSWR			10:1		
			6:1		

Note: DCCH: Dedicated Control Channel  
 FCH: Fundamental Channel  
 CCDF: Complementary Cumulative Distribution Function

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>High Power State- CDMA450 (V<sub>MODE</sub> Low)</b>					Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V, V <sub>MODE</sub> =0V to 0.5V, Freq=452MHz to 458MHz (unless otherwise specified)
Frequency Range	452		458	MHz	
Linear Gain		31		dB	
Second Harmonic		30		dBc	
Third Harmonic		-60		dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency		35		%	P <sub>OUT</sub> =29dBm
Adjacent Channel Power Rejection		-49		dBc	ACPR @ 885kHz
		-56		dBc	ACPR @ 1980kHz
Input VSWR		2:1			
Output VSWR			10:1 6:1		No damage. No oscillations. > -70dBc
<b>Low Power State- CDMA450 (V<sub>MODE</sub> High)</b>					Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V, V <sub>MODE</sub> =2.85V, Freq=452MHz to 458MHz (unless otherwise specified)
Frequency Range	452		458	MHz	
Linear Gain		23		dB	
Maximum Linear Output Power (CDMA Modulation)	16			dBm	
Max I <sub>CC</sub>		160		mA	P <sub>OUT</sub> =+16dBm (all currents included)
Adjacent Channel Power Rejection		-52		dBc	ACPR @ 885kHz
		-70		dBc	ACPR @ 1980kHz
Input VSWR		2:1			
Output VSWR			10:1 6:1		No damage. No oscillations. > -70dBc
<b>DC Supply</b>					
Supply Voltage	3.0	3.4	4.2	V	The maximum power out for V <sub>CC</sub> =3.0V is 28dBm.
Quiescent Current		160		mA	V <sub>MODE</sub> =Low
		45	70	mA	V <sub>MODE</sub> =High
V <sub>REG</sub> Current			10	mA	
V <sub>MODE</sub> Current			1	mA	
Turn On/Off Time			<40	μs	Time between V <sub>REG</sub> turned on and PA reaching full power. Turn on/off time can be reduced by lowering the bypass capacitor value on the V <sub>REG</sub> line.
Total Current (Power Down)			10	μA	V <sub>REG</sub> =Low
V <sub>REG</sub> "Low" Voltage	0		0.5	V	
V <sub>REG</sub> "High" Voltage	2.75	2.85	2.95	V	
V <sub>MODE</sub> "Low" Voltage	0		0.5	V	
V <sub>MODE</sub> "High" Voltage	1.8	2.85	3.0	V	

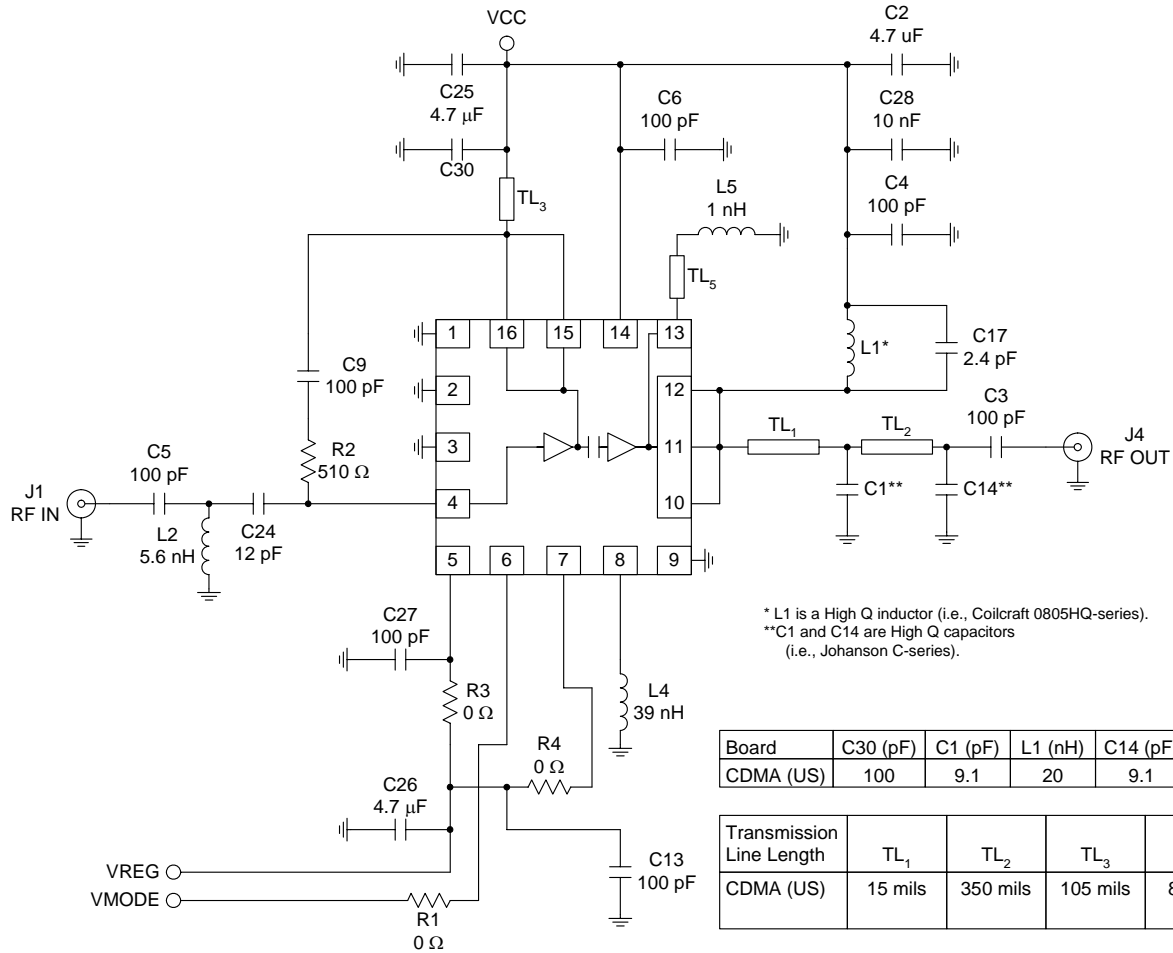
Pin	Function	Description	Interface Schematic
1	<b>GND</b>	Ground connection.	
2	<b>GND</b>	Ground connection.	
3	<b>GND</b>	Ground connection.	
4	<b>RF IN</b>	RF input. An external 100pF series capacitor is required as a DC block. In addition, shunt inductor and series capacitor are required to provide 2:1 VSWR.	
5	<b>VREG1</b>	Power Down control for first stage. Regulated voltage supply for amplifier bias. In Power Down mode, both $V_{REG}$ and $V_{MODE}$ need to be LOW (<0.5V).	
6	<b>VMODE</b>	For nominal operation (High Power Mode), $V_{MODE}$ is set LOW. When set HIGH, the driver and final stage are dynamically scaled to reduce the device size and as a result to reduce the idle current.	
7	<b>VREG2</b>	Power Down control for the second stage. Regulated voltage supply for amplifier bias. In Power Down mode, both $V_{REG}$ and $V_{MODE}$ need to be LOW (<0.5V).	
8	<b>BIAS GND</b>	Bias circuitry ground. See application schematic.	
9	<b>GND</b>	Ground connection.	
10	<b>RF OUT</b>	RF output and power supply for final stage. This is the unmatched collector output of the second stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 824MHz to 849MHz. It is important to select an inductor with very low DC resistance with a 1 A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
11	<b>RF OUT</b>	Same as pin 10.	See pin 10.
12	<b>RF OUT</b>	Same as pin 10.	
13	<b>2FO</b>	Harmonic trap. This pin connects to the RF output but is used for providing a low impedance to the second harmonic of the operating frequency. An inductor or transmission line resonating with an on chip capacitor at 2fo is required at this pin.	
14	<b>VCC BIAS</b>	Power supply for bias circuitry. A 100pF high frequency bypass capacitor is recommended.	
15	<b>VCC1</b>	Power supply for first stage.	
16	<b>VCC1</b>	Same as Pin 15.	
<b>Pkg Base</b>	<b>GND</b>	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Note: This schematic is a preliminary schematic. This 450MHz band CDMA tune is done by modifying the existing 800MHz band CDMA evaluation board.

# RF2192

## Evaluation Board Schematic US-CDMA

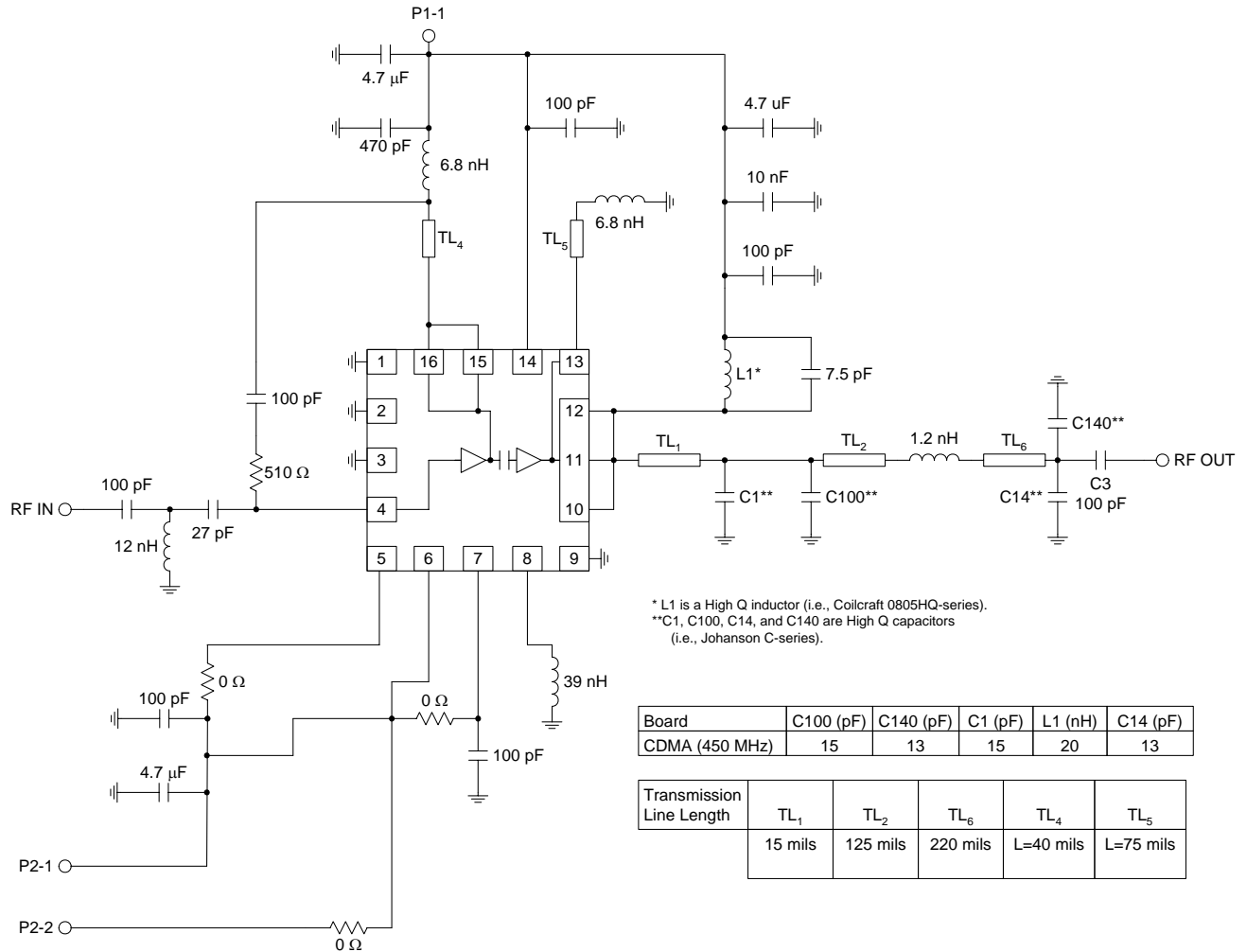
(Download [Bill of Materials](http://www.rfmd.com) from [www.rfmd.com](http://www.rfmd.com).)



Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (US)	100	9.1	20	9.1

Transmission Line Length	TL <sub>1</sub>	TL <sub>2</sub>	TL <sub>3</sub>	TL <sub>5</sub>
CDMA (US)	15 mils	350 mils	105 mils	85 mils

## Application Schematic CDMA-450MHz Band







## PCB Design Requirements

### PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

### PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

### PCB Metal Land Pattern

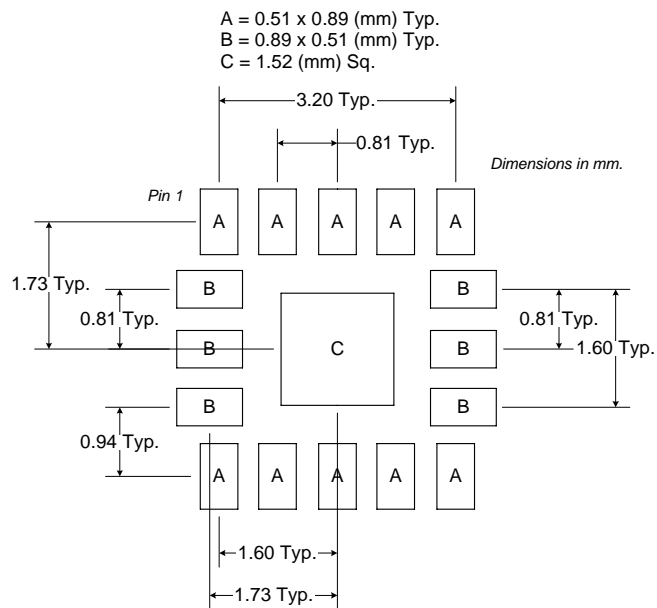
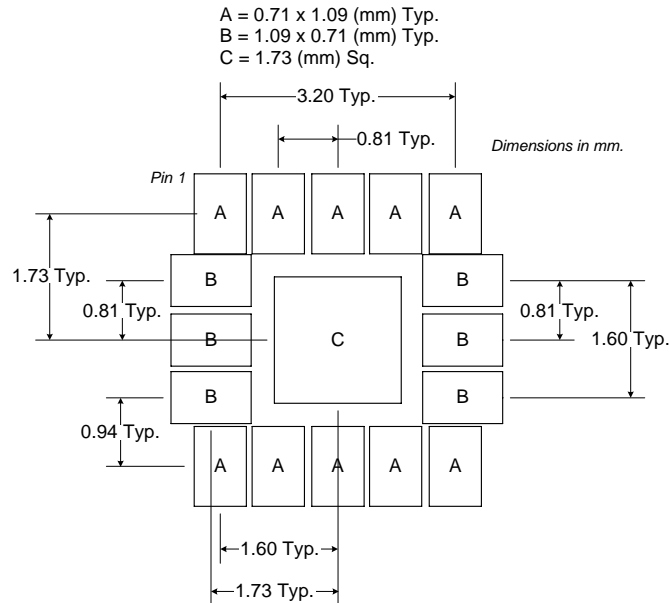


Figure 1. PCB Metal Land Pattern (Top View)

## PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB Metal Land Pattern with a 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.



**Figure 2. PCB Solder Mask (Top View)**

## Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.