CONEXANT™

RF105

900 MHz Digital Spread Spectrum Transceiver

The RF105, a fully integrated transceiver device, provides the transmit, receive, and frequency synthesis functions for Digital Spread Spectrum (DSS) systems operating in the 902–928 MHz Industrial, Scientific, and Medical (ISM) band. It implements a direct conversion architecture and Time Division Duplexing (TDD) of the transmit and receive signals to minimize circuit complexity.

The receive path of the RF105 provides complete RF-to-baseband In-Phase and Quadrature (I/Q) demodulation, including a Low Noise Amplifier (LNA), double-balanced quadrature mixers, fully integrated channel selection filters, and baseband variable-gain amplifiers. The transmit path is a variable-gain direct conversion modulator. These paths are shown in Figure 1.

A 902–928 MHz frequency synthesizer with on-chip VCO and resonator provides the LO frequency for both transmit and receive modes.

The RF105 features low-voltage operation (2.7–4.5 V) for low power consumption. The RF105, combined with Conexant's RF106 power amplifier, forms a complete system solution for a direct conversion 900 MHz DSS radio that is fully compliant with FCC Part 15 regulations in the ISM band.

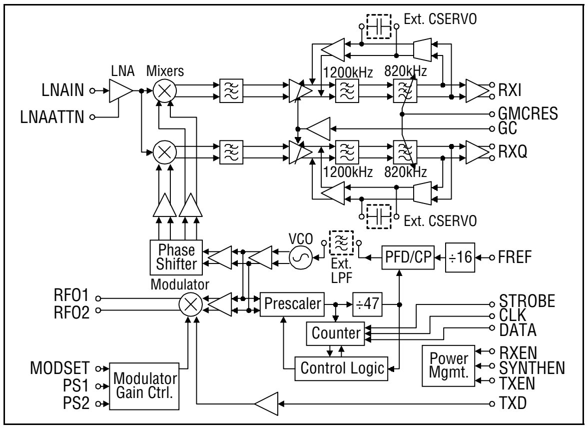


Figure 1. RF105 Block Diagram

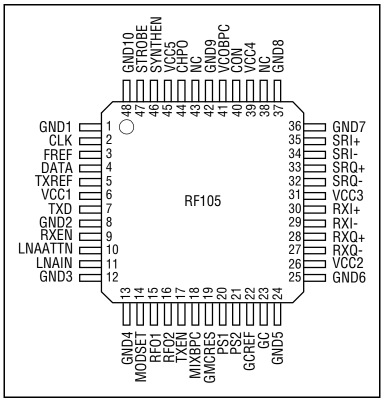


Figure 2. RF105 Pin Signals – 48 Pin TQFP

Features

- Complete 900 MHz ISM band transceiver with fully integrated synthesizer and VCO including resonator
- Low power dissipation
- Fast settling from standby mode to active mode
- Separate enable lines for transmit, receive, and synthesizer
- 41 programmable channels with 600 kHz channel spacing
- 3-battery cell operation (2.7–4.5 V)
- 48-pin TQFP package (see Figure 2)

Receiver

- LNA/Quadrature mixer from RF down to baseband
- Selectable LNA gain
- Fully integrated channel selection filter with adjustable bandwidth
- Receiver baseband amplifier with variable gain
- Differential receiver baseband outputs

Transmitter

- Variable gain modulator
- Double-balanced mixer for baseband-to-RF modulation
- Differential RF outputs

Applications

- DSS cordless telephone
- Direct sequence spread spectrum systems
- Frequency hopping spread spectrum systems
- Wireless LANs
- Wireless modems
- Wireless security
- Inventory control systems

Technical Description

Baseband Filter Bandwidth

The receive baseband filters have a bandpass characteristic. The low-pass cutoff is determined by the GmC filters and is set by the R_{gmc} resistor connected to pin 19.

The GmC filter has a 3-pole Butterworth response and is preceded by a 4-pole Butterworth Sallen & Key low-pass filter with a fixed cutoff frequency of 1.2 MHz. The fixed filters are designed to attenuate out-of-band blocking signals propagating through the receive path.

The baseband high-pass cutoff is set by the bandwidth of the DC servo loop, which in turn is set by the value of the C_{servo} capacitors connected between pins 32 and 33, and pins 34 and 35. The DC servo loop nulls out the DC offset in the receive baseband path. It is designed to be tolerant of the C_{servo} Equivalent Series Resistance (ESR), so that common surface mount capacitors are suitable.

The baseband high-pass cutoff frequency should be set much lower than the low-pass cutoff frequency, or else the servo loop will become unstable.

The optimum receive bandwidth values are:
f_{LPF} = 820 kHz, R_{gmc} = 875 Ω
f_{HPF} = 20 kHz, C_{servo} = 0.082 μF

RF Output

The transmit RF outputs from the RF105 are differential and matched to 100 Ω differential. If a single-ended connection is required, the unused output must be suitably terminated by a 50 Ω resistor (see Figure 4). The transmit output power is determined by the output power control inputs, PS1 (pin 20) and PS2 (pin 21), and by the value of R_{mod} (connected to pin 14). R_{mod} sets the bias current into the modulator, which is then multiplied by a factor set by the state of PS1 and PS2. PS1 and PS2 input programming is described in the Transmitter section of Table 3.

The characteristic of the output Peak Envelope Power (PEP) versus R_{mod} is shown in Figure 3 for a sinusoidal 120 mV peak-to-peak input signal and for high power mode (PS1 = 0, PS2 = 0). For R_{mod} equal to 1.2 kΩ, the typical RF105 output power is approximately –8 dBm in high-power mode. This provides approximately 20 dBm of transmit power when used with Conexant's RF106 (29 dB gain PA).

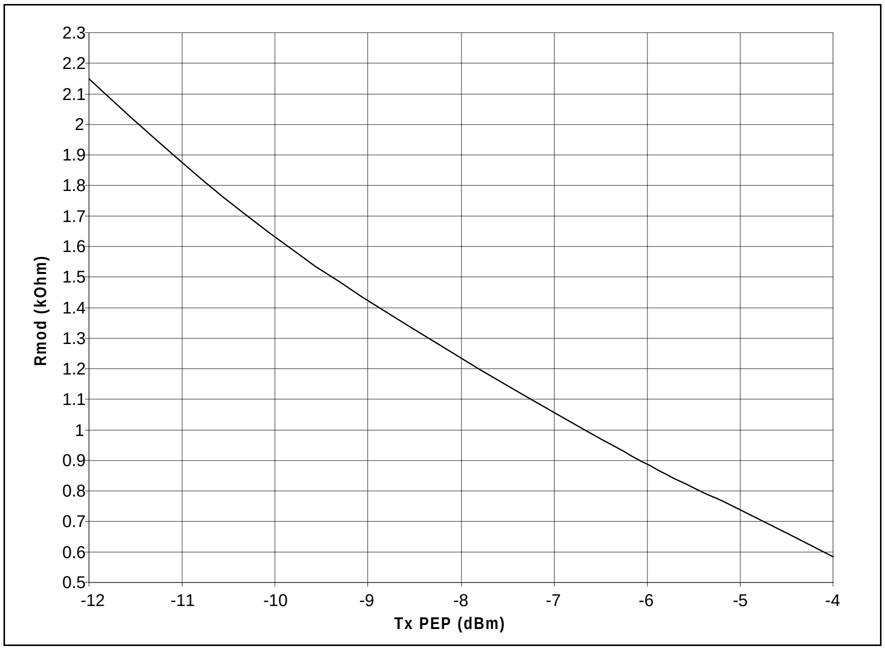


Figure 3. Tx PEP vs Rmod
(Txd signal = 120 mVpp, 300 kHz sinusoid, Vcc = 3.0V)

Recommendations on Layout and Implementation

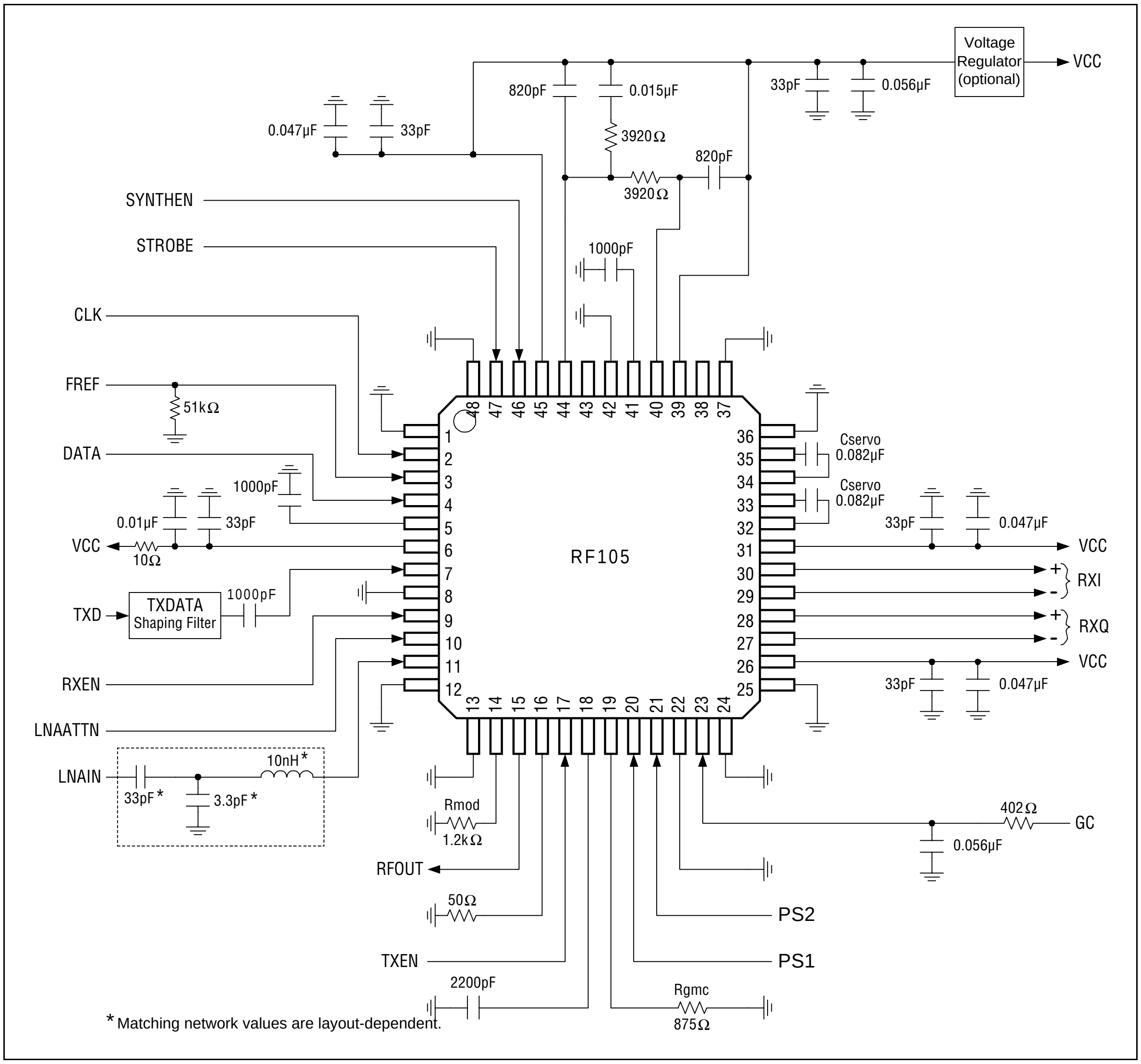
A typical applications schematic is shown in Figure 4. All Vcc pins should be decoupled as close to the supply pin as possible, preferably right at the input pins.

All ground pins should have minimum trace inductance to ground. If a ground plane cannot be provided right at the pins, the vias to the ground plane should be placed as close to the pins as possible. There should be one via for each ground pin. If the ground plane is at the bottom layer, it is recommended to have two vias in parallel for each ground pin.

VCC1 (pin 6), VCC2 (pin 26), and VCC3 (pin 31) should be connected to the common Vcc supply through individual decoupling networks.

ESD Sensitivity

The RF105 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper Electrostatic Discharge (ESD) precautions.



*Matching network values are layout-dependent.

Figure 4. Typical Applications Diagram – RF105

Synthesizer Programming

The synthesizer is programmed with a half-duplex 3-wire serial interface. The three signals are DATA, CLK, and STROBE. Each rising edge of the CLK signal shifts one bit of the data into the shift register and control register. When the STROBE input is toggled from low to high, the data latched in the shift register is transferred to the programmable counter. Six bits are shifted into the synthesizer for programming. The data format is as follows:

MSB					**LSB**
S6	S5	S4	S3	S2	S1

The timing relationship is shown in Figure 6. The values of the programming bits, S1 to S6, for the programmable counter are defined in Table 1.

Channel Selection

Using a 9.6 MHz reference frequency, the Phase Locked Loop (PLL) synthesizer can generate frequencies from 903 MHz (Channel 1) to 927 MHz (Channel 41) at a channel spacing of 600 kHz. The LO frequency (F_{LO}) is calculated by the following equation:

$$F_{LO} = (F_{REF}/R) \times [(M \times N) + A]$$

where:

F_{REF} is 9.6 MHz (reference oscillator)
R is 16 (reference divider)
M is 32/33 (prescaler)
N is 47 (fixed counter)
A is 1 to 41 (programmable counter)

Examples:

(9.6 MHz / 16) × (32 × 47 + 1) = 903 MHz
(9.6 MHz / 16) × (32 × 47 + 41) = 927 MHz

Synthesizer Loop Filter

The VCO for the synthesizer is designed on-chip with the varactor referenced to VCC. Therefore, ***the loop filter components will need to be tied to VCC4*** (pin 39) instead of ground. A typical loop filter design is shown below in Figure 5. The loop bandwidth is approximately 5 kHz with a nominal phase margin of 45 degrees.

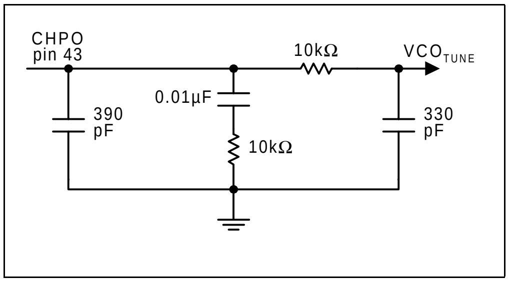
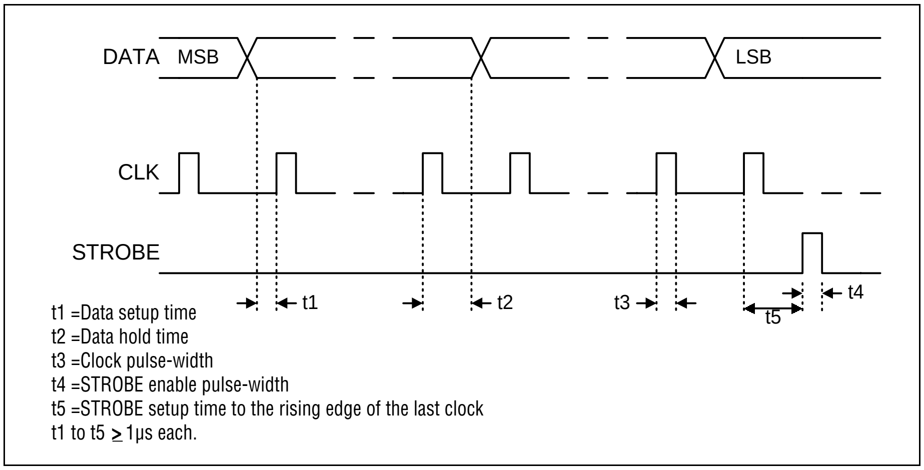


Figure 5. Loop Filter



t1 =Data setup time
t2 =Data hold time
t3 =Clock pulse-width
t4 =STROBE enable pulse-width
t5 =STROBE setup time to the rising edge of the last clock
t1 to t5 ≥ 1µs each.

Figure 6. Timing Diagram

Table 1. Programmable Counter Data Input

DSS Telephone Channel No. *	Synthesizer Channel No. (A)	Frequency (MHz)	S6	S5	S4	S3	S2	S1
–	1	903.0	0	0	0	0	0	0
–	2	903.6	0	0	0	0	0	1
1	3	904.2	0	0	0	0	1	0
2	4	904.8	0	0	0	0	1	1
–	5	905.4	0	0	0	1	0	0
3	6	906.0	0	0	0	1	0	1
–	7	906.6	0	0	0	1	1	0
4	8	907.2	0	0	0	1	1	1
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
17	34	922.8	1	0	0	0	0	1
–	35	923.4	1	0	0	0	1	0
18	36	924.0	1	0	0	0	1	1
–	37	924.6	1	0	0	1	0	0
19	38	925.2	1	0	0	1	0	1
20	39	925.8	1	0	0	1	1	0
–	40	926.4	1	0	0	1	1	1
–	41	927.0	1	0	1	0	0	0

* DSS telephone channel numbers are applicable when RF105 is used with Conexant's Hummingbird chip set. Channel spacing = 1.2 MHz between adjacent channels from channel 2 through channel 19; channel spacing = 600 kHz between channels 1–2 and between channels 19–20.

Interface Description

Table 2. Pin Description

Pin	Name	Description	Pin	Name	Description
1	GND1	Ground	25	GND6	Ground
2	CLK	Synthesizer programming clock input	26	VCC2	Supply for baseband outputs
3	FREF	Reference frequency input for synthesizer	27	RX Q–	Q channel baseband differential outputs
4	DATA	Synthesizer programming data input	28	RX Q+	
5	TXREF	Reference for TX data input, ac-coupled to ground	29	RX I–	I channel baseband differential outputs
6	VCC1	Supply for LNA and RX mixer	30	RX I+	
7	TXD	Baseband TX data input	31	VCC3	Supply for baseband circuits
8	GND2	LNA emitter ground	32	SR Q–	Q channel DC offset cancellation servo external capacitor connections
9	RXEN	Receive enable	33	SR Q+	
10	LNAATTN	LNA attenuation control 0 = high-gain mode, 1 = low-gain mode	34	SR I–	I channel DC offset cancellation servo external capacitor connections
11	LNAIN	LNA RF input	35	SR I+	
12	GND3	Ground	36	GND7	Ground
13	GND4	Ground	37	GND8	Ground
14	MODSET	Input to set TX modulator gain	38	NC	No connect
15	RFO1	Differential TX RF output	39	VCC4	Supply for VCO
16	RFO2	Differential TX RF output, inverse polarity	40	CON	VCO control input
17	TXEN	Transmit enable	41	VCOBPC	Bias bypass capacitor for VCO bias
18	MIXBPC	Bypass capacitor for RX mixer bias	42	GND9	Ground for VCO
19	GMCRES	Resistor to set cutoff frequency of channel selection filter	43	NC	No connect
20	PS1	Modulator power control input (see Table 3)	44	CHPO	Charge pump output
21	PS2	Modulator power control input (see Table 3)	45	VCC5	Supply for synthesizer
22	GCREF	Reference for gain control input connected to ground	46	SYNTHEN	Synthesizer enable
23	GC	Baseband variable gain amplifier control input	47	STROBE	Synthesizer programming load enable
24	GND5	Ground	48	GND10	Ground

Specifications

Table 3. Electrical Specifications (1 of 3)

Note: T_A = 25 °C, V_{CC} = 3.6 V, f_{LO}= 915 MHz

Parameter	Min	Typical	Max	Units
RECEIVER SECTION				
RX voltage gain: LNA high-gain mode (LNAATTN = 0)				
GC = 1.3 V	99.5	105	109.5	dB
GC = 1.6 V	77.5	82.5	87.5	
GC = 1.9 V	37.5	38	42.5	
LNA gain step		19		
RX gain variation vs. frequency 902 MHz < f_{LO} < 928 MHz		0.5	1	dB
RX SSB noise figure: High-gain mode, GC = 1.3 V		6.5	8.0	dB
RX input IP3: LNA high-gain mode, GC = 1.9 V		–36		dBm
LNA low-gain mode, GC = 1.9 V		–15		
RX input P1dB: LNA high-gain mode (LNAATTN = 0)				
GC = 1.3 V	–101	–97		dBm
GC = 1.6 V	–79	–74		
GC = 1.9 V	–47	–43		
LNA low-gain mode (LNAATTN = 1)				
GC = 1.9 V		–22		
AM demodulation suppression at LNA input to mixer output	60			dB
LO power at LNAIN		–80		dBm
I/Q phase imbalance		±1	±5	deg
I/Q amplitude imbalance		0.5	3	dB
Input high voltage, LNAATTN, RXEN VIH	1.9			V
Input low voltage, LNAATTN, RXEN VIL			0.75	
Input high current, RXEN IIH		125	200	µA
Input low current , RXEN IIL	–25			
Input high current, LNAATTN IIH			60	µA
Input low current, LNAATTN IIL	–25			
GC I_{IN}	–500		500	µA
Baseband amplifier gain control range (GC = 1.3V – 1.9V)	60	67	75	dB
GC input voltage range	1.2	1.6	2.0	V
Baseband amplifier gain control sensitivity GC = 1.3–1.9 V			0.17	dB/mV
GC = 1.3 V		0.04		
GC = 1.6 V		0.14		
GC = 1.9 V		0.13		
RX P1dB @ 3.9 MHz offset LNA high gain, GC = 1.9 V		–45		dBm
LNA low gain, GC = 1.9 V		–14		
Baseband output load capacitance		20	50	pF
Baseband LPF 3 dB bandwidth (Rgmc = 875 Ω)	0.65	0.82	0.97	MHz
Baseband selectivity @ 3.9 MHz	60	70		dB
Baseband differential output VCM	1.0		VDD – 1.0	V
Baseband output DC offset			25	mV
RXI, RXQ DC and gain settle time (note 1) from initial RXEN input at TDD rate > 250 Hz		50	100	µs
Baseband HPF 3dB bandwidth (servo capacitors = 82 nF)	13	20	29	kHz
Baseband output voltage swing (peak differential)		300		mV
Baseband output SNR (GC = 1.9 V)		24		dB

Table 3. Electrical Specifications (2 of 3)

Parameter	Min	Typical	Max	Units
FREQUENCY SYNTHESIZER SECTION				
LO frequency range	903		927	MHz
PLL VCO center frequency @ control voltage of 1.1 V		915		MHz
PLL VCO sensitivity	35	50	75	MHz/V
LO settling time Δf = 10 MHz, settle to f_{FINAL} ± 5 kHz, 5 kHz LFBW			2	msec
LO phase noise 100 kHz offset		–100	–95	dBc/Hz
1 MHz offset			–115	
VCO (varactor) input leakage		0.01		µA
Input reference frequency, FREF		9.6		MHz
Frequency step, F_S		600		kHz
Comparison frequency (600 kHz) spur level			–60	dBc
RMS phase jitter, 25–700 kHz			5	degrees RMS
Input high voltage, STROBE, CLK, DATA, SYNTHEN VIH	1.9			V
Input low voltage, STROBE, CLK, DATA, SYNTHEN VIL			0.75	
Input high current, STROBE, CLK, DATA IIH			40	µA
Input low current, STROBE, CLK, DATA IIL	–25			
Input high current, SYNTHEN IIH			100	µA
Input low current, SYNTHEN IIL	–25			
Input high voltage, FREF VIH	1.9			V
Input low voltage, FREF VIL			0.75	
Input high current, FREF IIH			100	µA
Input low current, FREF IIL	–25			
Charge-pump output current		±225		µA
Output short-circuit current CHPO			1.0	mA
TRANSMITTER SECTION				
Gain variation vs. frequency 902 MHz < f_{LO} < 928 MHz		0.5	1.0	dB
Peak-envelope output power (single-ended): (note 2)				
High power mode (PS1 = 0, PS2 = 0)	–11	–8	–6.5	dBm
Medium power mode (PS1 = 0, PS2 = 1)		–19		
Low power mode (PS1 = 1, PS2 = 0)		–27.5		
Undefined mode (PS1 = 1, PS2 = 1)		not used		
IM3 (TXD input signal 2 tones each 60 mVpp)	–30	–40		dBc
Output VSWR for unconditional stability			10:1	
LO suppression	–15	–25		dBc
TXD input impedance		10		kΩ
TXD input peak-to-peak sine wave for target output peak-envelope power		120		mV_{pp}
TXD input bandwidth		80		MHz
TXD to RF settle time to within spec value from TXEN			50	µs
TX DC offset			2	mV
Input high voltage, PS1, PS2, TXEN VIH	1.9			V
Input low voltage, PS1, PS2, TXEN VIL			0.75	
Input high current, PS1, PS2, TXEN IIH			60	µA
Input low current, PS1, PS2, TXEN IIL	–25			
Input high current TXEN IIH			100	µA
Input low current TXEN IIL	–25			

Table 3. Electrical Specifications (3 of 3)

Parameter	Min	Typical	Max	Units
POWER SUPPLY				
Total supply current:				
RX mode (RXEN, SYNTHEN = 1)	48	65	78	mA
TX mode (TXEN, SYNTHEN = 1) (note 2)				
High power mode	25	33	41	mA
Medium power mode	20	28	35	mA
Low power mode	20	27	34	mA
Synth mode (SYNTHEN = 1)	15	21	25	mA
Sleep mode (RXEN, TXEN, SYNTHEN, LNAATTN = 0)		5	100	µA
Power supply range (note 3)	2.7	3.6	4.5	VDC

Notes:
1. Gain settled to within 90% of final value, DC settled to within 10% of desired signal's final value.
2. TXD input signal 120 mVpp, 300 kHz sinusoidal, Rmod = 1.2 kΩ.
3. The specifications in Table 3 are guaranteed at a supply voltage (Vcc) of 3.6 V. At Vcc below 3.0 V, the RF105 is functional, but the system performance may be degraded.

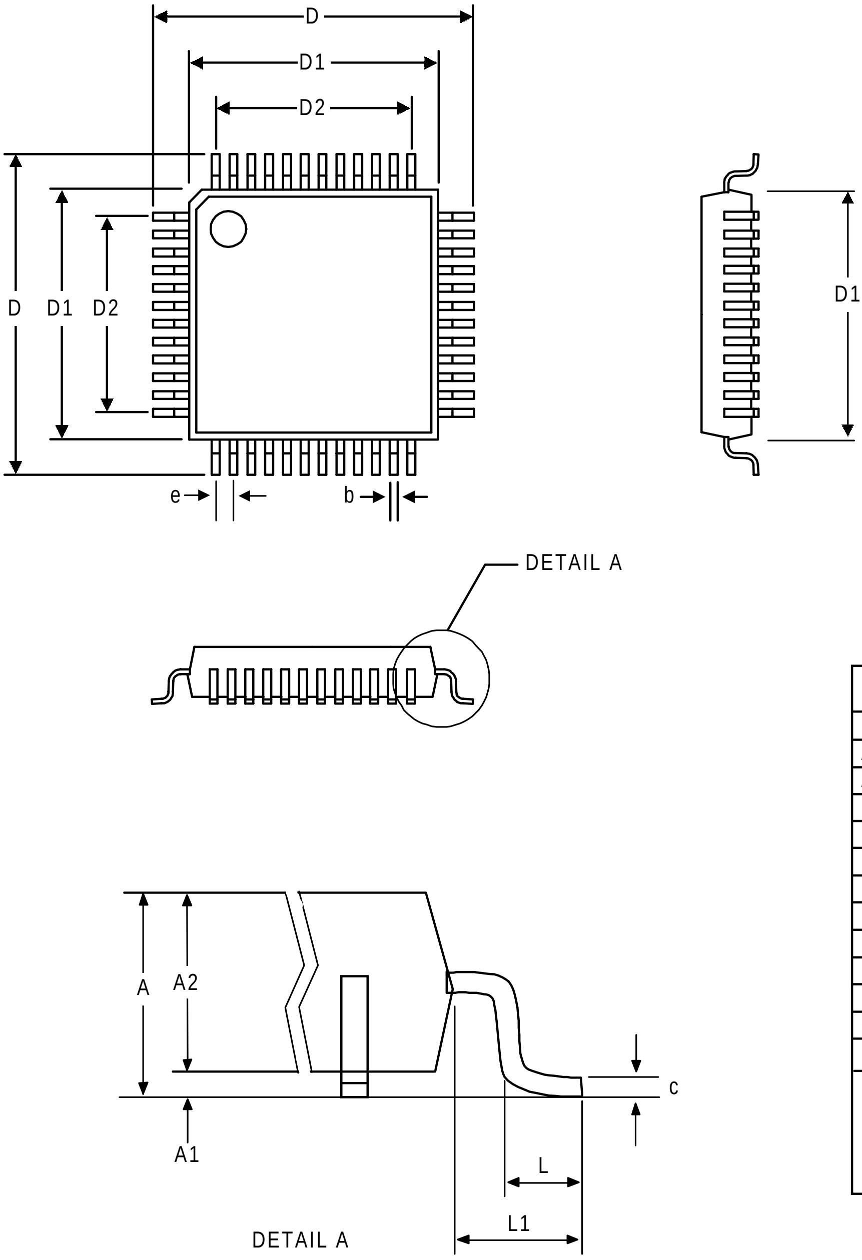
Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply voltage (Vcc) (note 1)	–0.3	5.0	V
Input voltage range (note 1)	–0.3	VCC	V
Power dissipation		500	mW
LNA input power		+5	dBm
Operating temperature range	–10	70	°C
Storage temperature	–40	125	°C

Notes:
1. Voltages are referenced to GND.

Device Dimensions

RF105 device dimensions are shown below in Figure 7.



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0060
A2	1.35	1.45	0.0528	0.0571
D	8.85	9.15	0.3484	0.3602
D1	6.95	7.05	0.2736	0.2776
D2	5.5 REF		0.2165 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.500 REF		0.0197 REF	
b	0.220 REF		0.0087 REF	
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.10 MAX		0.0039 MAX	
Ref: 48-PIN TQFP (GP00-D283)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may contain round-off errors.

Figure 7. RF105 Device Dimensions

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