

RD15LD74AP, RD15LD74ANP, RD15LD74AT

8-bit D-type Flip-Flop Driver (with Clear)

REJ03D0894-0300

Rev.3.00

Feb 29, 2008

Description

RD15LD74AP, RD15LD74ANP, RD15LD74AT have eight D-type flip-flop drivers and high voltage NMOS output (open drain output) in a 20 pin package. Each bit, there are a common clear and clock input. The input signal is output with the rising edge of clock signals. The voltage of maximum 15 V can be impressed to the drain-source voltage.

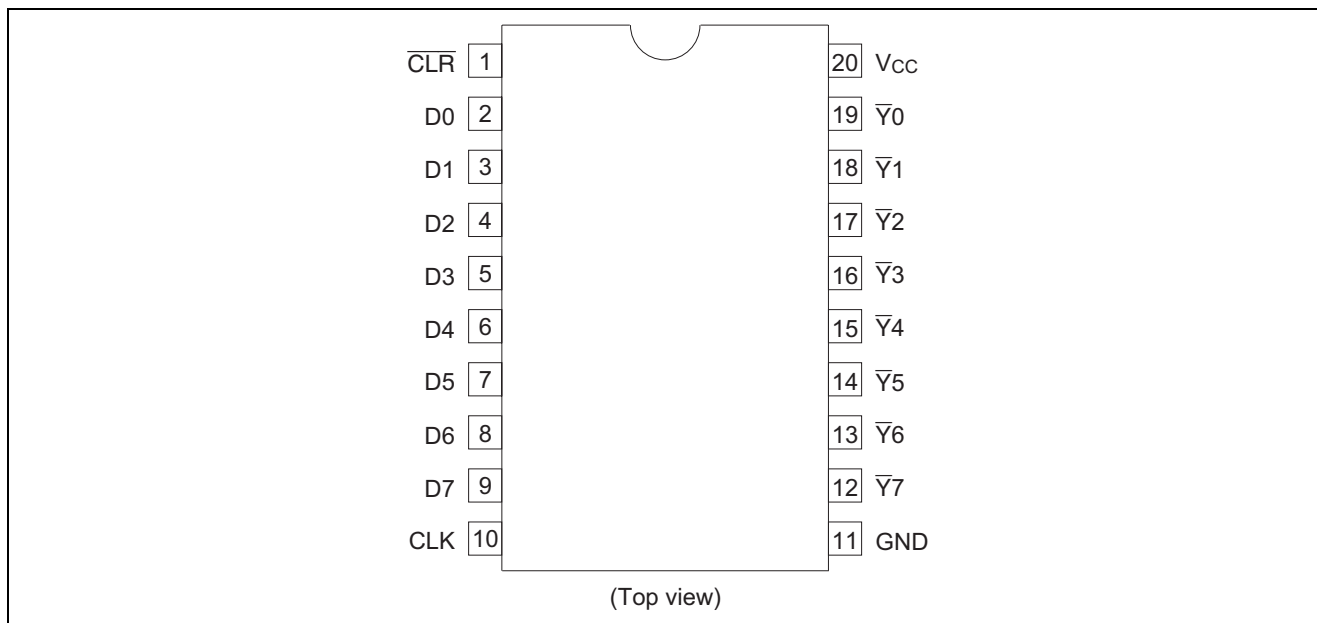
Features

- Application of amusement equipment.
- Output voltage : $V_{DS}(\text{max}) = 15 \text{ V}$
- Output current : $I_{DS}(\text{max}) = 200 \text{ mA}$ (par pin)
- Supply voltage range : 3.0 to 5.5 V
- Operating temperature range : -20 to $+85 \text{ }^\circ\text{C}$
- Quiescent supply current : $5 \mu\text{A}$ max.
- Low input current : $1 \mu\text{A}$ max.
- Ordering Information

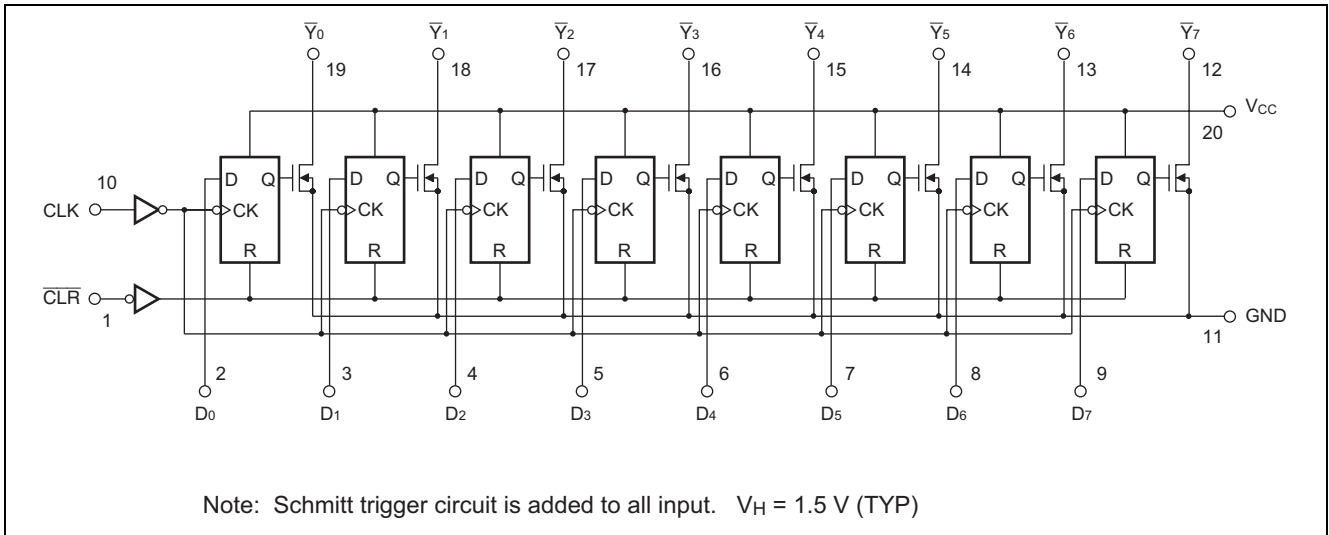
| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Packing Abbreviation (Quantity) | Surface Treatment |
|---------------|--------------|------------------------------|----------------------|---------------------------------|-------------------|
| RD15LD74APT0 | SDIP-20 pin | PRDP0020BA-A (20P4B) | P | T (1,125 pcs/box) | 0 (Sn-Cu) |
| RD15LD74ANPT0 | DILP-20 pin | PRDP0020AC-B (DP-20NEV) | P | T (1,000 pcs/box) | 0 (Ni/Pd/Au) |
| RD15LD74ATH0 | TSSOP-20 pin | PTSP0020JB-A (TTP-20DAV) | T | H (2,000 pcs/reel) | 0 (Ni/Pd/Au) |

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Logic Diagram



Function Table

| Inputs | | | Output |
|-------------------------|--------------|---|-----------------------|
| $\overline{\text{CLR}}$ | CLK | D | $\overline{\text{Y}}$ |
| L | X | X | Z |
| H | \uparrow | L | Z |
| H | \uparrow | H | L |
| H | L | X | Y_0 |
| H | \downarrow | X | Y_0 |

H : High level

L : Low level

X : Immaterial

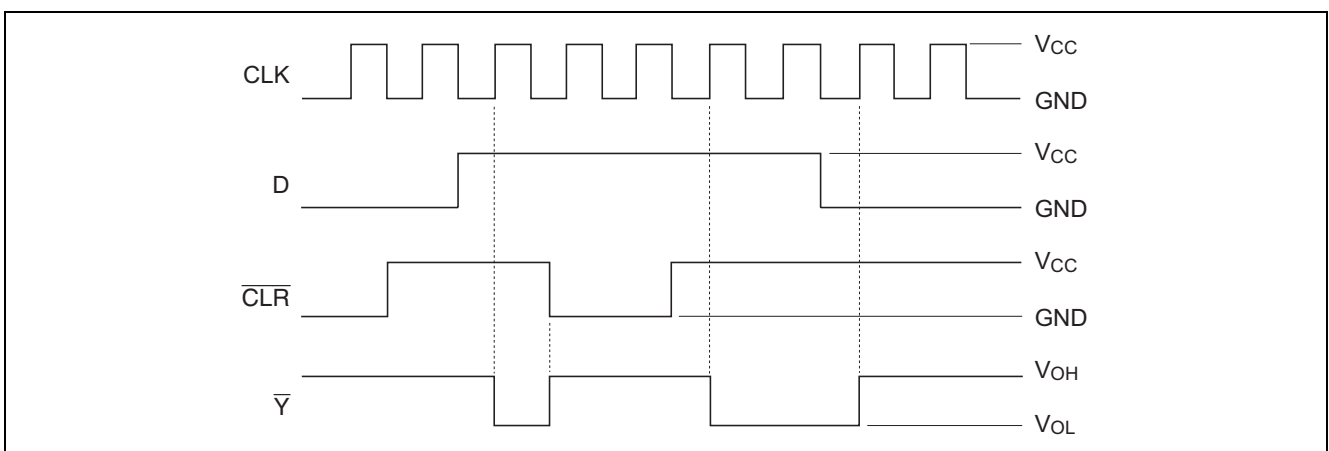
Z : High Impedance

\uparrow : Low to High transition

\downarrow : High to Low transition

Y_0 : Level of $\overline{\text{Y}}$ before the indicated steady input conditions were established.

Timing Figure



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---|----------|------------------|------|---|
| Supply voltage | V_{CC} | 6.5 | V | |
| Input voltage | V_I | -0.5 to V_{CC} | V | |
| Output voltage | V_{DS} | -0.5 to 15 | V | Output : "Z" (off) |
| Output current | I_{DS} | 200 | mA | Output : "on", Current of one circuit |
| Maximum power dissipation ^{*1} | P_T | 1.47 | W | SDIP DILP TSSOP Ta = 25°C Base implementation |
| | | 1.38 | | |
| | | 0.76 | | |
| Storage temperature | Tstg | -55 to +125 | °C | |

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

- The maximum package power dissipation was calculated using a junction temperature of 150°C

Recommended Operating Conditions

| Item | Symbol | Ratings | | Unit | Conditions |
|---|------------|---------|----------|------|--|
| Supply voltage | V_{CC} | 3.0 | 5.5 | V | |
| Input voltage | V_I | 0 | V_{CC} | V | |
| Output voltage | V_{DS} | 0 | 15 | V | Output "Z" (off) |
| Output current (Current of an one circuit, when eight circuit operation) | I_{DS} | 0 | 200 | mA | SDIP Duty cycle ≤ 60% Duty cycle ≤ 100% |
| | | 0 | 150 | | |
| | | 0 | 200 | mA | DILP Duty cycle ≤ 55% Duty cycle ≤ 100% |
| | | 0 | 140 | | |
| | | 0 | 200 | mA | TSSOP Duty cycle ≤ 25% Duty cycle ≤ 100% |
| | | 0 | 105 | | |
| Input rise / fall time | t_r, t_f | 0 | 500 | ns | $V_{CC} = 3.0\text{ V}, 4.5\text{ V}$ |
| Operating temperature | Ta | -20 | 85 | °C | |

Note: Unused or floating inputs must be held high or low.

Electrical Characteristics

(Ta = -20 to +85°C)

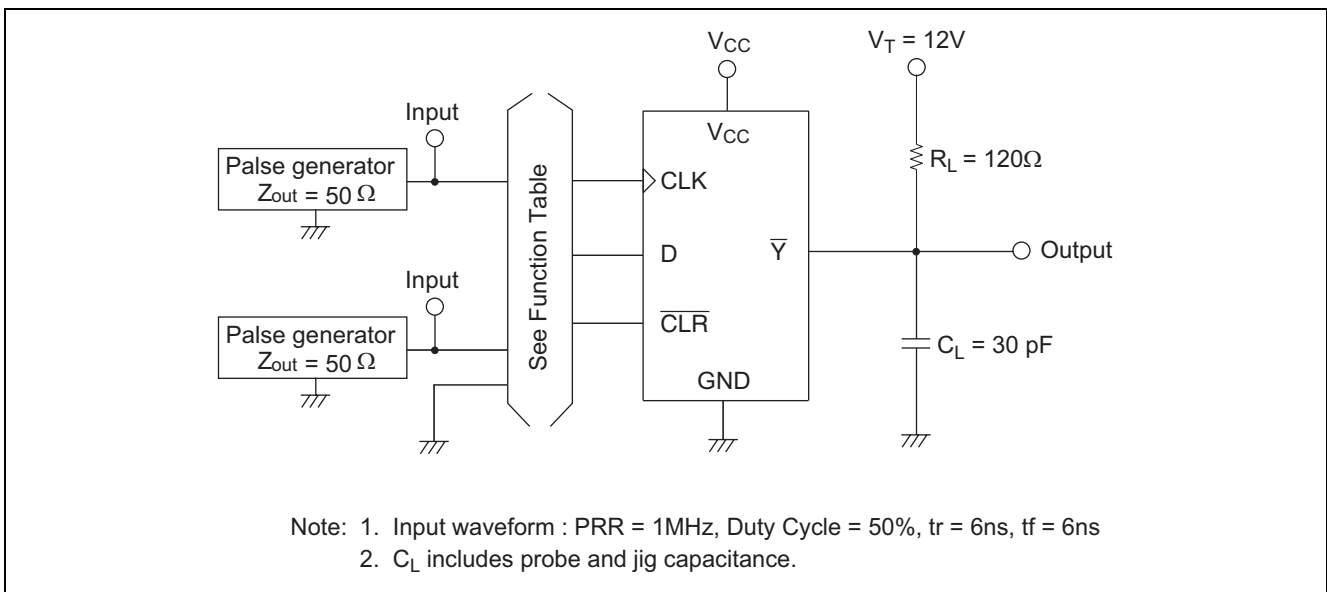
| Item | Symbol | VCC (V) | Ratings | | | Unit | Conditions |
|-------------------------------|----------|------------|----------------------|-------|----------------------|------|---|
| | | | Min | Typ | Max | | |
| Input voltage | V_{IH} | 3.0 to 3.6 | $V_{CC} \times 0.84$ | — | — | V | |
| | | 4.5 to 5.5 | $V_{CC} \times 0.76$ | — | — | | |
| | V_{IL} | 3.0 to 3.6 | — | — | $V_{CC} \times 0.16$ | V | |
| | | 4.5 to 5.5 | — | — | $V_{CC} \times 0.24$ | | |
| Output voltage | V_{DS} | 3.0 to 3.6 | — | 0.30 | 0.45 | V | $I_{DS} = 100\text{ mA}$ |
| | | 4.5 to 5.5 | — | 0.25 | 0.38 | | |
| | | 3.0 to 3.6 | — | 0.60 | 0.90 | | $I_{DS} = 200\text{ mA}$ |
| | | 4.5 to 5.5 | — | 0.51 | 0.77 | | |
| "H" input current | I_{IH} | 3.0 to 5.5 | — | 0.005 | 1.0 | μA | $V_I = V_{CC}$ |
| "L" input current | I_{IL} | 3.0 to 5.5 | — | 0.005 | -1.0 | μA | $V_I = 0\text{ V}$ |
| Quiescent supply current | I_{CC} | 5.5 | — | 0.005 | 5.0 | μA | All output "Z" (off) $V_I = V_{CC}$ or GND |
| | | 5.5 | — | 0.005 | 5.0 | | All output "on", $V_I = V_{CC}$ or GND |
| Output off state leak current | I_{DS} | 5.0 | — | 0.002 | 5.0 | μA | $V_{DS} = 12\text{ V}$ |
| Output on resister | R_{DS} | 4.5 | — | 2.5 | 3.8 | Ω | $I_{DS} = 100\text{ mA}$ |

Switching Characteristics

($T_a = -20$ to $+85^\circ\text{C}$, $C_L = 30$ pF, $t_r = t_f = 6$ ns)

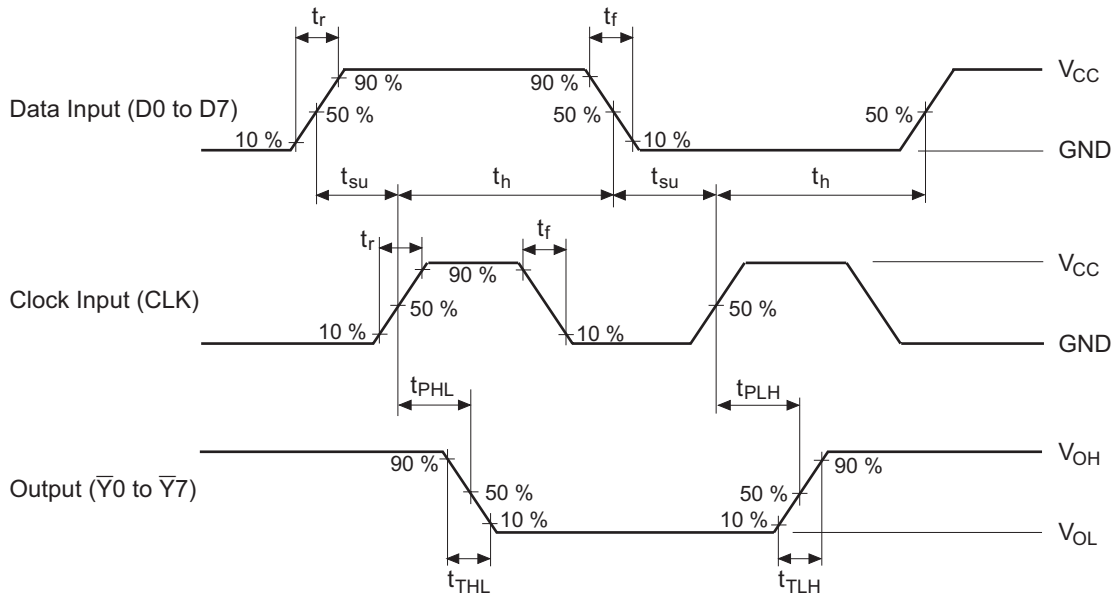
| Item | Symbol | VCC (V) | Ratings | | Unit | Conditions |
|-------------------------|------------|---------------|---------|-----|------|---|
| | | | Min | Max | | |
| Maximum clock frequency | f_{\max} | 3.3 ± 0.3 | — | 15 | MHz | |
| | | 5.0 ± 0.5 | — | 20 | | |
| Propagation delay time | t_{PLH} | 3.3 ± 0.3 | 1.0 | 65 | ns | CLK, $\overline{\text{CLR}}$ to $\overline{\text{Y}}$ |
| | | 5.0 ± 0.5 | 1.0 | 50 | | |
| Propagation delay time | t_{PHL} | 3.3 ± 0.3 | 1.0 | 60 | ns | CLK to $\overline{\text{Y}}$ |
| | | 5.0 ± 0.5 | 1.0 | 45 | | |
| Setup time | t_{su} | 3.3 ± 0.3 | 25 | — | ns | D to CLK |
| | | 5.0 ± 0.5 | 20 | — | | |
| Hold time | t_h | 3.3 ± 0.3 | 3 | — | ns | CLK to D |
| | | 5.0 ± 0.5 | 3 | — | | |
| Pulse width | t_w | 3.3 ± 0.3 | 50 | — | ns | CLK, $\overline{\text{CLR}}$ |
| | | 5.0 ± 0.5 | 40 | — | | |
| Output rise time | t_{TLH} | 3.3 ± 0.3 | — | 30 | ns | $\overline{\text{Y}}$ |
| | | 5.0 ± 0.5 | — | 20 | | |
| Output fall time | t_{THL} | 3.3 ± 0.3 | — | 10 | ns | $\overline{\text{Y}}$ |
| | | 5.0 ± 0.5 | — | 5 | | |

Test Circuit

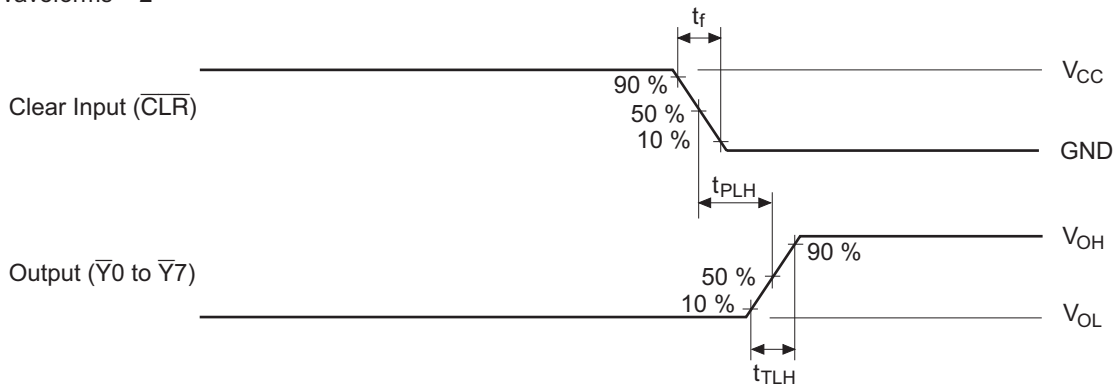


Waveforms

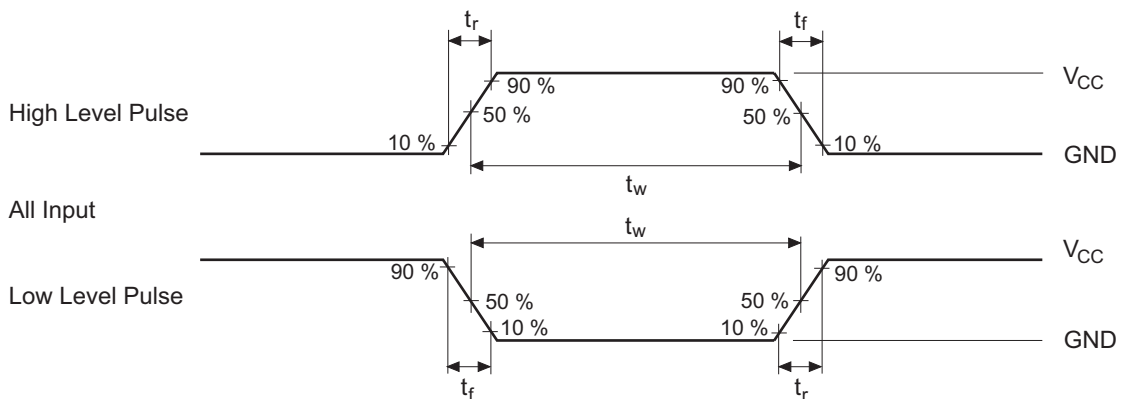
• Waveforms – 1



• Waveforms – 2

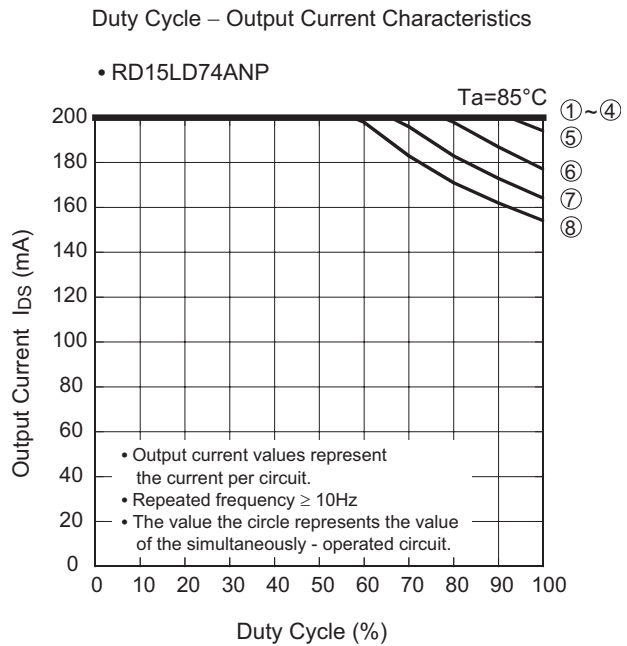
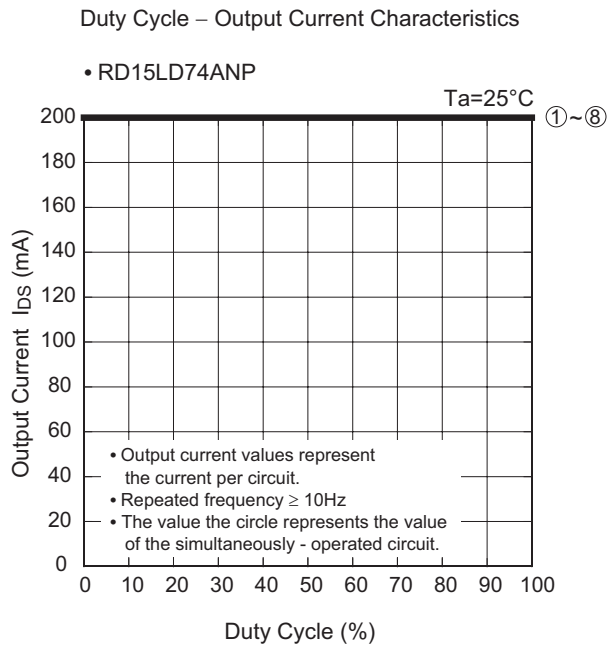
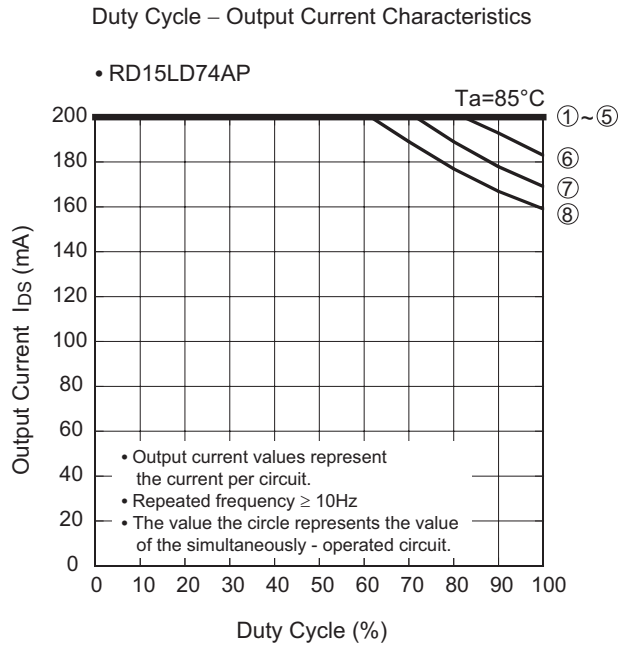
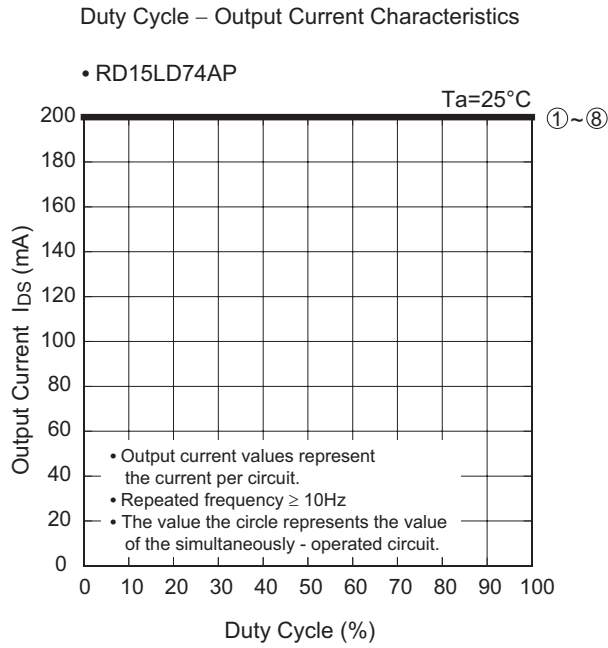


• Waveforms – 3

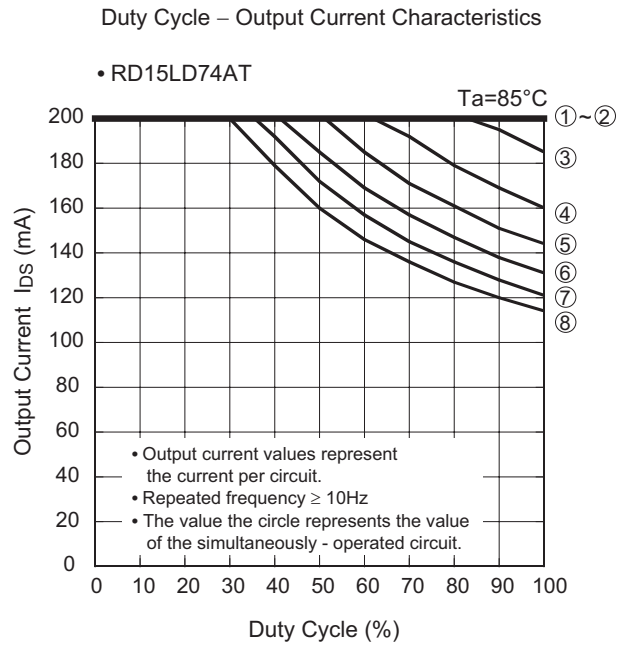
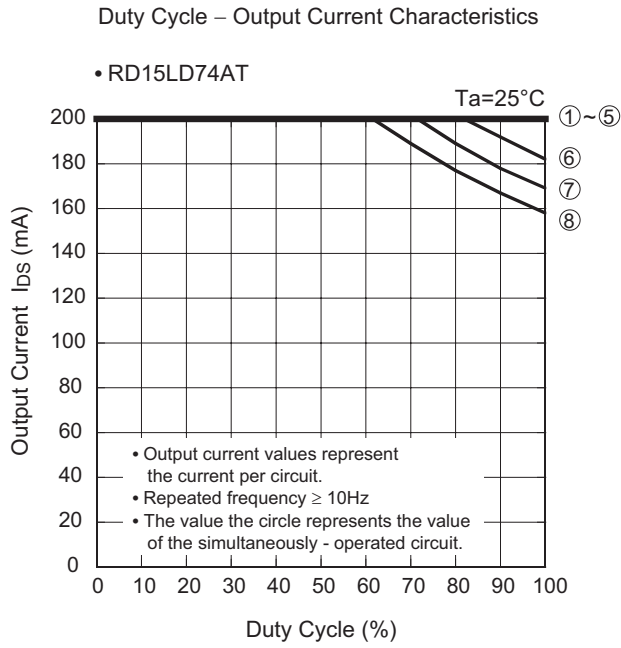


- Notes: 1. Input waveform : PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns
 2. The input and output is measured one at a time with one transition per measurement.

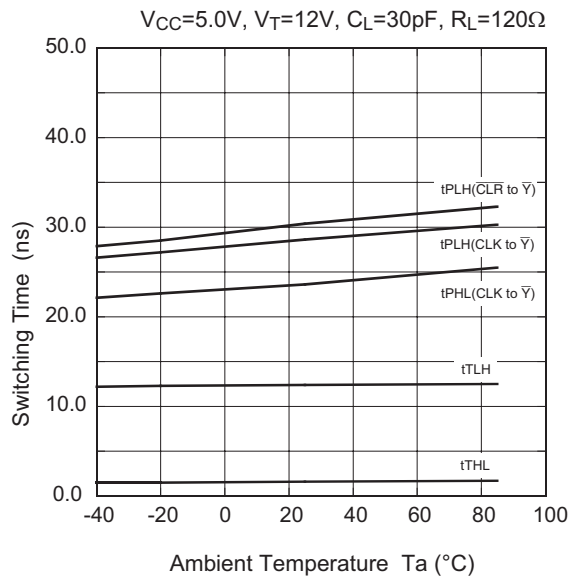
Application Data



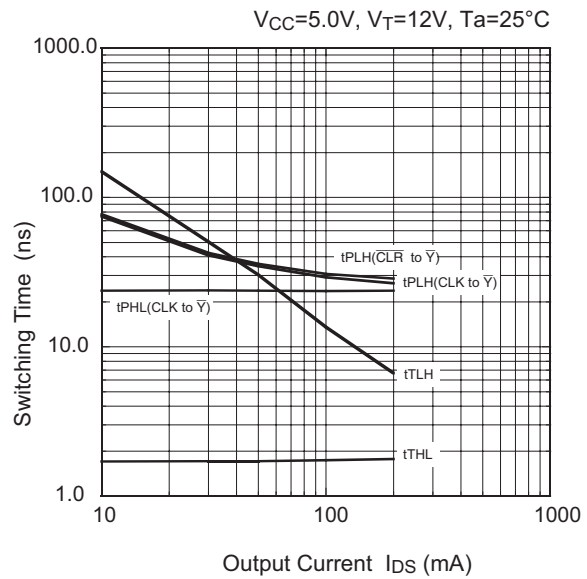
Application Data



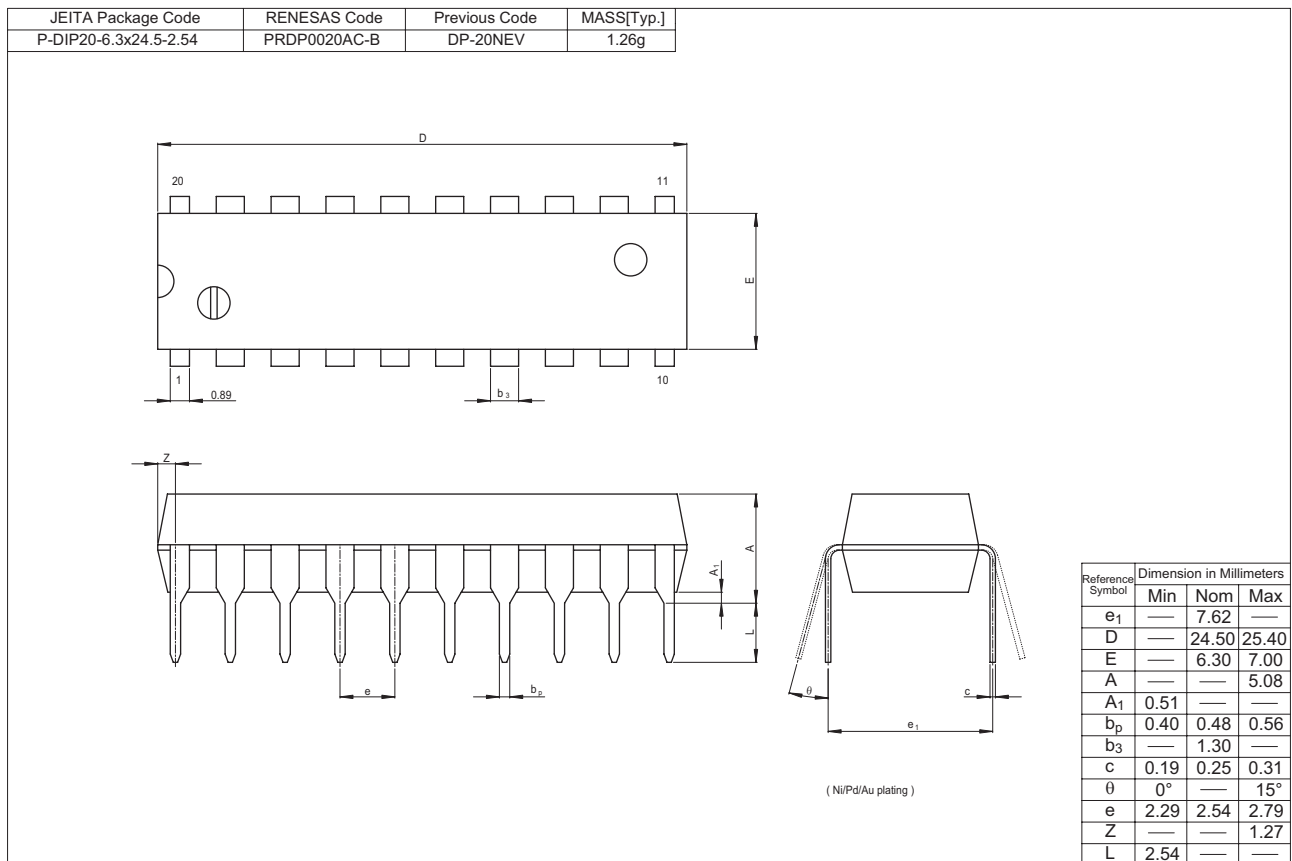
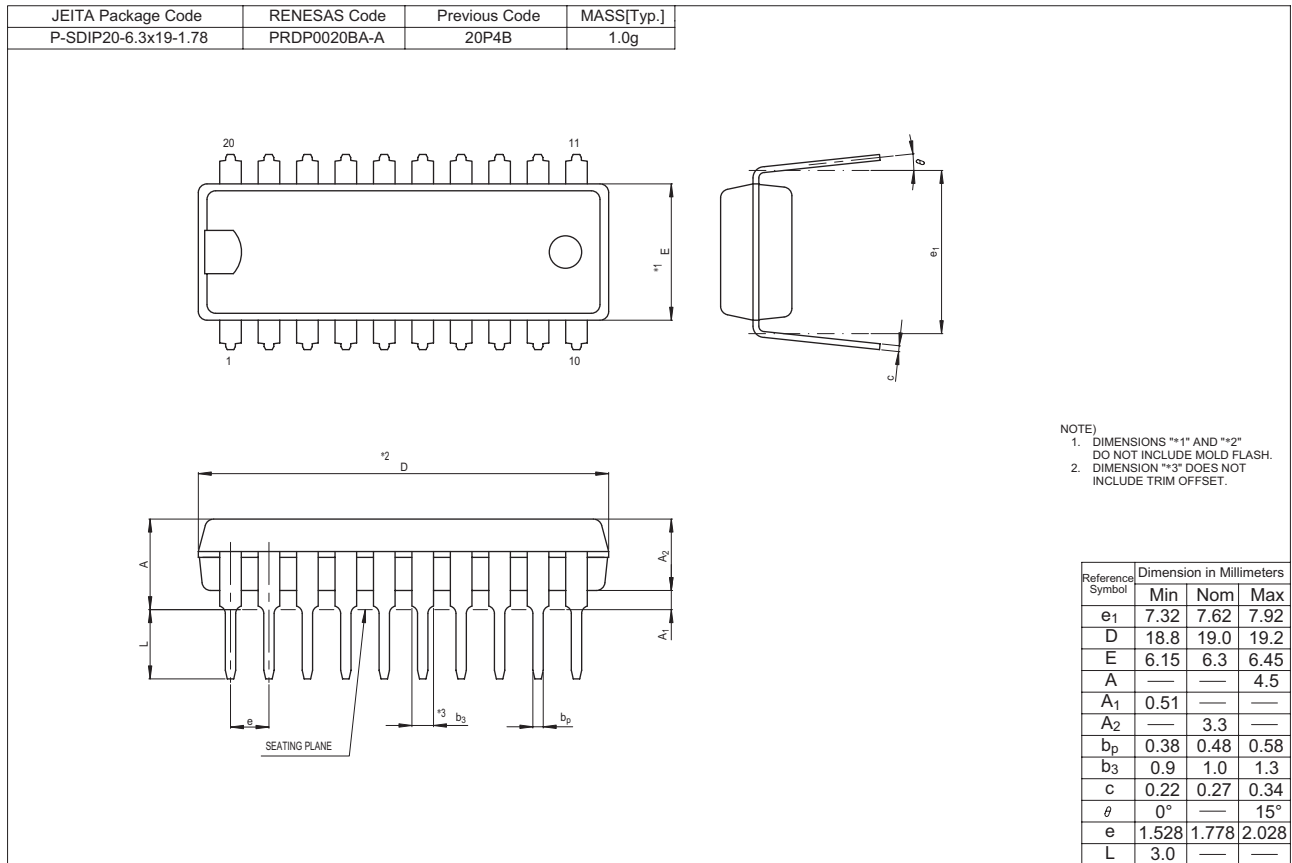
Switching Time – Ambient Temperature Characteristics



Switching Time – Output Current Characteristics

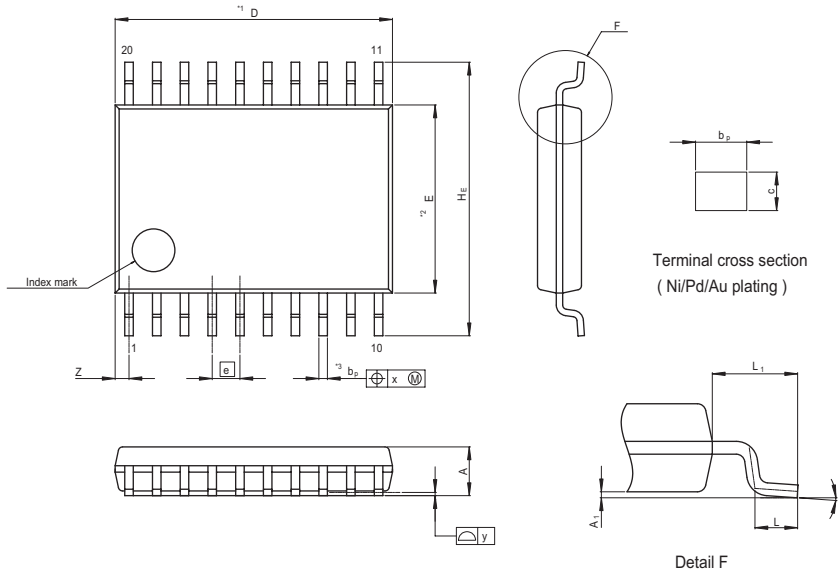


Package Dimensions



RD15LD74AP, RD15LD74ANP, RD15LD74AT

| | | | |
|------------------------|--------------|---------------|------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
| P-TSSOP20-4.4x6.5-0.65 | PTSP0020JB-A | TTP-20DAV | 0.07g |



NOTE)
 1. DIMENSIONS**1 (Nom)**AND**2*
 DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION**3*DOES NOT
 INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min | Nom | Max |
| D | — | 6.50 | 6.80 |
| E | — | 4.40 | — |
| A ₂ | — | — | — |
| A ₁ | 0.03 | 0.07 | 0.10 |
| A | — | — | 1.10 |
| b _p | 0.15 | 0.20 | 0.25 |
| b ₁ | — | — | — |
| c | 0.10 | 0.15 | 0.20 |
| c ₁ | — | — | — |
| θ | 0° | — | 8° |
| H _E | 6.20 | 6.40 | 6.60 |
| [e] | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| Z | — | — | 0.65 |
| L | 0.4 | 0.5 | 0.6 |
| L ₁ | — | 1.0 | — |

Notes:

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