SIEMENS

Preliminary

SAB 82284 Clock Generator and Ready Interface for SAB 80286 Processors

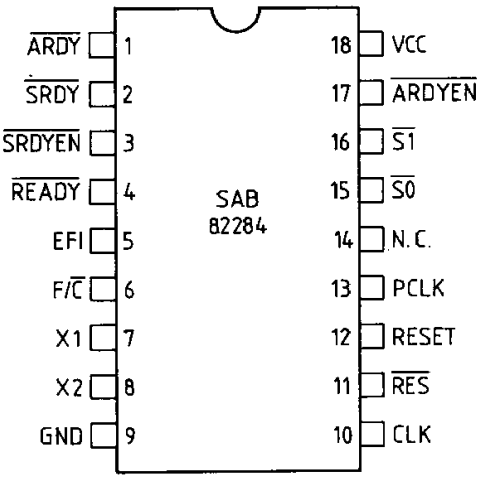
SAB 82284 up to 16 MHz

- Generates system clock for SAB 80286 processors
- Uses crystal or TTL signal for frequency source
- Provides local $\overline{\text{READY}}$ and multimaster system bus $\overline{\text{READY}}$ synchronization

SAB 82284-1 up to 20 MHz

- 18-pin package
- Single +5 V power supply
- Generates system reset output from Schmitt-trigger input

Pin Configuration



Pin Names

CLK	System Clock
F/$\overline{\text{C}}$	Frequency/Crystal Select
X1, X2	Crystal In
EFI	External Frequency In
PCLK	Peripheral Clock
$\overline{\text{ARDYEN}}$	Asynchronous Ready Enable
$\overline{\text{ARDY}}$	Asynchronous Ready
$\overline{\text{SRDYEN}}$	Synchronous Ready Enable
$\overline{\text{SRDY}}$	Synchronous Ready
$\overline{\text{READY}}$	Bus Cycle Termination
$\overline{\text{S0}}$, $\overline{\text{S1}}$	Status
RESET	Reset
$\overline{\text{RES}}$	Reset In
VCC	Power supply (+5V)
GND	Ground (0V)

The SAB 82284 is a bipolar clock generator/driver which provides clock signals for SAB 80286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

May 1987

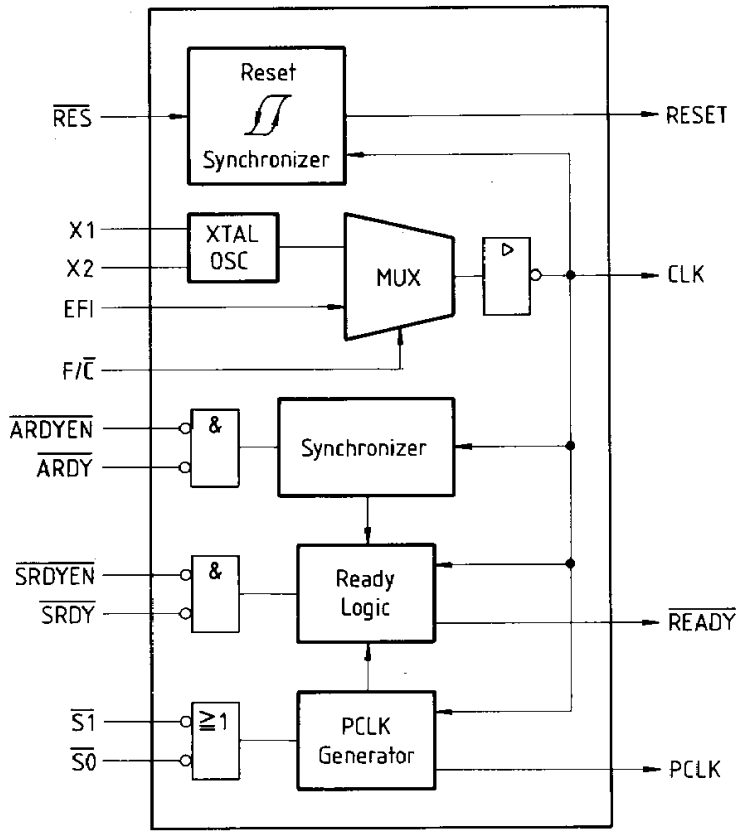
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{ARDY}$	1	I	ASYNCHRONOUS READY is an active low input used to terminate the current bus cycle. The $\overline{ARDY}$ input is qualified by $\overline{ARDYEN}$. Inputs to ARDY may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{SRDY}$	2	I	SYNCHRONOUS READY is an active low input used to terminate the current bus cycle. The $\overline{SRDY}$ input is qualified by the $\overline{SRDYEN}$ input. Setup and hold times must be satisfied for proper operation.
$\overline{SRDYEN}$	3	I	SYNCHRONOUS READY ENABLE is an active low input which qualifies $\overline{SRDY}$. $\overline{SRDYEN}$ selects $\overline{SRDY}$ as the source for $\overline{READY}$ to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
$\overline{READY}$	4	O	READY is an active low output which signals the current bus cycle is to be completed. The $\overline{SRDY}$, $\overline{SRDYEN}$, $\overline{ARDY}$, $\overline{ARDYEN}$, $\overline{S1}$, $\overline{S0}$ and $\overline{RES}$ inputs control $\overline{READY}$ as explained later in the $\overline{READY}$ generator section. $\overline{READY}$ is an open collector output requiring an external pullup resistor.
EFI	5	I	EXTERNAL FREQUENCY IN drives CLK when the F/$\overline{C}$ input is strapped high. The EFI input frequency must be twice the desired internal processor clock frequency.
F/$\overline{C}$	6	I	FREQUENCY/CRYSTAL SELECT is a strapping option to select the source for the CLK output. When F/$\overline{C}$ is strapped low, the internal crystal oscillator drives CLK. When F/$\overline{C}$ is strapped high, the EFI input drives the CLK output.
X1, X2	7, 8	I	CRYSTAL IN are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/$\overline{C}$ is low, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
CLK	10	O	SYSTEM CLOCK is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
$\overline{RES}$	11	I	RESET IN is an active low input which generates the system reset signal RESET. Signals to $\overline{RES}$ may be applied asynchronously to CLK. A Schmitt-trigger input is provided on $\overline{RES}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
RESET	12	O	RESET is an active high output which is derived from the $\overline{RES}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{READY}$ will be active (low).

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
PCLK	13	O	PERIPHERAL CLOCK is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{S0}$, $\overline{S1}$	15, 16	I	STATUS inputs prepare the SAB 82284 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control $\overline{READY}$. These inputs have pullup resistors to keep them high if nothing is driving them. Setup and hold times must be satisfied for proper operation.
$\overline{ARDYEN}$	17	I	ASYNCHRONOUS READY ENABLE is an active low input which qualifies the $\overline{ARDY}$ input. $\overline{ARDYEN}$ selects $\overline{ARDY}$ as the source of ready for the current bus cycle. Inputs to $\overline{ARDYEN}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
VCC	18	–	POWER SUPPLY (+5 V)
GND	9	–	GROUND (0 V)

Block Diagram



Functional Description

Introduction

The SAB 82284 generates the clock, ready, and reset signals required for SAB 80286 processors and support components. The SAB 82284 is packaged in an 18-pin DIP package and contains a crystal-controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready synchronization logic, and system reset generation logic.

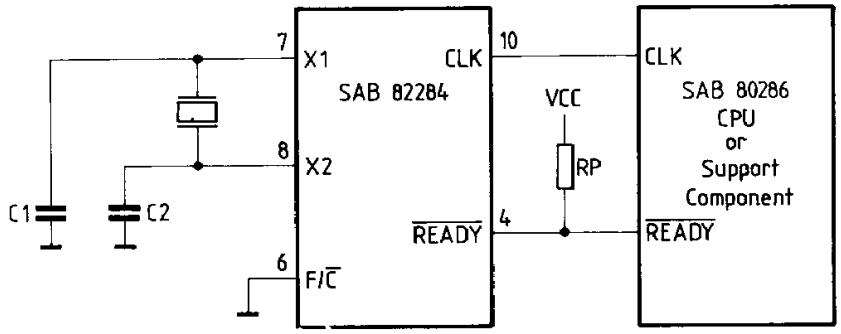
Clock generator

The CLK output provides the basic timing control for an SAB 80286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is low, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is high, the EFI input drives the CLK output. The SAB 82284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL output drive characteristics. PCLK is normally synchronized to the internal processor clock. After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its high time beyond one system clock (see waveforms). PCLK is forced high whenever either $\overline{S0}$ or $\overline{S1}$ were active (low) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are high.
Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the SAB 82284 is a linear Pierce oscillator which requires an external, parallel, resonant, fundamental-mode crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.
X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in the figure below. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10pF between the X1 and X2 pins.
Decouple VCC and GND as close to the SAB 82284 as possible.

Recommended Crystal and $\overline{\text{READY}}$ Connections
(for RP see note 6 of ac characteristics)



Crystal Loading Table

Crystal Frequency	C1 Capacitance	C2 Capacitance
2 to 8MHz	60pF	40pF
8 to 20MHz	25pF	15pF

Reset Operation

The reset logic provides the RESET output to force the system into a known initial state. When the $\overline{RES}$ input is active (low), the RESET output becomes active (high). $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{RES}$ input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have a stable VCC and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until VCC and CLK stabilize at their operating values. SAB 80286 processors and support components also require their RESET inputs be high a minimum number of CLK cycles. An RC network, as shown below, will keep $\overline{RES}$ low long enough to satisfy both needs.

A Schmitt-trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches from high to low from the input voltage level at which the circuit output switches from low to high. The $\overline{RES}$ high to low input transition voltage is lower than the $\overline{RES}$ low to high input transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

Ready Operation

The SAB 82284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

The figure on synchronous ready mode illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S1}$ and $\overline{S0}$ are inactive and PCLK is high. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as low.

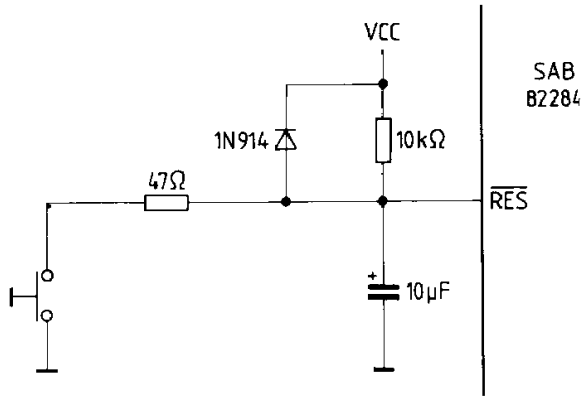
The figure on asynchronous ready mode shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is high. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ inputs to have been active (low), $\overline{READY}$ becomes active (low) and the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored.

$\overline{READY}$ remains active until either $\overline{S1}$ or $\overline{S0}$ is sampled low, or the ready inputs are sampled as inactive.

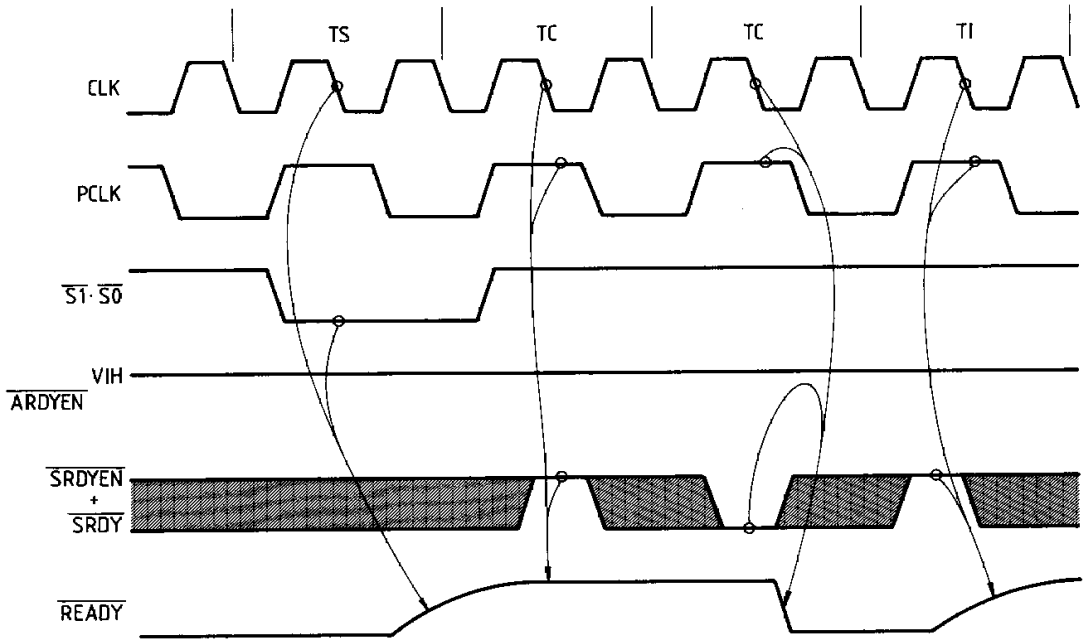
$\overline{READY}$ is enabled (low), if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0 or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0 when sampled by the SAB 82284 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-collector driver allowing other ready circuits to be wire-ORed with it. The $\overline{READY}$ signal of an SAB 80286 system requires an external pullup resistor (see Note 6 of AC Characteristics). To force the $\overline{READY}$ signal inactive (high) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled low at the falling edge of CLK. Two system clock periods are allowed for the pullup resistor to pull the $\overline{READY}$ signal to VIH. When RESET is active, $\overline{READY}$ is forced active one CLK later (see waveforms).

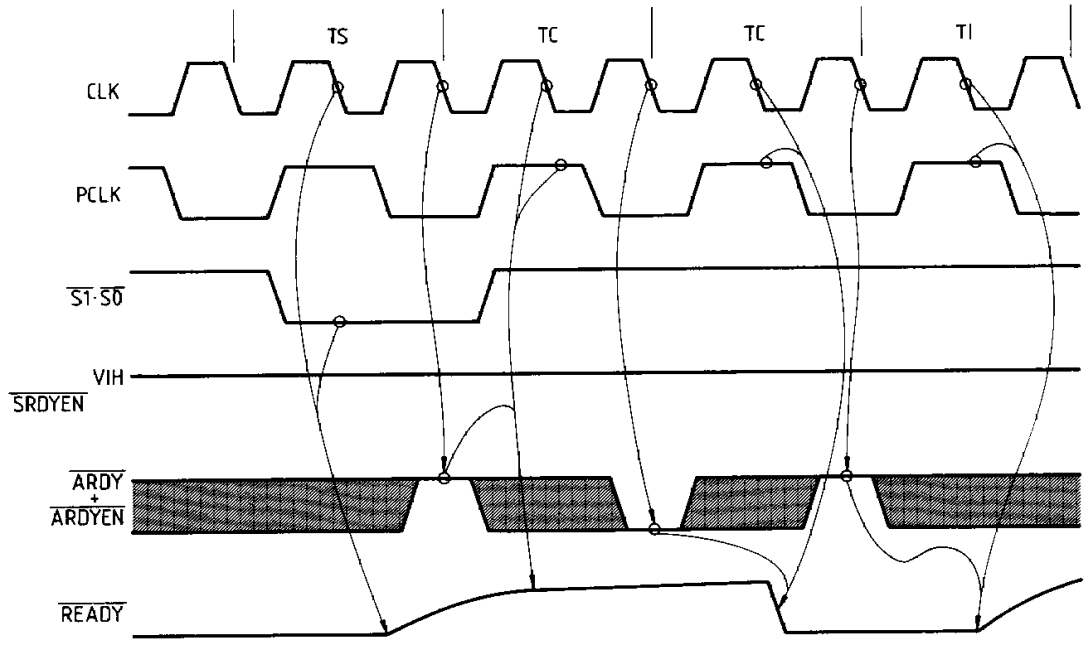
Typical RC $\overline{RES}$ Timing Circuit



Synchronous Ready Operation



Asynchronous Ready Operation



Absolute Maximum Ratings [1]

Temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
All output and supply voltages	−0.5 to +7V
All input voltages	−1.0 to +5.5V
Power dissipation	1 W

DC Characteristics

TA = 0 to 70°C, VCC = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
IF	Forward input current	–	−0.5	mA	VF = 0.45V
IR	Reverse input current	–	50	µA	VR = VCC
VC	Input forward clamp voltage	–	−1.0	V	IC = −5mA
ICC	Power supply current	–	145	mA	–
VIL	Input low voltage	–	0.8	V	–
VIH	Input high voltage	2.0	–	V	–
VOL, VCL	Output low voltage	–	0.45	V	IOL = 5mA (8.5mA at $\overline{\text{READY}}$)
VCH	CLK output high voltage	4.0	–	V	IOH = −1mA
VOH	Output high voltage	2.4	–	V	IOH = −1mA
VIHR	$\overline{\text{RES}}$ input high voltage	2.6	–	V	–
VIHR – VILR	$\overline{\text{RES}}$ input hysteresis	0.25	–	V	–
CI	Input capacitance	–	10	pF	fC = 1 MHz

[1] Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 82284

TA = 0 to 70°C, VCC = 5V ±10%
AC timings are referenced to 0.8 and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
T1	EFI to CLK delay	–	30	ns	at 1.5V [1]
T2	EFI low time	22	–	ns	at 1.5V [1] [2]
T3	EFI high time	30	–	ns	at 1.5V [1] [2]
T4	CLK period	62	500	ns	–
T5	CLK low time	15	–	ns	at 1.0V [1] [2] [3] [4]
T6	CLK high time	25	–	ns	at 3.6V [1] [2] [3] [4]
T7	CLK rise time	–	10	ns	from 1.0V to 3.6V [1]
T8	CLK fall time	–	10	ns	from 3.6V to 1.0V [1]
T9	Status setup time	22.5	–	ns	[1]
T10	Status hold time	1	–	ns	[1]
T11	$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ setup time	15	–	ns	[1]
T12	$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ hold time	0	–	ns	[1]
T13	$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ setup time	0	–	ns	[1] [5]
T14	$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ hold time	30	–	ns	[1] [5]
T15	$\overline{\text{RES}}$ setup time	20	–	ns	[1] [5]
T16	$\overline{\text{RES}}$ hold time	10	–	ns	[1] [5]
T17	$\overline{\text{READY}}$ inactive delay	5	–	ns	at 0.8V [6]
T18	$\overline{\text{READY}}$ active delay	0	24	ns	at 0.8V [6]
T19	PCLK delay	0	45	ns	[7]
T20	RESET delay	5	34	ns	[7]
T21	PCLK low time	T4–20	–	ns	at 0.6V [7] [8]
T22	PCLK high time	T4–20	–	ns	at 2.0V [7] [8]

For notes refer to page 10.

AC Characteristics SAB 82284-1

TA = 0 to 70°C, VCC = 5V ±10%
AC timings are referenced to 0.8 and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
T1	EFI to CLK delay	–	30	ns	at 1.5V [1]
T2	EFI low time	25	–	ns	at 1.5V [1] [2]
T3	EFI high time	25	–	ns	at 1.5V [1] [2]
T4	CLK period	50	500	ns	–
T5	CLK low time	12	–	ns	at 1.0V [1] [2] [3] [4]
T6	CLK high time	16	–	ns	at 3.6V [1] [2] [3] [4]
T7	CLK rise time	–	8	ns	from 1.0V to 3.6V [1]
T8	CLK fall time	–	8	ns	from 3.6V to 1.0V [1]
T9	Status setup time	20	–	ns	[1]
T10	Status hold time	1	–	ns	[1]
T11	$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ setup time	15	–	ns	[1]
T12	$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ hold time	0	–	ns	[1]
T13	$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ setup time	0	–	ns	[1] [5]
T14	$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ hold time	30	–	ns	[1] [5]
T15	$\overline{\text{RES}}$ setup time	20	–	ns	[1] [5]
T16	$\overline{\text{RES}}$ hold time	10	–	ns	[1] [5]
T17	$\overline{\text{READY}}$ inactive delay	5	–	ns	at 0.8V [6]
T18	$\overline{\text{READY}}$ active delay	0	24	ns	at 0.8V [6]
T19	PCLK delay	0	35	ns	[7]
T20	RESET delay	5	27	ns	[7]
T21	PCLK low time	T4–20	–	ns	at 0.6V [7] [8]
T22	PCLK high time	T4–20	–	ns	at 2.0V [7] [8]

For notes refer to page 10.

Notes referring to AC Characteristics:

[1] CLK loading: CL = 150 pF.
The SAB 82284's X1 and X2 inputs are designed primarily for parallel resonant crystals. Serial resonant crystals may oscillate up to 0.01% faster than their rated frequencies, when used with the SAB 82284. For either type capacitive loading should be according to the crystal loading table.

[2] At CLK frequencies above 12 MHz, CLK high and low times are guaranteed only when using a crystal with recommended capacitive loading (see table), not when driving the component from EFI input.

[3] With either the internal oscillator and recommended crystal and load or with the EFI input meeting specifications T2 and T3. The values from the crystal loading table are ±5 pF and include all stray capacitances. Decouple VCC and GND as close to the SAB 82284 as possible.

[4] When using a crystal (with recommended load) appropriate for speed of the SAB 80286, CLK output low and high times are guaranteed to meet the SAB 80286 requirements.

[5] This is an asynchronous input. The specification is given for testing purposes only, to assure recognition at a specific clock edge.

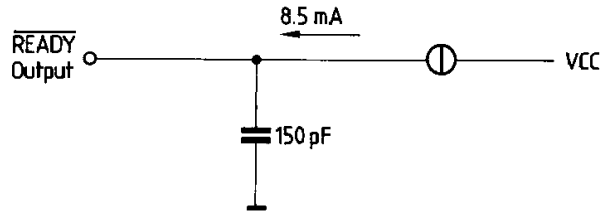
[6] $\overline{\text{READY}}$ loading: CL = 150 pF, pullup resistor RP, with RP = 910 Ω.

[7] PCLK and RESET loading: CL = 75 pF. PCLK output with 750 Ω pullup resistor.

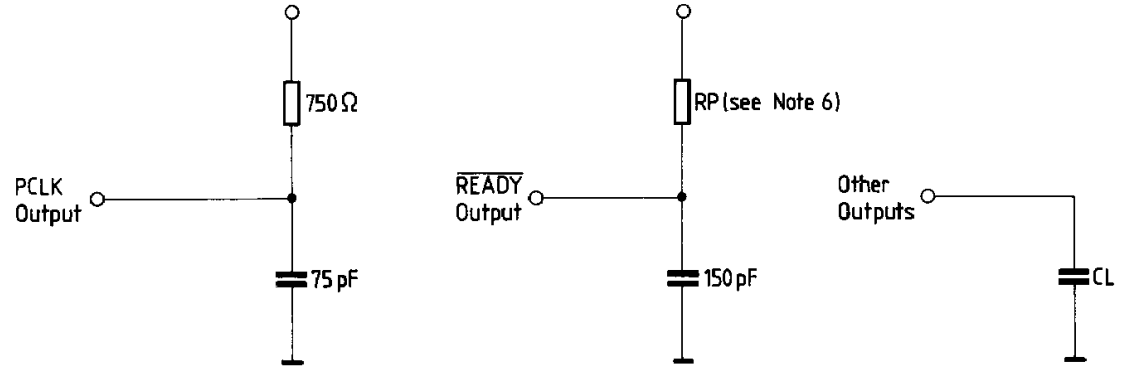
[8] T4 refers to any allowable CLK period.

Testing Waveforms

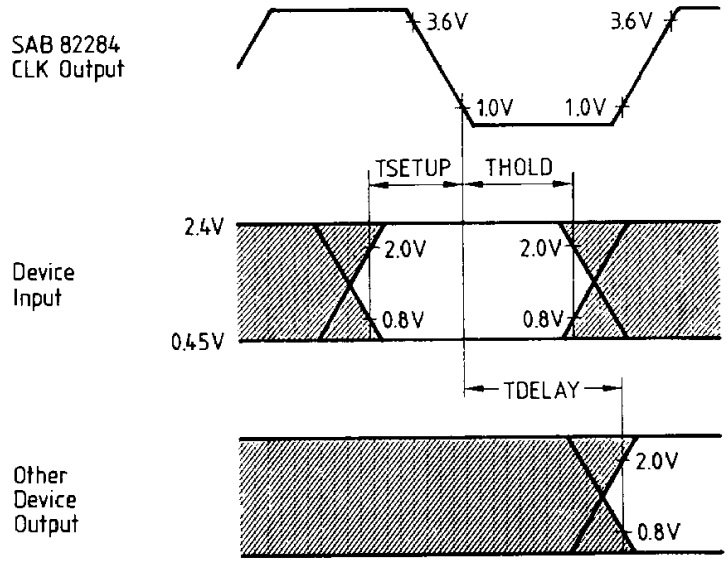
DC Test Loadings



AC Test Loadings

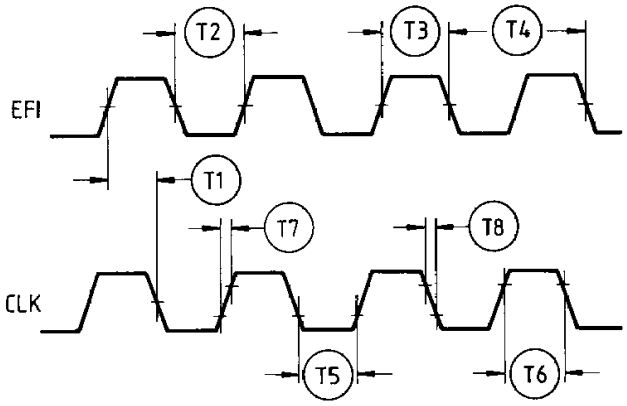


Setup, Hold and Delay Time Measurement – General



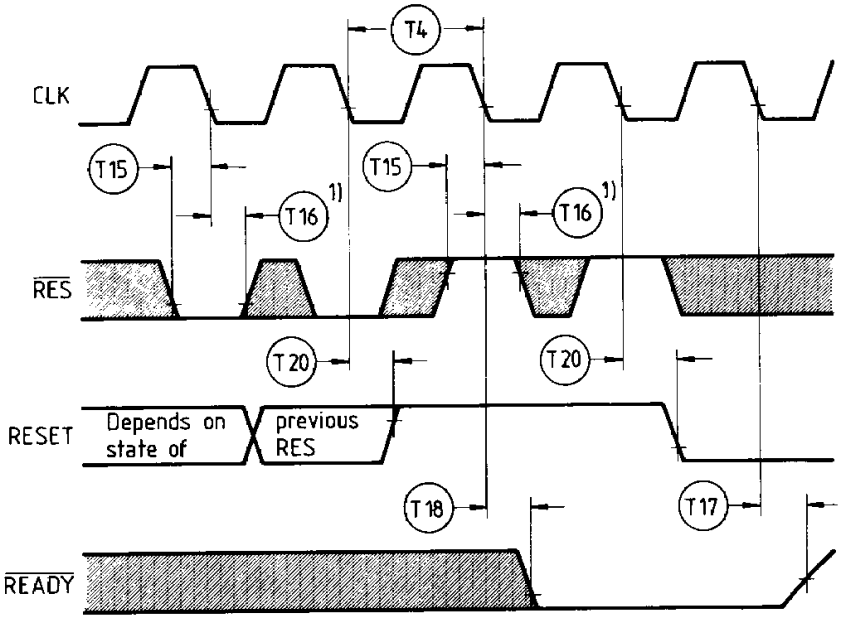
Waveforms

CLK versus EFI



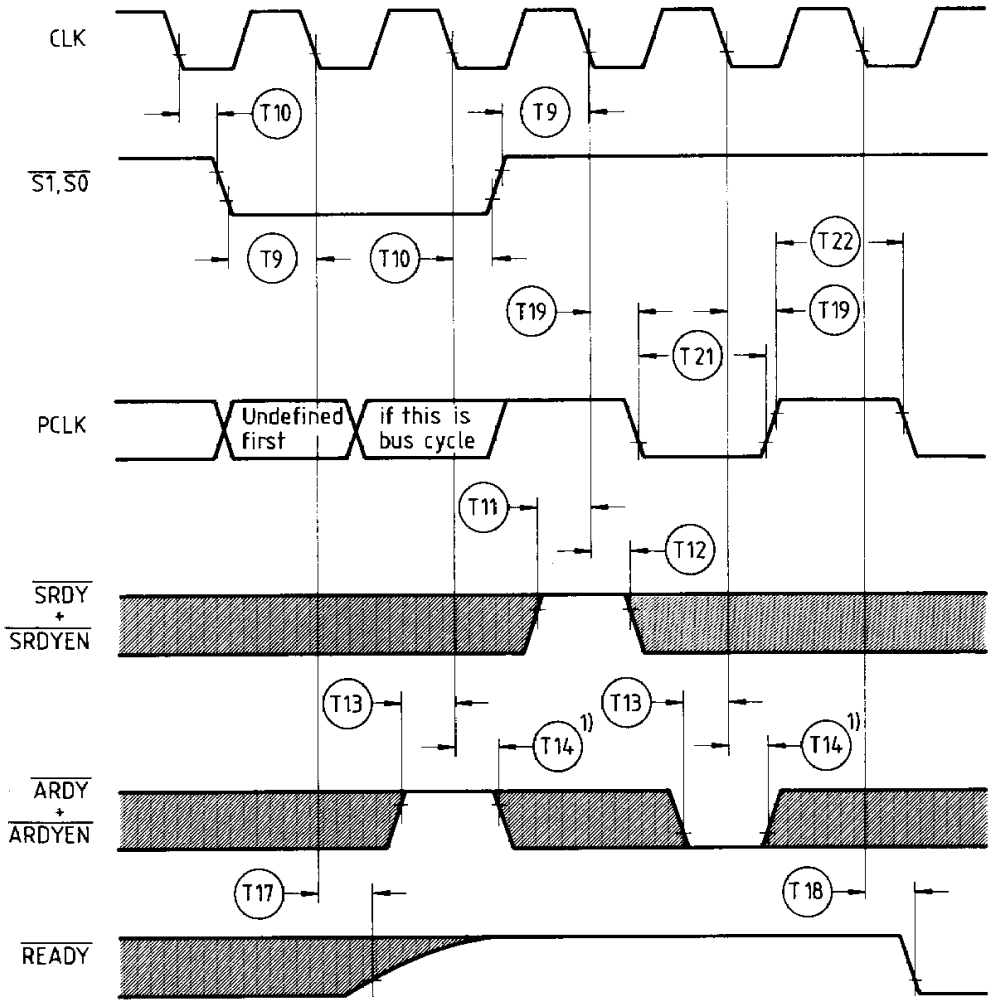
The EFI input low and high times as shown are required to guarantee the CLK low and high times shown.

RESET and $\overline{\text{READY}}$ Timing versus $\overline{\text{RES}}$ with $\overline{\text{S1}}$ and $\overline{\text{S0}}$ High



[1] This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
[2] One or two CLK cycles depending on PCLK phase.

$\overline{\text{READY}}$ and PCLK Timing with $\overline{\text{RES}}$ High



1) This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

Ordering Information

Type	Description	Ordering code
SAB 82284-P	Clock generator (plastic package) up to 16 MHz	Q67020-Y162
SAB 82284-1-P	Clock generator (plastic package) up to 20 MHz	Q67020-Y167