PT6301
5 x 7 Dot Character x 20-Digit x 2-Line Display Controller/Driver with Character RAM

DESCRIPTION

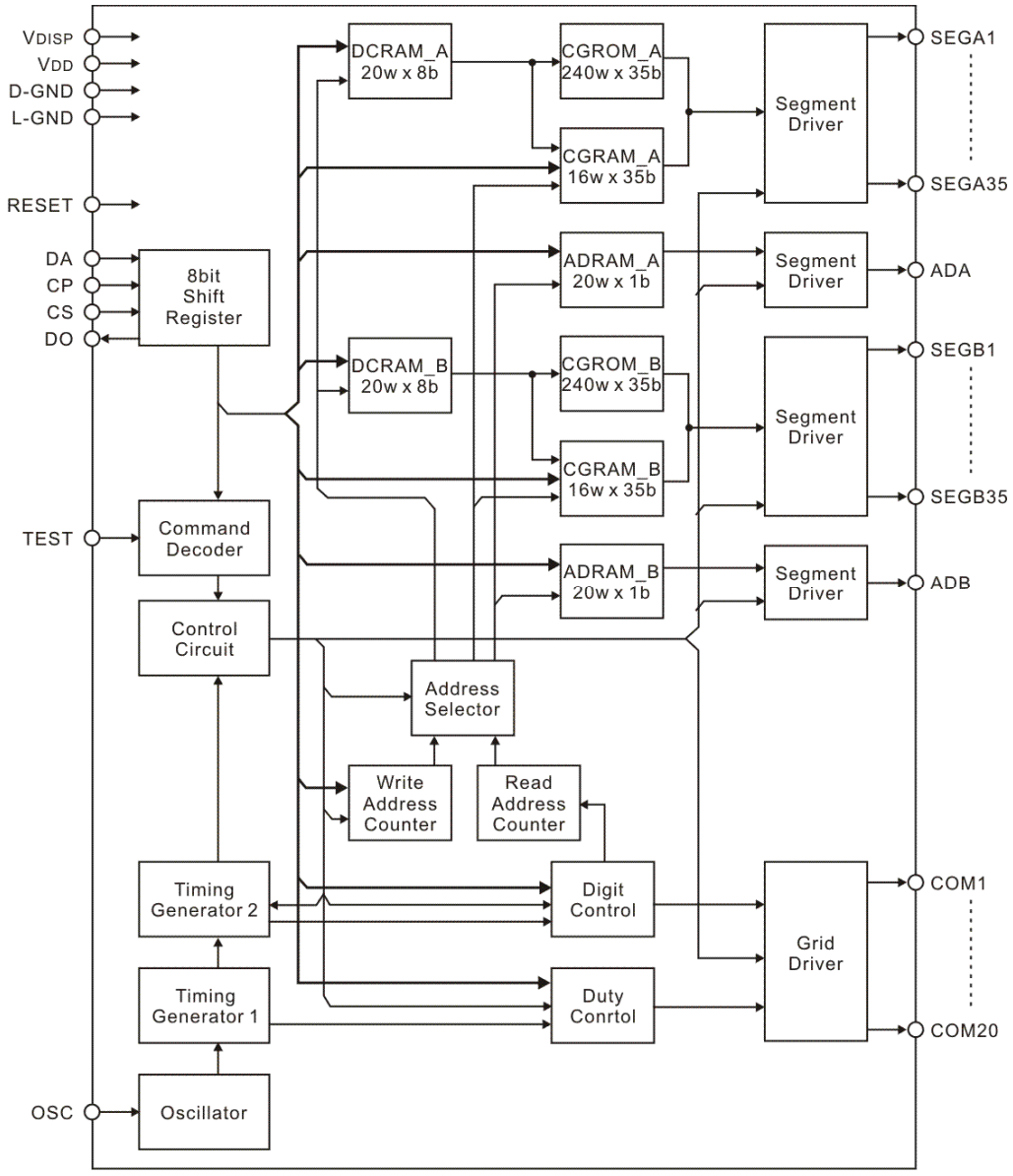
The PT6301 is a 5 × 7 dot matrix type vacuum fluorescent display tube controller driver IC which displays characters, numerics and symbols of a maximum of 20 digits × 2 lines. Dot matrix vacuum fluorescent display tube drive signals are generated by serial data sent from a micro-controller.
A display system is easily realized by internal ROM and RAM for character display. PT6301 has low power consumption since it is made by CMOS process technology. Custom codes are provided on customer's request.

FEATURES

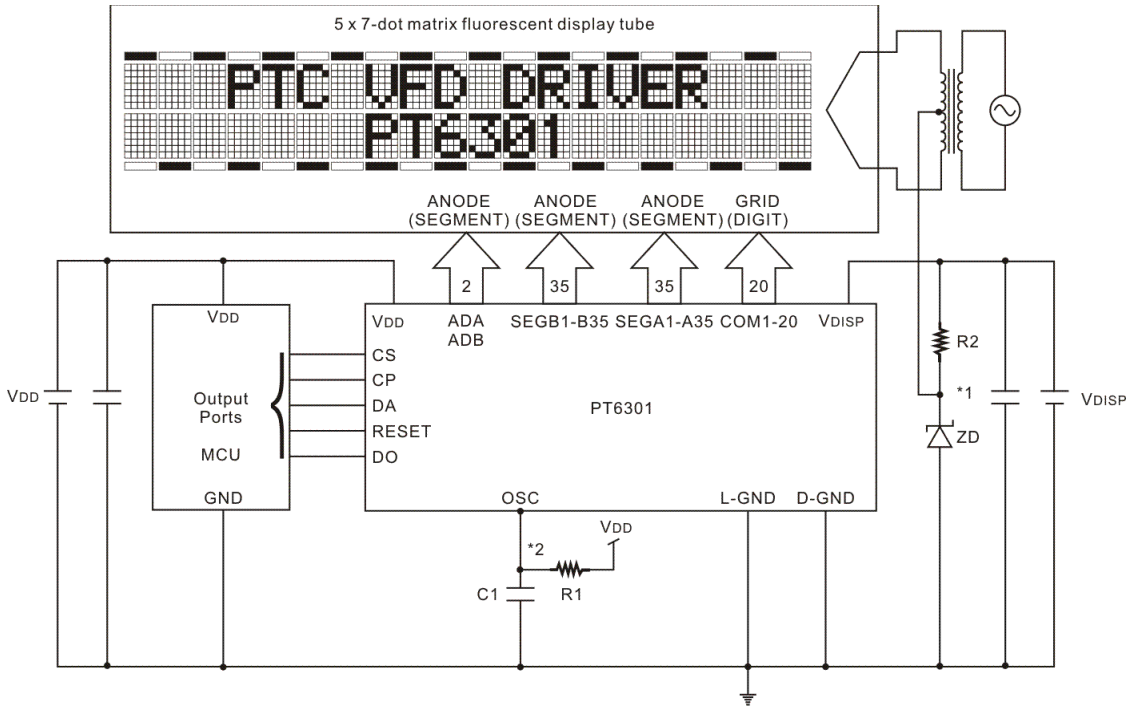
- Logic power supply (V_{DD}): 3.3V±10% or 5.0V±10%
- VFD tube drive power supply (V_{DISP}): 30 to 60V
- VFD driver output current(VFD driver output can be connected directly to the VFD tube. No pull-down resistor is required.)
  - Segment driver (SEGA1 to A35, SEGB1 to B35)
    Only one driver output is high: -5mA @ V_{DISP}-4V (V_{DISP}=50V, Tj=25℃)
    All the driver outputs are high: -350mA @ V_{DISP}-4V (V_{DISP}=50V, Tj=25℃)
  - Segment driver (ADA, ADB): -15mA @ V_{DISP}-4V (V_{DISP}=50V, Tj=25℃)
  - Grid driver (COM1 to 20): -40mA @ V_{DISP}-4V (V_{DISP}=50V, Tj=25℃)
- Content of display
  SEGA1 to SEGA35 and ADA
  - CGROM_A 5 × 7 dots: 240 types (character data)
  - CGRAM_A 5 × 7 dots: 16 types (character data)
  - ADRAM_A 20 (display digit) × 1 bit (symbol data; can be used for a cursor.)
  - DCRAM_A 20 (display digit) × 8 bits (register for character data display)

  SEGB1 to SEGB35 and ADB
  - CGROM_B 5 × 7 dots: 240 types (character data)
  - CGRAM_B 5 × 7 dots: 16 types (character data)
  - ADRAM_B 20 (display digit) × 1 bit (symbol data; can be used for a cursor.)
  - DCRAM_B 20 (display digit) × 8 bits (register for character data display)
- Display control function
  - Display digit: 1 to 20 digits
  - Display duty (brightness adjustment): 0/1024 to 960/1024 stages
  - All lights ON/OFF
- 4 interfaces with microcontroller : DA, CS, CP, and RESET
- Built-in oscillation circuit (external R & C)
- Standby function
  Inhibiting the oscillator circuit provides low power consumption.
- Built-in CIG testing circuit
- Available in CIG package type

BLOCK DIAGRAM



APPLICATION CIRCUIT

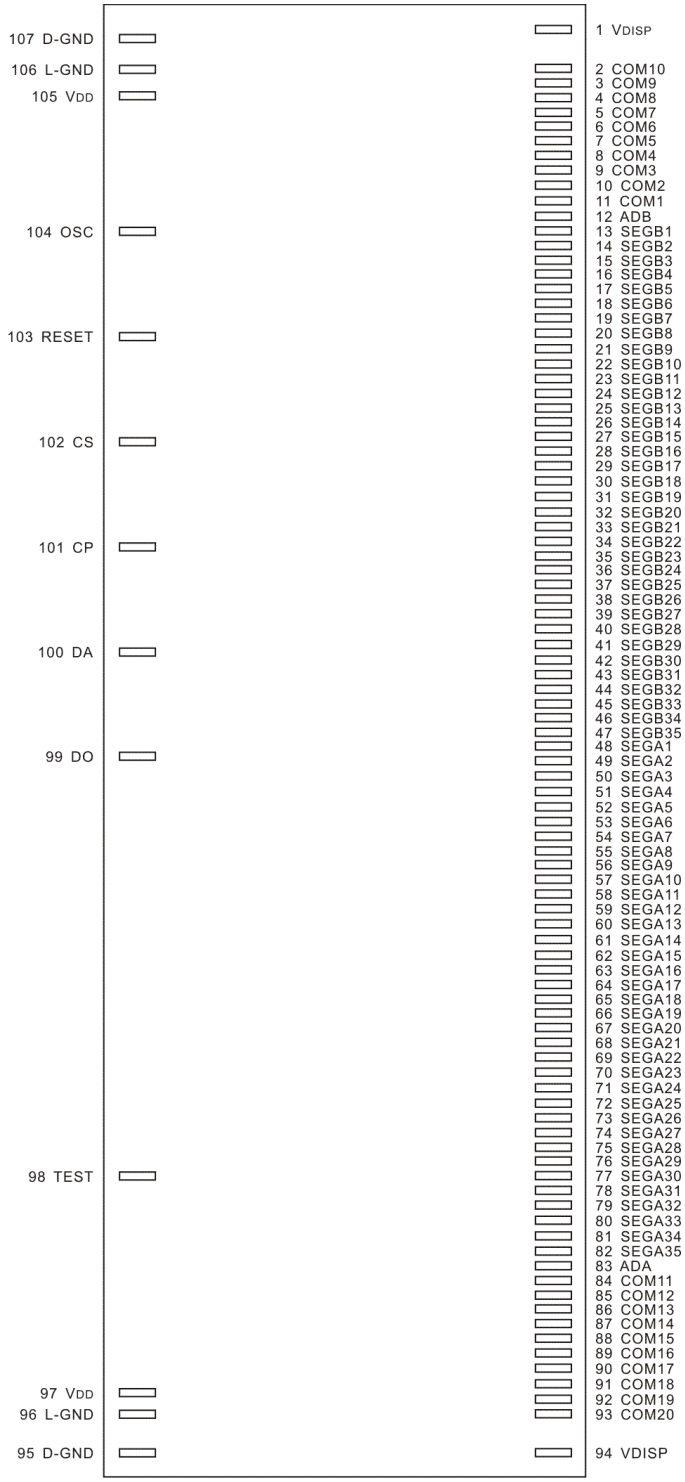


Notes:
*1. The V_{DISP} voltage depends on the fluorescent display tube used. Adjust the value of the constants R2 and ZD to the V_{DISP} voltage used.
*2. The value of R1 & C1 depend on PT6301 IC chip Supply voltage of V_{DD} (R1=8.2KΩ, C1=39pF, when V_{DD}=5V; R1=6.2KΩ, C1=39pF, when V_{DD}=3.3V).

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6301	CIG	-

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SEGA1 ~ SEGA35	O	VFD tube anode electrode drive output. Directly connected to fluorescent display tube and a pulldown resistor is not necessary. IOH > -5mA	48 ~ 82
SEGB1 ~ SEGB35			13 ~ 47
COM1 ~ COM20	O	VFD tube grid electrode drive output. Directly connected to fluorescent display tube and a pulldown resistor is not necessary. IOH > -40mA	11 ~ 2, 84 ~ 93
ADA, ADB	O	VFD tube anode electrode drive output. Directly connected to fluorescent display tube and a pulldown resistor is not necessary. IOH > -15mA	83, 12
V_{DD}	-	V_{DD}, L-GND are power supplies for internal logic. V_{DISP}, D-GND are power supplies for driving fluorescent tubes. Apply V_{DISP} after V_{DD} is applied. Use the same power supply for L-GND and D-GND.	97, 105
L-GND			96, 106
V_{DISP}			1, 94
D-GND			95, 107
TEST	I	Test mode control pin "High" → Test mode enable "Low" → Test mode disable	98
DO	O	Data output pin for testing purpose only	99
DA	I	Serial data input (positive logic). Input from LSB.	100
CP	I	Shift clock input. Serial data is shifted on the rising edge of CP.	101
CS	I	Chip select input. Serial data transfer is disabled when CS pin is "H" level.	102
RESET	I	Reset input. "Low" initializes all the functions. Initial status is as follows. • Address of each RAM ...address "00"H • Data of each RAM..... Content is undefined • Display digit.....20 digits • Brightness adjustment....0/1024 • All lights ON or OFF .....OFF mode	103
OSC	I/O	Oscillation connection An oscillator circuit is formed by connecting an external resistor and capacitor at this pin. See Application circuit	104

FUNCTION DESCRIPTION

COMMAND LIST

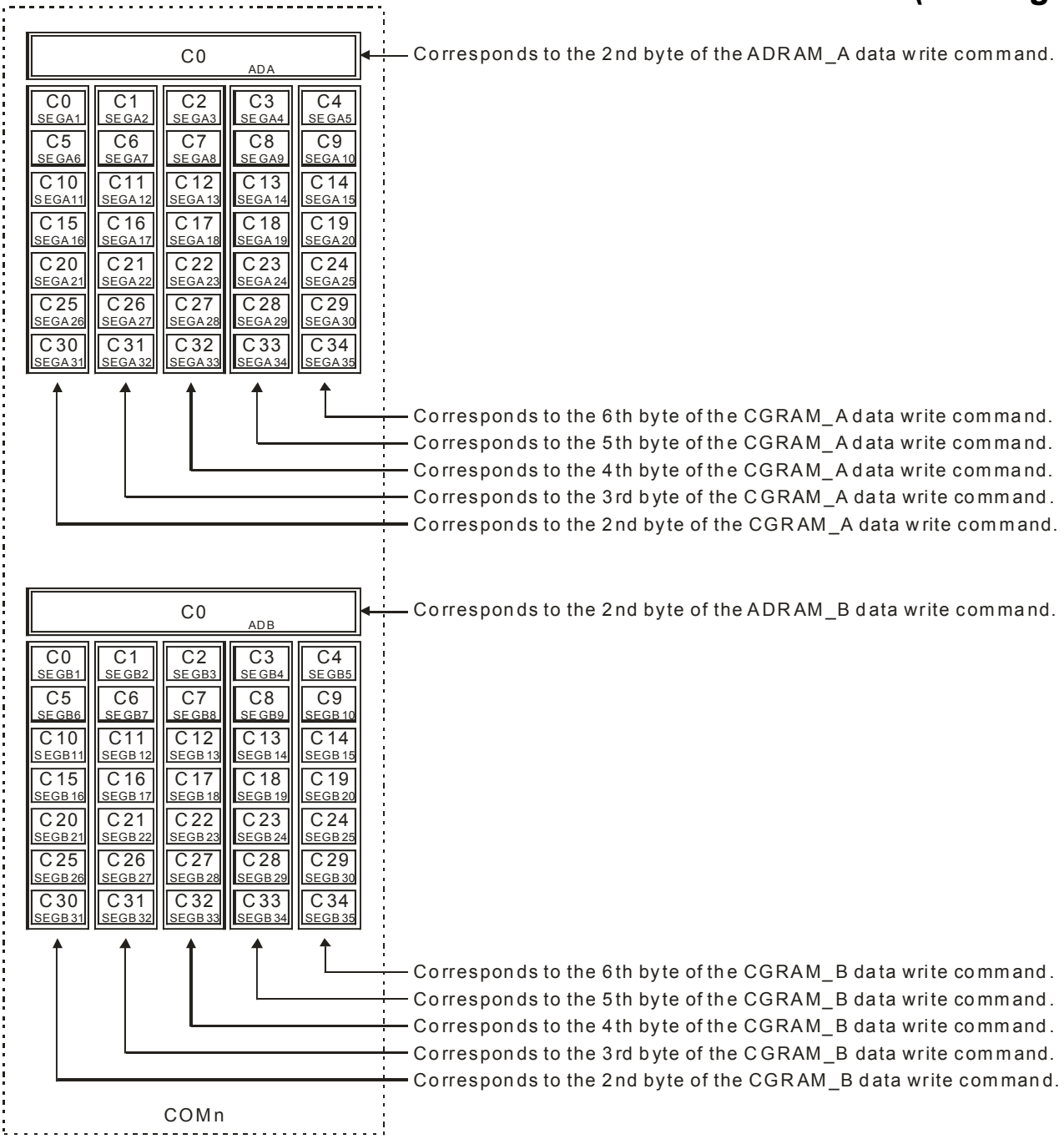
NO.	COMMAND	MSB 1ST BYTE LSB								MSB 2ND BYTE LSB								
		B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0	
1	DCRAM_A Data Write	0	0	0	1	*	*	*	*	C7	C6	C5	C4	C3	C2	C1	C0	
2	CGRAM_A Data Write	0	0	1	0	X3	X2	X1	X0	*	C30	C25	C20	C15	C10	C5	C0	2nd byte
										*	C31	C26	C21	C16	C11	C6	C1	3rd byte
										*	C32	C27	C22	C17	C12	C7	C2	4th byte
										*	C33	C28	C23	C18	C13	C8	C3	5th byte
										*	C34	C29	C24	C19	C14	C9	C4	6th byte
3	ADRAM_A Data Write	0	0	1	1	*	*	*	*	*	*	*	*	*	*	*	C0	
5	Display Duty Set	0	1	0	1	*	*	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	
6	Number of digits set	0	1	1	0	K3	K2	K1	K0									
7	All lights on/off	0	1	1	1	*	*	H	L									
8	Test Mode	1	0	0	0	T3	T2	T1	T0									
9	DCRAM_B Data Write	1	0	0	1	*	*	*	*	C7	C6	C5	C4	C3	C2	C1	C0	
A	CGRAM_B Data Write	1	0	1	0	X3	X2	X1	X0	*	C30	C25	C20	C15	C10	C5	C0	2nd byte
										*	C31	C26	C21	C16	C11	C6	C1	3rd byte
										*	C32	C27	C22	C17	C12	C7	C2	4th byte
										*	C33	C28	C23	C18	C13	C8	C3	5th byte
										*	C34	C29	C24	C19	C14	C9	C4	6th byte
B	ADRAM_B Data Write	1	0	1	1	*	*	*	*	*	*	*	*	*	*	*	C0	
F	Standby Mode	1	1	1	1	*	*	*	*									

*: Don't care
Xn: Address specification for each RAM
Cn: Character code specification for each RAM
Dn: Display duty specification
Kn: Number of digits specification
Tn: Test mode specification
H: All lights ON instruction
L: All lights OFF instruction

When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Note:
The test mode is used for inspection before shipment. It is not a user function. The user cannot use this command. Enter commands 1 to 3, 5 to 7, 9 to B, and F alone in the way described on the next page and the following pages. (The operation of this device cannot be guaranteed if other commands are used.)

POSITIONAL RELATIONSHIP BETWEEN SEGn AND ADn (one digit)

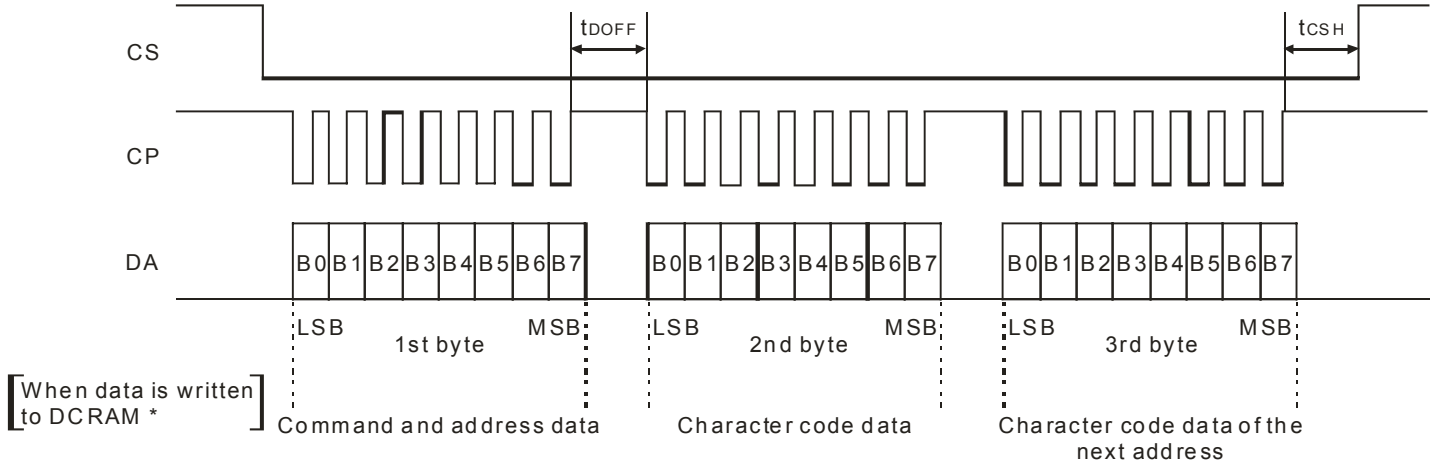


DATA TRANSFER METHOD AND COMMAND WRITE METHOD

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the CS pin to “Low” level enables a data transfer.
Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the CP pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the CS pin to “High” disables data transfer. Data input from the point when the CS pin changes from “High” to “Low” is recognized in 8-bit units.



Note:
When data is written to RAM (DCRAM, ADRAM, CGRAM) continuously, addresses are internally incremented automatically. Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

RESET FUNCTION

Reset is executed when the RESET pin is set to “L”, (when turning power on, for example) and initializes all functions. Initial status is as follows.

Address of each RAM.....address “00”H
Data of each RAM.....All contents are undefined
Display digit .....20 digits
Brightness adjustment 0/1024
All display lights ON or OFF.....OFF mode
Segment output.....All segment outputs go “Low”
AD output.....All AD outputs go “Low”

Be sure to execute the reset operation when turning power on and set again according to “Setting Flowchart” after reset.

DESCRIPTION OF COMMANDS AND FUNCTIONS

1 AND 9. DCRAM DATA WRITE

(Write the character code of CGROM and CGRAM to DCRAM)
DCRAM (Data Control RAM) has 20 address x 8-bit RAM to store character code of CGROM and CGRAM. Address 00H(0) to 13H(19) corresponds to COM1 to 20. The character code stored in DCRAM is CONVERTED TO A 5 x 7 dot matrix character pattern via CGROM or CGRAM.
The DCRAM can store 20 characters. This command writes data from DCRAM address 00H.

COMMAND FORMAT

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Select DCRAM data write mode (RAM address is set to 00H automatically)
	0/1	0	0	1	*	*	*	*	

Note: 0: Select DCRAM_A, 1: Select DCRAM_B

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies character code of CGRAM and CGROM (written into DCRAM address 00H)
	C7	C6	C5	C4	C3	C2	C1	C0	

To specify the character code of CGROM and CGRAM continuously to the next address, specify only character code as follows. The address of DCRAM is automatically incremented.

	MSB							LSB	
2nd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies character code of CGRAM and CGROM (written into DCRAM address 01H)
	C7	C6	C5	C4	C3	C2	C1	C0	

	MSB							LSB	
2nd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies character code of CGRAM and CGROM (written into DCRAM address 02H)
	C7	C6	C5	C4	C3	C2	C1	C0	

⋮

	MSB							LSB	
2nd Byte (21th)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies character code of CGRAM and CGROM (written into DCRAM address 13H)
	C7	C6	C5	C4	C3	C2	C1	C0	

	MSB							LSB	
2nd Byte (22th)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies character code of CGRAM and CGROM (written into DCRAM address 00H)
	C7	C6	C5	C4	C3	C2	C1	C0	

C0 (LSB) to C7 (MSB): Character code of CGROM and CGRAM (8 bits 256 characters)
*: Don't care.

COM POSITIONS AND DCRAM ADDRESSES

DCRAM address (HEX)	COM position	DCRAM address (HEX)	COM position
00H	COM1	0AH	COM11
01H	COM2	0BH	COM12
02H	COM3	0CH	COM13
03H	COM4	0DH	COM14
04H	COM5	0EH	COM15
05H	COM6	0FH	COM16
06H	COM7	10H	COM17
07H	COM8	11H	COM18
08H	COM9	12H	COM19
09H	COM10	13H	COM20

2 AND A. CGRAM DATA WRITE

(Specifies the addresses of CGRAM and write character pattern data)
CGRAM (Character Generator RAM) has 16 address x 35-bit RAM to store 5 x 7 dot matrix character patterns. A character pattern stored in CGRAM can be displayed by specifying the character code in a DCRAM. The address of CGRAM is assigned to 00H to 0FH. (All other addresses are CGROM addresses.) CGRAM can store 16 types of character patterns.

COMMAND FORMAT

1st Byte (1st)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0/1	0	1	0	X3	X2	X1	X0

Select CGRAM data write mode and specifies CGRAM address (Ex. Specifies CGRAM address 00H)

Note: 0: Select CGRAM_A, 1: Select CGRAM_B

2nd Byte (2nd)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C30	C25	C20	C15	C10	C5	C0

Specifies 1st column data (written into CGRAM address 00H)

3rd Byte (3rd)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C31	C26	C21	C16	C11	C6	C1

Specifies 2nd column data (written into CGRAM address 00H)

4th Byte (4th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C32	C27	C22	C17	C12	C7	C2

Specifies 3rd column data (written into CGRAM address 00H)

5th Byte (5th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C33	C28	C23	C18	C13	C8	C3

Specifies 4th column data (written into CGRAM address 00H)

6th Byte (6th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C34	C29	C24	C19	C14	C9	C4

Specifies 5th column data (written into CGRAM address 00H)

To specify the character pattern data continuously to the next address, specify only character pattern data as follows. The address of CGRAM is automatically incremented. Specification of an address is unnecessary.
The 2nd to 6th byte (character pattern data) are regarded as one data item, so 200ns is sufficient for t_{DOFF} time between bytes.

2nd Byte (7th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C30	C25	C20	C15	C10	C5	C0

Specifies 1st column data (written into CGRAM address 01H)

:
:

6th Byte (11th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C34	C29	C24	C19	C14	C9	C4

Specifies 5th column data (written into CGRAM address 01H)

X0 (LSB) to X3 (MSB): CGRAM address (4 bits 16 characters)
C0 (LSB) to C34 (MSB): Character pattern data (35 bits: 35 outputs per character)
*: Don't care.

CGRAM ADDRESSES AND CORRESPONDING CGROM ADDRESS

HEX	X3	X2	X1	X0	CGROM address
0	0	0	0	0	RAM00 (00000000B)
1	0	0	0	1	RAM01 (00000001B)
2	0	0	1	0	RAM02 (00000010B)
3	0	0	1	1	RAM03 (00000011B)
4	0	1	0	0	RAM04 (00000100B)
5	0	1	0	1	RAM05 (00000101B)
6	0	1	1	0	RAM06 (00000110B)
7	0	1	1	1	RAM07 (00000111B)
8	1	0	0	0	RAM08 (00001000B)
9	1	0	0	1	RAM09 (00001001B)
A	1	0	1	0	RAM0A (00001010B)
B	1	0	1	1	RAM0B (00001011B)
C	1	1	0	0	RAM0C (00001100B)
D	1	1	0	1	RAM0D (00001101B)
E	1	1	1	0	RAM0E (00001110B)
F	1	1	1	1	RAM0F (00001111B)

Note: Refer to ROM code tables

3 AND B. ADRAM DATA WRITE

(Writes symbol data)
ADRAM (Additional Data RAM) has 20 address x 1-bit RAM to store symbol data. Address 00H(0) to 13H(19) corresponds to COM1 to 20. Symbol data stored in ADRAM is directly output without translation of CGROM and CGRAM. The ADRAM can store 1 type of symbol patterns per each digit.
The terminal to which the contents of ADRAM are output can be used as a cursor. This command writes data from ADRAM address 00H.

COMMAND FORMAT

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Select ADRAM data write mode (RAM address is set to 00H automatically)
	0/1	0	1	1	*	*	*	*	

Note: 0: Select ADRAM_A, 1: Select ADRAM_B

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	Sets symbol data (written into ADRAM address 00H)
	*	*	*	*	*	*	*	C0	

To specify symbol data continuously to the next address, specify only symbol data as follows. The address of ADRAM is automatically incremented.

	MSB							LSB	
2nd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	Sets symbol data (written into ADRAM address 01H)
	*	*	*	*	*	*	*	C0	

	MSB							LSB	
2nd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	Sets symbol data (written into ADRAM address 02H)
	*	*	*	*	*	*	*	C0	

⋮

	MSB							LSB	
2nd Byte (21th)	B7	B6	B5	B4	B3	B2	B1	B0	Sets symbol data (written into ADRAM address 13H)
	*	*	*	*	*	*	*	C0	

	MSB							LSB	
2nd Byte (22th)	B7	B6	B5	B4	B3	B2	B1	B0	Sets symbol data (re-written into ADRAM address 00H)
	*	*	*	*	*	*	*	C0	

C0: Symbol data (1 bit: 1-symbol data per digit)
*: Don't care.

COM POSITIONS AND ADRAM ADDRESSES

ADRAM address (HEX)	COM position	ADRAM address (HEX)	COM position
00H	COM1	0AH	COM11
01H	COM2	0BH	COM12
02H	COM3	0CH	COM13
03H	COM4	0DH	COM14
04H	COM5	0EH	COM15
05H	COM6	0FH	COM16
06H	COM7	10H	COM17
07H	COM8	11H	COM18
08H	COM9	12H	COM19
09H	COM10	13H	COM20

DISPLAY DUTY SET

(Writes display duty value to duty cycle register)

Display duty adjusts brightness in 1024 stages using 10-bit data.

When power is turned on or when the RESET signal is input, the duty cycle register value is “0”. Always execute this instruction before turning the display on, then set a desired duty value.

COMMAND FORMAT

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Select display duty set mode and set duty value (lower 2 bits)
	0	1	0	1	*	*	D1	D0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	Sets duty value (upper 8 bits)
	D9	D8	D7	D6	D5	D4	D3	D2	

D0 (LSB) to D9 (MSB): Display duty data (10 bits: 1024 stages)

*: Don’t care

RELATION BETWEEN SETUP DATA AND CONTROLLED COM DUTY

HEX	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	COM duty
000	0	0	0	0	0	0	0	0	0	0	0/1024
001	0	0	0	0	0	0	0	0	0	1	1/1024
002	0	0	0	0	0	0	0	0	1	0	2/1024
:											:
3BE	1	1	1	0	1	1	1	1	1	0	958/1024
3BF	1	1	1	0	1	1	1	1	1	1	959/1024
3C0	1	1	1	1	0	0	0	0	0	0	960/1024
3C1	1	1	1	1	0	0	0	0	0	1	960/1024
:											:
3FF	1	1	1	1	1	1	1	1	1	1	960/1024

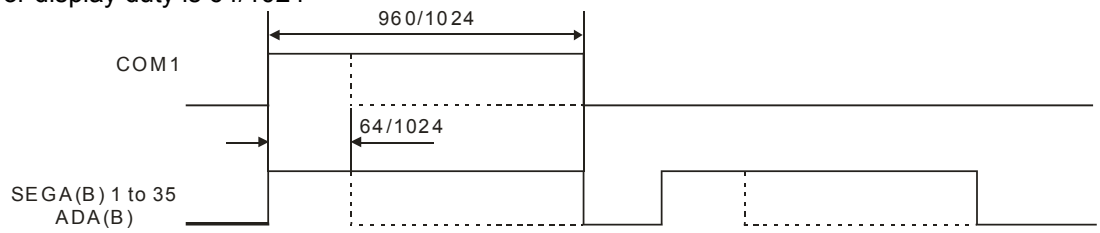
*The state when power is turned on or when RESET signal is input.

DISPLAY DUTY OUTPUT TIMING

Example: COM1

Solid line: For display duty is 960/1024

Doted line: For display duty is 64/1024



NUMBER OF DIGIT SET

(Writes the number of display digit to the display digit register)
This command can set the number of display digit between 5 to 20 digits using 4-bit data. When power is tuned on or when a RESET signal is input, the number of digit register value is “0”. Always execute this instruction to change the number of digit before turning the display on.

COMMAND FORMAT

	MSB							LSB
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0
	0	1	1	0	K3	K2	K1	K0

Select the number of digit set mode and specifies the number of digit value

K0 (LSB) to K3 (MSB): the Number of digit data (4 bits: 5 to 20 digits)
*: Don’t care.

RELATION BETWEEN SETUP DATA AND CONTROLLED COM

HEX	K0	K1	K2	K3	The number of digit of COM	HEX	K0	K1	K2	K3	The number of digit of COM
0	0	0	0	0	COM1 to 20	8	0	0	0	1	COM1 to 12
1	1	0	0	0	COM1 to 5	9	1	0	0	1	COM1 to 13
2	0	1	0	0	COM1 to 6	A	0	1	0	1	COM1 to 14
3	1	1	0	0	COM1 to 7	B	1	1	0	1	COM1 to 15
4	0	0	1	0	COM1 to 8	C	0	0	1	1	COM1 to 16
5	1	0	1	0	COM1 to 9	D	1	0	1	1	COM1 to 17
6	0	1	1	0	COM1 to 10	E	0	1	1	1	COM1 to 18
7	1	1	1	0	COM1 to 11	F	1	1	1	1	COM1 to 19

*The state when power is turned on or when RESET signal is input.

ALL DISPLAY LIGHTS ON/OFF SET

(Turns all display lights ON or OFF)
All display lights ON mode is used primarily for display resting.
(The display duty during ON mode is the value of the duty cycle register.)

All display lights OFF mode is primarily used for display blink and to prevent malfunction when power is turned on.
(All the segment output are “Low”, but COM outputs are still driving.)

COMMAND FORMAT

	MSB							LSB
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0
	0	1	1	1	*	*	H	L

Selects all display lights ON or OFF mode

H, L: Display operation data
*: Don’t care.

SET DATA AND DISPLAY STATE OF SEG AND AD

L	H	Display state of SEG and AD
0	0	Normal display
1	0	Sets all outputs to Low
0	1	Sets all outputs to High
1	1	Sets all outputs to High

(The state when power is turned on or when RESET is input)

F. STAND-BY MODE

(Turning off all display-lights and stopped oscillation function)
This mode turns off all display-lights (fixing COM at “Low”) and stops oscillation function.
This completely stops the internal operation of the PT6301 and attains low power consumption of V_{DD} and V_{DISP}.

Note: If the RESET signal is input while the stand-by mode in progress, the stand-by mode is released and all states are initialized.

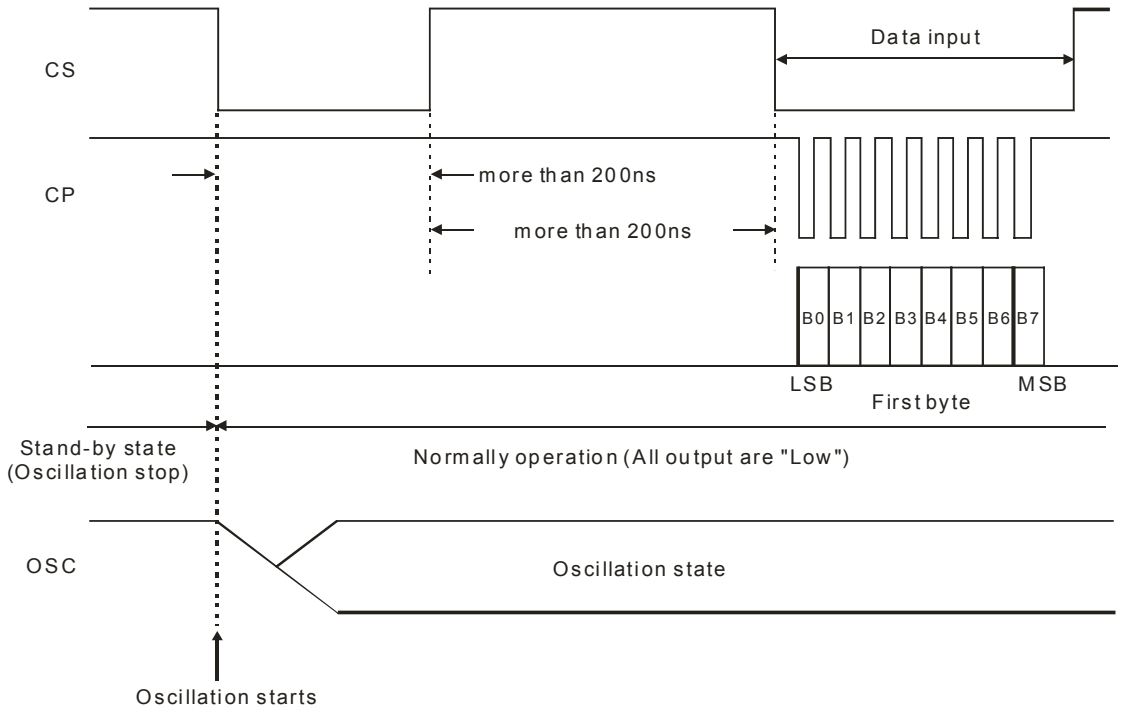
COMMAND FORMAT

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Selects the stand-by mode
	1	1	1	1	*	*	*	*	

*: Don’t care.

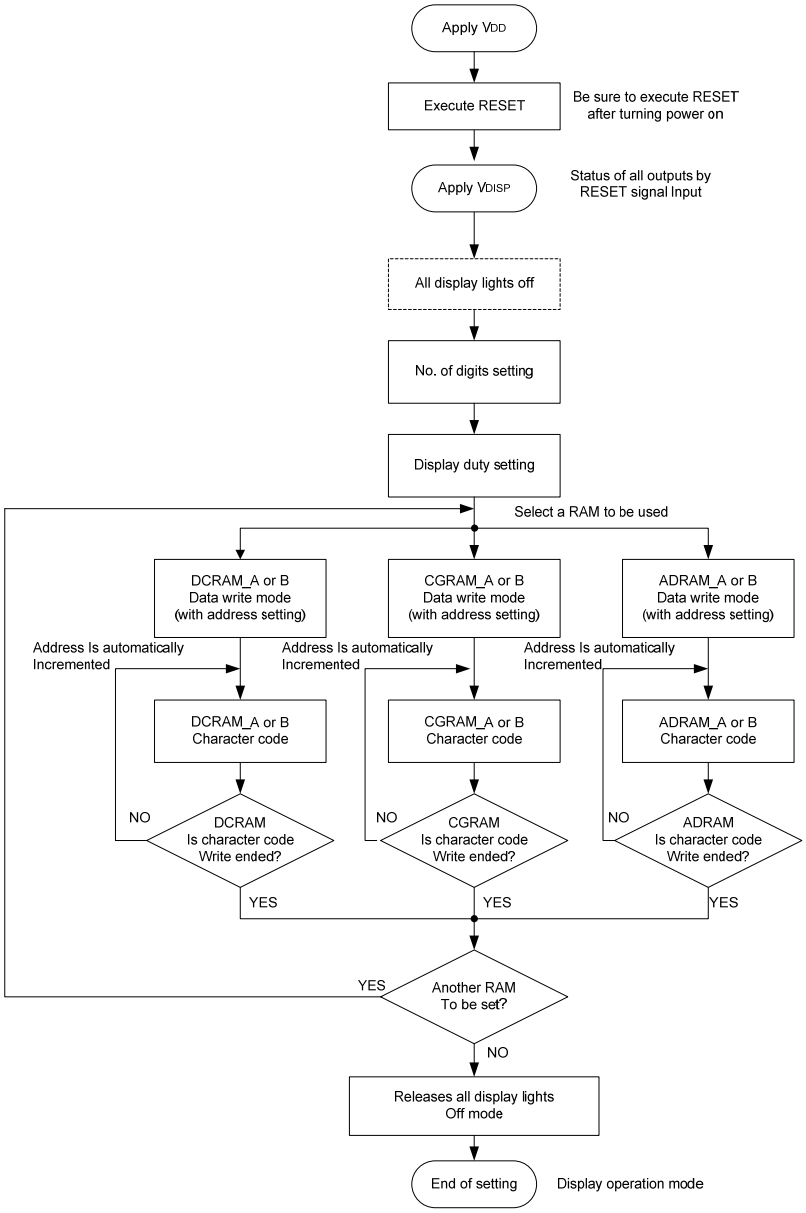
RELEASING THE STAND-BY MODE

The timing to release the stand-by mode is shown below.
The stand-by mode is released at the falling edge of CS. (The internal oscillation starts)
When the oscillation becomes stable, the data input is enabled. (Return CS to “High” before entering data)
After the stand-by mode is released, all display-lights are turned off. Release the all display-lights OFF mode to turn on the display-lights.

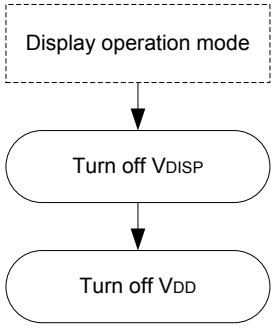


SETTING FLOWCHART

(Power applying included)



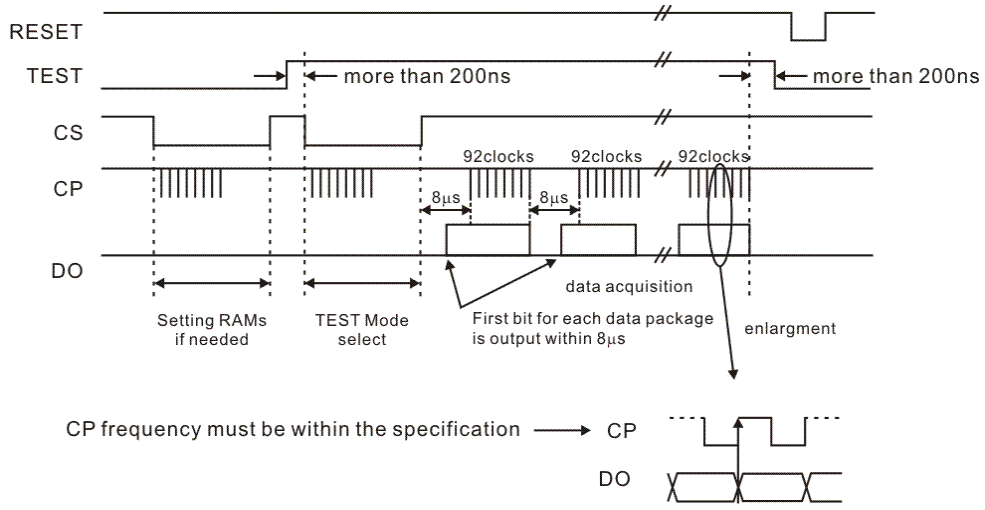
POWER-OFF FLOWCHART



COMMAND WRITE METHOD AND DATA TRANSFER METHOD FOR TEST MODE

BASIC FLOW FOR TEST MODE

Test flow is shown as the following chart.
Detailed data format for each test are explained in the following pages.



TEST MODE LIST

	MSB							LSB	
TEST Mode 1	1	0	0	0	0	0	0	1	Oscillation stop with all output “Low”
TEST Mode 2	1	0	0	0	0	0	1	0	Oscillation stop with all output “High”
TEST Mode 3	1	0	0	0	0	0	1	1	Driver circuit check mode
TEST Mode 4	1	0	0	0	0	1	0	0	DCRAM/ADRAM/DIGIT data output mode
TEST Mode 5	1	0	0	0	0	1	0	1	CGRAM/CGROM data output mode

TEST MODE 1. OSCILLATION STOP WITH ALL OUTPUT “LOW”

In this test, you can confirm that all the driver output signals are changed to “L”. Also, you can measure the static I_{DO} and static I_{DISP} without oscillation.

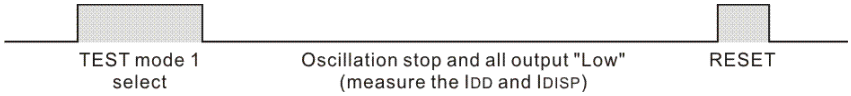
COMMAND FORMAT

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Selects TEST Mode 1
	1	0	0	0	0	0	0	1	

STATUS OF OUTPUT SIGNALS

COM1 to 20: All “L”
ADA, ADB: All “L”
SEGA1 to 35, SEGB1 to 35: All “L”
DO: “L”

TEST FLOW



TEST MODE 2. OSCILLATION STOP WITH ALL OUTPUT “HIGH”

In this test, you can confirm that all the driver output signals are changed to “H”. Also, you can measure the static IDO and static IDISP without oscillation.

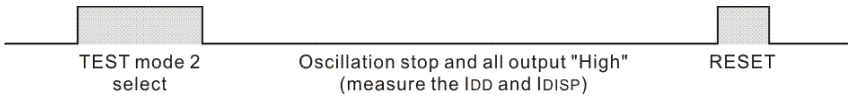
COMMAND FORMAT

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Selects TEST Mode 2
	1	0	0	0	0	0	1	0	

STATUS OF OUTPUT SIGNALS

COM1 to 20: All “H”
ADA, ADB: All “H”
SEGA1 to 35, SEGB1 to 35: All “H”
DO: “H”

TEST FLOW



TEST MODE 3. DRIVER CIRCUIT CHECK MODE

In this mode, all driver outputs can be directly controlled by input data. Driver control data are input by serial transfer from DA pin after TEST mode 3 is selected. Data input method is same as normal operation.

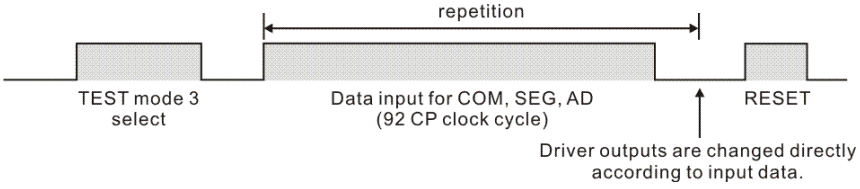
COMMAND FORMAT

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Selects TEST Mode 3
	1	0	0	0	0	0	1	1	

STATUS OF OUTPUT SIGNALS

COM1 to 20: Changed by input data
ADA, ADB: Changed by input data
SEGA1 to 35, SEGB1 to 35: Changed by input data
DO: Undefined

TEST FLOW



INPUT DATA FORMAT

92-bit data are written to DA pin.

First bit					Last bit
COM <20:11>	ADA	SEGA <35:1>	SEGB <35:1>	ADB	COM <1:10>
10-bit	1bit	35-bit	35-bit	1bit	10-bit

TEST MODE 4. DCRAM/ADRAM/DIGIT DATA OUTPUT MODE

In this mode, contents of DCRAM and ADRAM for each digit can be confirmed. DCRAM and ADRAM for each digit must be set before entering TEST mode 4.

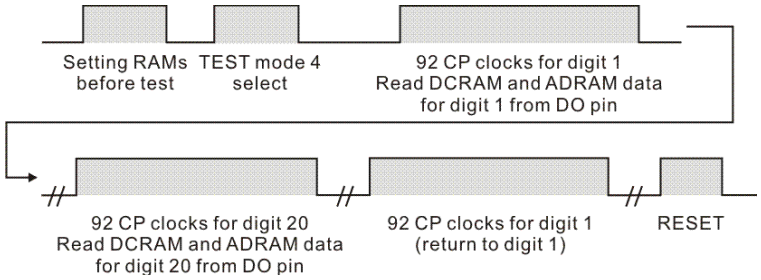
COMMAND FORMAT

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Selects TEST Mode 4
	1	0	0	0	0	1	0	0	

STATUS OF OUTPUT SIGNALS

COM1 to 20: All “L”
ADA, ADB: All “L”
SEGA1 to 35, SEGB1 to 35: All “L”
DO: Data Out

TEST FLOW



OUTPUT DATA FORMAT

92-bit data digits are read from DO pin.

First bit						Last bit
Digit	ADRAM_A	DCRAM_A <1:8>	Null	DCRAM_B <8:1>	ADRAM_B	Digit
COM <20:11> 10-bit	1bit	8-bit	54-bit	8-bit	1bit	COM <1:10> 10-bit

TEST MODE 5. CGRAM/CGROM DATA OUTPUT MODE

In this mode, content of CGRAM and CGROM can be confirmed. CGRAM must be set before entering TEST mode 5.

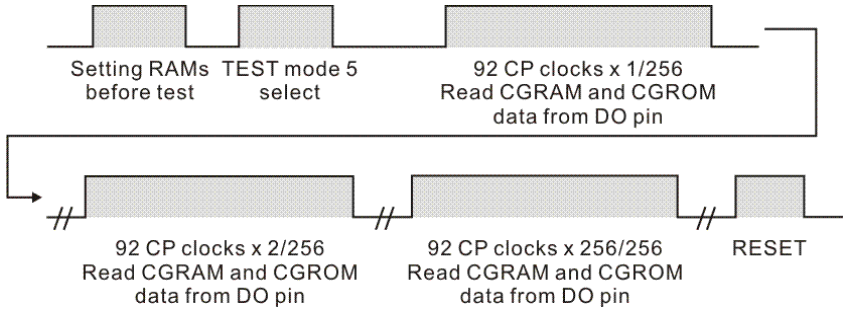
COMMAND FORMAT

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Selects TEST Mode 5
	1	0	0	0	0	1	0	1	

STATUS OF OUTPUT SIGNALS

COM1 to 20: All “L”
ADA, ADB: All “L”
SEGA1 to 35, SEGB1 to 35: All “L”
DO: Data Out

TEST FLOW



OUTPUT DATA FORMAT

92-bit data per character are read from DO pin.

First bit			Last bit
Null	CGRAM_A <35:1> or CGROM_A <35:1>	CGRAM_B <35:1> or CGROM_B <35:1>	Null
11-bit	35-bit	35-bit	11-bit

ABSOLUTE MAXIMUN RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply voltage (1)	V_{DD}	-	-0.3 to +6.5	V
Supply voltage (2)	V_{DISP}	-	-0.3 to +70	V
Input voltage	V_{IN}	-	-0.3 to V_{DD}+0.3	V
Operating temperature	Topr	-	-40 to +85	℃
Storage temperature	Tstg	-	-65 to +150	℃
Output current	I_{O1}	COM1 to COM16	-50 to 2.0	mA
	I_{O2}	ADA, ADB	-25 to 2.0	mA
	I_{O3}	SEGA1 to SEGA35, SEGB1 to SEGB35	-15 to 2.0	mA
	I_{O4}	DO	-2 to 2.0	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	When the power supply voltage is 5V (typ.)	4.5	5.0	5.5	V
		When the power supply voltage is 3.3V (typ.)	3.0	3.3	3.6	
Supply voltage (2)	V_{DISP}	-	30	-	60	V
Operating frequency	fosc	VDD=5.0V, C=39pF, R=8.2KΩ, T_j=25℃	3.0	4.0	5.0	MHz
		VDD=3.3V, C=39pF, R=6.2KΩ, T_j=25℃	3.0	4.0	5.0	
Frame frequency	f_{FR}	DIGIT=1 to 20, oscillation, T_j=25℃	146	195	215	Hz
Junction temperature	Tj	-	-40	-	+125	℃

DC CHARACTERISTICS

(Unless otherwise specified, V_{DD}=5.0V±10%, V_{DISP}=30 to 60V, Tj=-40 to +125℃)

Parameter	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	*1	-	0.8V_{DD}	-	-	V
Low level input voltage	V_{IL}	*1	-	-	-	0.2V_{DD}	V
High level input current	I_{IH}	*1	V_{DO}=V_{IN}=5.0V	-1.0	-	+1.0	μA
Low level input current	I_{IL}	*1	V_{DO}=5.0V, V_{IN}=0.0V	-1.0	-	+1.0	μA
High level output voltage	V_{OH1}	COM1 to 20	V_{DISP}=50V, I_{OH1}=-40mA, Tj=25℃	V_{DISP}-4	-	-	V
	V_{OH2}	ADA, ADB	V_{DISP}=50V, I_{OH2}=-15mA, Tj=25℃	V_{DISP}-4	-	-	V
	V_{OH3}	SEGA1 to 35, SEGB1 to 35	V_{DISP}=50V, I_{OH3}=-5mA, Tj=25℃	V_{DISP}-4	-	-	V
	V_{OH4}	DO	V_{DD}=5.0V, I_{OH4}=-400μA	V_{DD}-0.3	-	-	V
Low level output voltage	V_{OL1}	*2	V_{DISP}=50V, I_{OL1}=+1mA,Tj=25℃	-	-	2.0	V
	V_{OL2}	DO	V_{DD}=5.0V, I_{OL2}=+400μA	-	-	0.3	V
Current consumption (1)	I_{DO1}	V_{DD}	V_{DD}=5.0V, fosc=4.0MHz	-	-	6	mA
	I_{DISP1}	V_{DISP}	fosc=4.0MHz, no load; All output lights on	-	-	1	mA
	I_{DISP2}		fosc=4.0MHz, no load; All output lights off (Typ: Tj=25℃) (Max. Tj=85℃)	-	1.0	15.0	μA
Current consumption (2)	I_{DD}	V_{DD}	Stand-by mode (Typ.: Tj=25℃) (Max. Tj=85℃)	-	1.0	1.0	μA
	I_{DISP}	V_{DISP}		-	1.0	10.0	μA

(Unless otherwise specified, V_{DD}=3.3V±10%, V_{DISP}=30 to 60V, Tj=-40 to +125℃)

Parameter	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	*1	-	0.8V_{DD}	-	-	V
Low level input voltage	V_{IL}	*1	-	-	-	0.2V_{DD}	V
High level input current	I_{IH}	*1	V_{DO}=V_{IN}=3.3V	-1.0	-	+1.0	μA
Low level input current	I_{IL}	*1	V_{DO}=3.3V, V_{IN}=0.0V	-1.0	-	+1.0	μA
High level output voltage	V_{OH1}	COM1 to 20	V_{DISP}=50V, I_{OH1}=-40mA, Tj=25℃	V_{DISP}-4	-	-	V
	V_{OH2}	ADA, ADB	V_{DISP}=50V, I_{OH2}=-15mA, Tj=25℃	V_{DISP}-4	-	-	V
	V_{OH3}	SEGA1 to 35, SEGB1 to 35	V_{DISP}=50V, I_{OH3}=-5mA, Tj=25℃	V_{DISP}-4	-	-	V
	V_{OH4}	DO	V_{DD}=3.3V, I_{OH4}=-400μA	V_{DD}-0.3	-	-	V
Low level output voltage	V_{OL1}	*2	V_{DISP}=50V, I_{OL1}=+1mA,Tj=25℃	-	-	2.0	V
	V_{OL2}	DO	V_{DD}=3.3V, I_{OL2}=+400μA	-	-	0.3	V
Current consumption (1)	I_{DO1}	V_{DD}	V_{DD}=3.3V, fosc=4.0MHz	-	-	4	mA
	I_{DISP1}	V_{DISP}	fosc=4.0MHz no load; All output lights on	-	-	1	mA
	I_{DISP2}		fosc=4.0MHz no load; All output lights off (Typ: Tj=25℃) (Max. Tj=85℃)	-	1.0	15.0	μA
Current consumption (2)	I_{DD}	V_{DD}	Stand-by mode (Typ.: Tj=25℃) (Max. Tj=85℃)	-	1.0	1.0	μA
	I_{DISP}	V_{DISP}		-	1.0	10.0	μA

Notes:
1. *1=CS, CP, DA, RESET
2. *2=SEGA1 to 35, SEGB1 to 35, ADA, ADB, COM1 to 20

AC CHARACTERISTICS

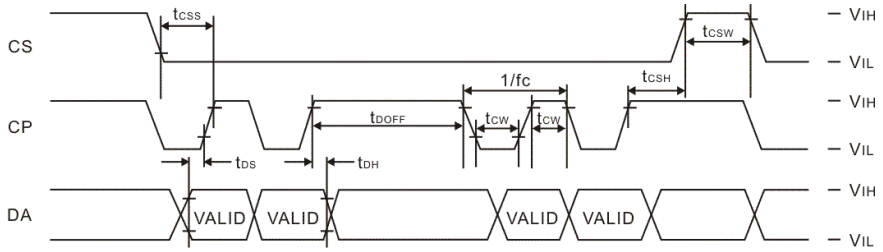
(Unless otherwise specified, V_{DD}=5.0V/3.3V±10%, V_{DISP}=30 to 60V, Tj=-40 to +125℃)

Parameter	Symbol	Condition		Min.	Max.	Unit
CP frequency	fc	-		-	2.0	MHz
CP pulse width	t_{CW}	-		200	-	ns
DA setup time	t_{DS}	-		200	-	ns
DA hold time	t_{DH}	-		200	-	ns
CS setup time	t_{CSS}	-		200	-	ns
CS hold time	t_{CSH}	Oscillation state		8	-	µs
CS wait time	t_{CSW}	-		200	-	ns
Data processing time	t_{DOFF}	Oscillation state		4	-	µs
RESET pulse width	t_{WRES}	When RESET signal is input from microcontroller etc. externally		200	-	ns
DA wait time	t_{RSOFF}	-		200	-	µs
All output slew rate	t_R	C_I=100pF	t_R=20 to 80%	-	2.0	µs
	t_F		t_F=80 to 20%	-	2.0	

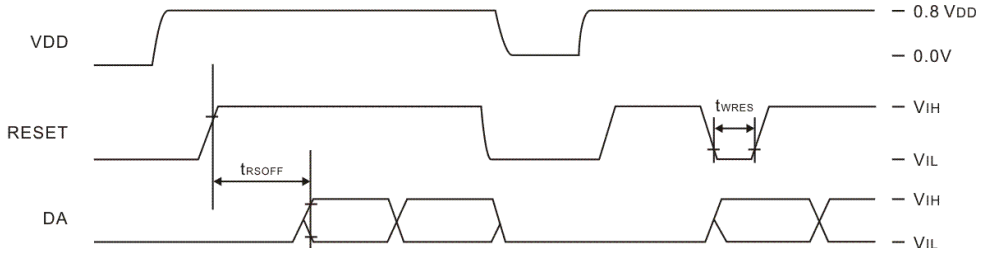
TIMING DIAGRAM

Symbol	V_{DD}=3.3V±10%	V_{DD}=5.0V±10%
V_{IH}	0.8V_{DD}	0.8V_{DD}
V_{IL}	0.2V_{DD}	0.2V_{DD}

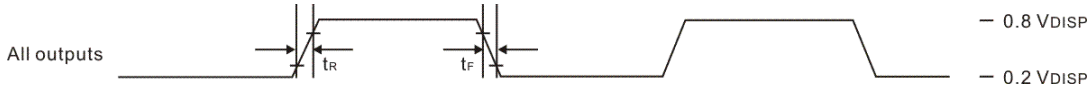
DATA TIMING



RESET TIMING

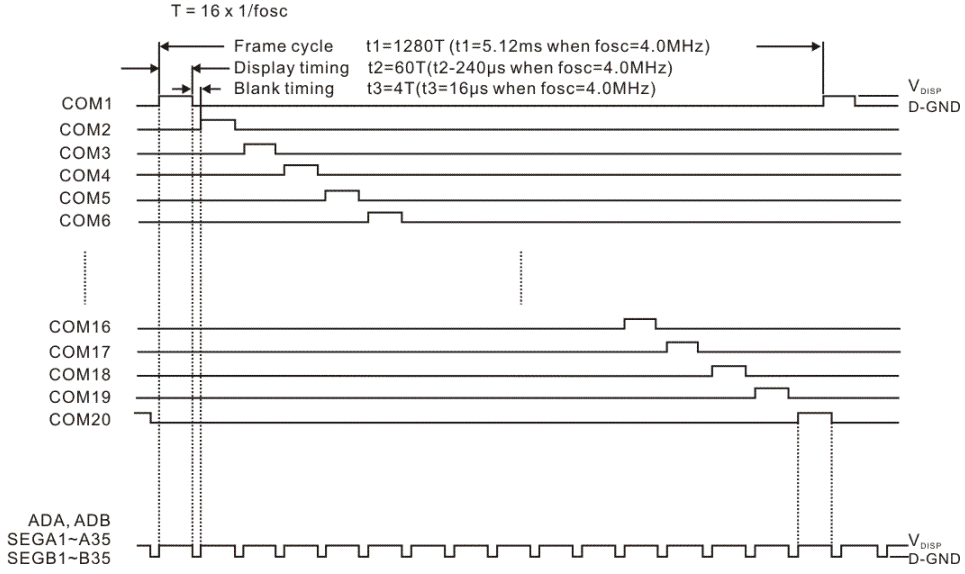


HIGH VOLTAGE OUTPUT TIMING



DIGIT OUTPUT TIMING

(for 20-digit display, at a duty of 960/1024)



ROM CODE

PT6301-001 (EUROPEAN)

PT6301-002 (KATAKANA)

PAD CONFIGURATION

Chip size: X=2.50mm, Y=10.14mm

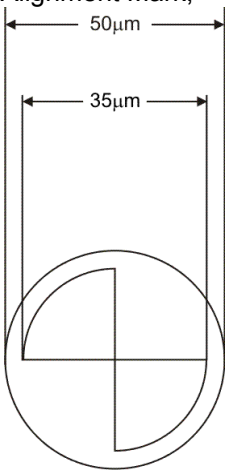
Chip thickness: 280μm

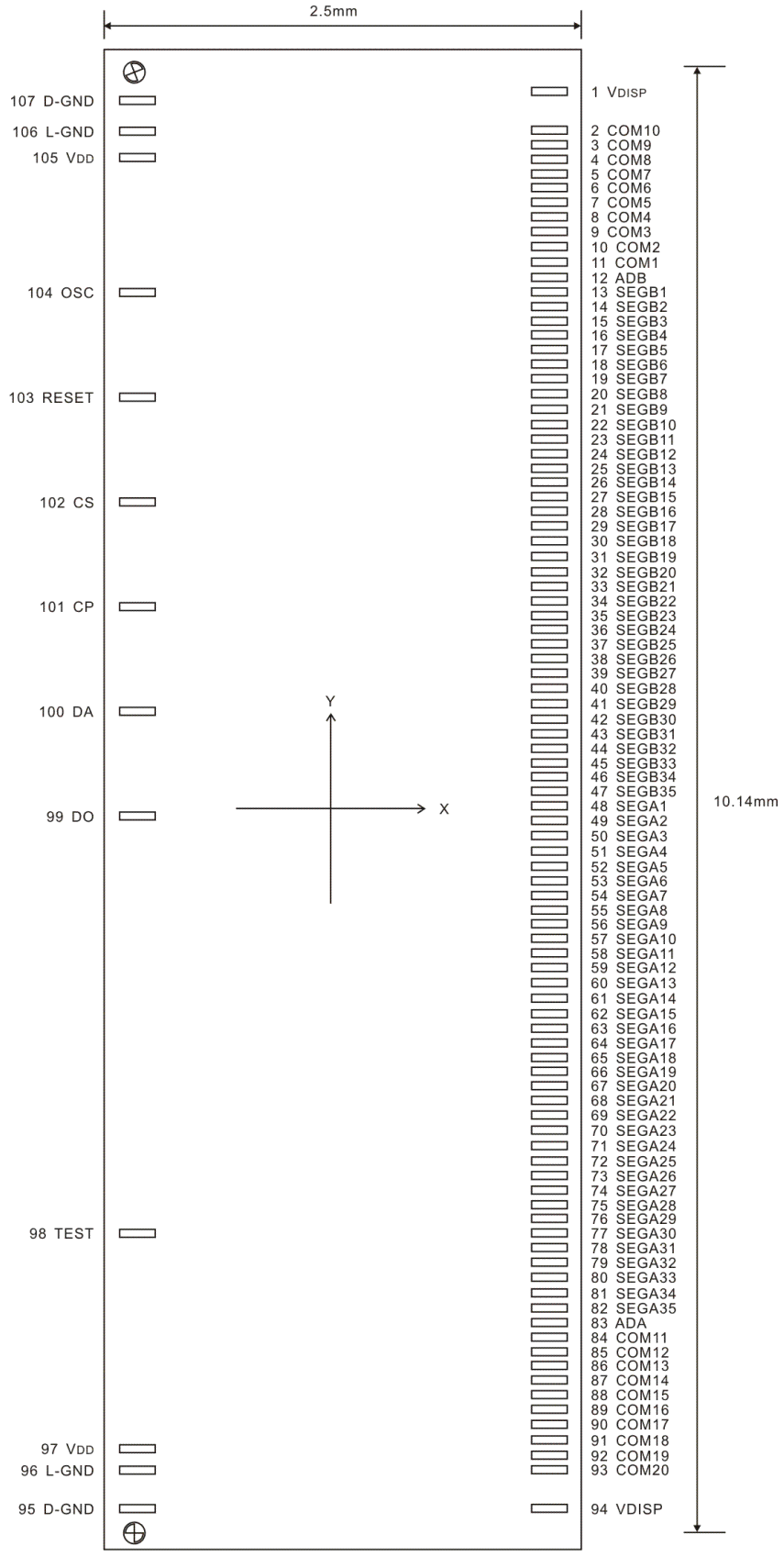
PAD size
- Driver output: X=90μm, Y=60μm
(SEGA1 to 35, SEGB1 to 35, ADA, ADB, COM1 to 20)

- Logic input/output: X=90μm, Y=65μm
(DA, CS, CP, RESET, OSC0, DO, TEST)

- Power: X=90μm, Y=80μm
(V_{DD}, L-GND, V_{DISP}, D-GND)

Alignment Mark;





PAD LOCATION

(unit: μm)

Pad No.	Pad Name	X	Y
1	VDISP	1110	4900
2	COM10	1110	4615
3	COM9	1110	4495
4	COM8	1110	4375
5	COM7	1110	4255
6	COM6	1110	4135
7	COM5	1110	4015
8	COM4	1110	3895
9	COM3	1110	3775
10	COM2	1110	3655
11	COM1	1110	3535
12	ADB	1110	3415
13	SEGB1	1110	3105
14	SEGB2	1110	3015
15	SEGB3	1110	2925
16	SEGB4	1110	2835
17	SEGB5	1110	2745
18	SEGB6	1110	2655
19	SEGB7	1110	2565
20	SEGB8	1110	2475
21	SEGB9	1110	2385
22	SEGB10	1110	2295
23	SEGB11	1110	2205
24	SEGB12	1110	2115
25	SEGB13	1110	2025
26	SEGB14	1110	1935
27	SEGB15	1110	1845
28	SEGB16	1110	1755
29	SEGB17	1110	1665
30	SEGB18	1110	1575
31	SEGB19	1110	1485
32	SEGB20	1110	1395
33	SEGB21	1110	1305
34	SEGB22	1110	1215
35	SEGB23	1110	1125
36	SEGB24	1110	1035
37	SEGB25	1110	945
38	SEGB26	1110	855
39	SEGB27	1110	765
40	SEGB28	1110	675
41	SEGB29	1110	585
42	SEGB30	1110	495
43	SEGB31	1110	405
44	SEGB32	1110	315
45	SEGB33	1110	225
46	SEGB34	1110	135
47	SEGB35	1110	45
48	SEGA1	1110	-45
49	SEGA2	1110	-135
50	SEGA3	1110	-225
51	SEGA4	1110	-315
52	SEGA5	1110	-405
53	SEGA6	1110	-495
54	SEGA7	1110	-585

Pad No.	Pad Name	X	Y
55	SEGA8	1110	-675
56	SEGA9	1110	-765
57	SEGA10	1110	-855
58	SEGA11	1110	-945
59	SEGA12	1110	-1035
60	SEGA13	1110	-1125
61	SEGA14	1110	-1215
62	SEGA15	1110	-1305
63	SEGA16	1110	-1395
64	SEGA17	1110	-1485
65	SEGA18	1110	-1575
66	SEGA19	1110	-1665
67	SEGA20	1110	-1755
68	SEGA21	1110	-1845
69	SEGA22	1110	-1935
70	SEGA23	1110	-2025
71	SEGA24	1110	-2115
72	SEGA25	1110	-2205
73	SEGA26	1110	-2295
74	SEGA27	1110	-2385
75	SEGA28	1110	-2475
76	SEGA29	1110	-2565
77	SEGA30	1110	-2655
78	SEGA31	1110	-2745
79	SEGA32	1110	-2835
80	SEGA33	1110	-2925
81	SEGA35	1110	-3015
82	SEGA35	1110	-3105
83	ADA	1110	-3415
84	COM11	1110	-3535
85	COM12	1110	-3655
86	COM13	1110	-3775
87	COM14	1110	-3895
88	COM15	1110	-4015
89	COM16	1110	-4135
90	COM17	1110	-4255
91	COM18	1110	-4375
92	COM19	1110	-4495
93	COM20	1110	-4615
94	VDISP	1110	-4900
95	D-GND	-1110	-4860
96	L-GND	-1110	-4655
97	VDD	-1110	-3015
98	TEST	-1110	-2385
99	DO	-1110	-1575
100	DA	-1110	-765
101	CP	-1110	45
102	CS	-1110	855
103	RESET	-1110	1665
104	OSC	-1110	2475
105	VDD	-1110	3015
106	L-GND	-1110	4655
107	D-GND	-1110	4860
Alignment		-1115	4955
Alignment		-1115	-4955

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian, Taipei 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw