SIEMENS

ICs for Communications

Analog Line Interface Solution
ALIS V3

PSB 4595 Version 2.1
PSB 4596 Version 3.1

Product Overview 06.98

ALIS **Revision History:**		**Current Version: 06.98**
Previous Version:		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)

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Edition 06.98

This edition was realized using the software system FrameMaker®.

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1 Overview

ALIS V3 is a chip set used to connect analog phone lines to digital equipment such as fax machines. Its technology and design make it especially suitable for use throughout the world in:

- V.34 modems
- V.90 modems
- Fax machines

The ALIS V3 chip set is an ideal front end for modems and fax machines because these pieces of equipment have to convert digital information into analog signals and vice versa for communications via telephone lines. ALIS V3 bridges the gap between a digital data pump and an analog phone line.

Reliability in digital processing is much better than in analog communications. The new design of the ALIS V3 chip set has transferred processing that was previously done on the analog side across to the digital part. Digital filters ensure great precision and virtually no fluctuation. They also provide maximum autonomy between the filter blocks.

Many manufacturers are concerned that when standards change, they will have to update the hardware. The ALIS V3 chip set removes this concern by integrating as many setting options as possible on the digital side in the form of software algorithms. Should standards change, all that equipment manufacturers need to do to modify their equipment is download or enter new coefficients. For example, V.34 sampling rates, including 16 kHz, are fully programmable.

The use of digital filter processing in combination with software algorithms ensures excellent transmission performance and adaptability. The ALIS V3 chip set is adaptable worldwide. International coefficient sets can be downloaded to the ALIS V3 chip set to comply with all specifications throughout the world.

Previous equipment had to operate in conjunction with external components in order to comply with local stringent requirements for communications equipment. One of these requirements can be for isolation between the analog and the digital signals for example. In the past, this was achieved using transformers, but they were awkward and heavy. They were especially a problem on PC Cards in notebooks. ALIS V3 has built-in isolation in the interface between digital and analog signals. In this overview, this is referred to as the “capacitor interface”. The capacitor interface (patents pending) is an effective, light-weight solution which isolates digital from analog signals without a transformer. This also allows very flat frequency response over the entire voice band even at low frequencies.

The Data Access Arrangement (DAA) is no longer necessary as a number of separate components. Precision has not been lost but gained since more processing, such as equalization and gain adjustment, is now done by digital filters.

As a result of the Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) technology used, the linearity of the ALIS V3 chip set is limited only by second-order parasitic effects.

The components and functions are described in more detail in the other chapters of this overview but the key technical data is also briefly mentioned here. A complete list of features follows in the next chapter, “Features”.

The main components of ALIS V3 are:

- Data Access Arrangement (DAA)
- Coder /Decoder (Codec)
- Hybrid circuit

The technology used for the two chips is:

- PSB 4595 (analog) low-power 0.8µm BiCMOS
- PSB 4596 (digital) 0.35 µm CMOS

Siemens offers a range of reference and evaluation tools for the ALIS V3 chip set. For appropriate tools, please contact your nearest Siemens representative.

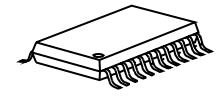
SIEMENS

Analog Line Interface Solution
ALIS

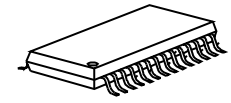
PSB 4595
PSB 4596

CMOS

1.1 Features



P-TSSOP24



P-TSSOP28

- The ALIS V3 chip set replaces the traditional Data Access Arrangement (DAA), codec and hybrid components.

- **International features:**
  Programmable ring detection: international levels, and frequency coefficients are downloadable
  Caller ID: detection, decoding and storage is now on-chip and programmable internationally
  Programmable international DC characteristics
  The ALIS V3 chip set complies with ETS 300 001, TBR21 and FCC requirements.

- **Modem features:**
  Programmable sampling rates in conformance with V.34, plus future-proof 16 kHz and 32 kHz sampling rates with one fixed master clock
  High performance analog-to-digital and digital-to-analog conversion
  Dual-line modem support
  Voice modem with speaker phone and handset support
  Output pin for line monitoring.

- Isolation by means of newly developed digital capacitor interface.

- Digital interface implemented with an interface processor; SIEMENS provides configuration support upon request.

Type	Ordering Code	Package
PSB 4595 V2.1		P-TSSOP24
PSB 4596 V3.1		P-TSSOP28

- Analog part powered from the Tip/Ring line by an integrated voltage regulator.
- Wake-up function to support PC power management, different operating modes (sleep, conversation, ring) to cut power consumption to a minimum.

- Two-chip solution: the P-TSSOP24 and P-TSSOP28 package is PC Card compliant.

- General purpose I/O pins.

- 3 V technology
  Output pins are TTL compatible
  Input pins are 5 V tolerant.

2 Block Diagram

For explanation of abbreviations, see “Pin Configuration and Definitions” on page 9

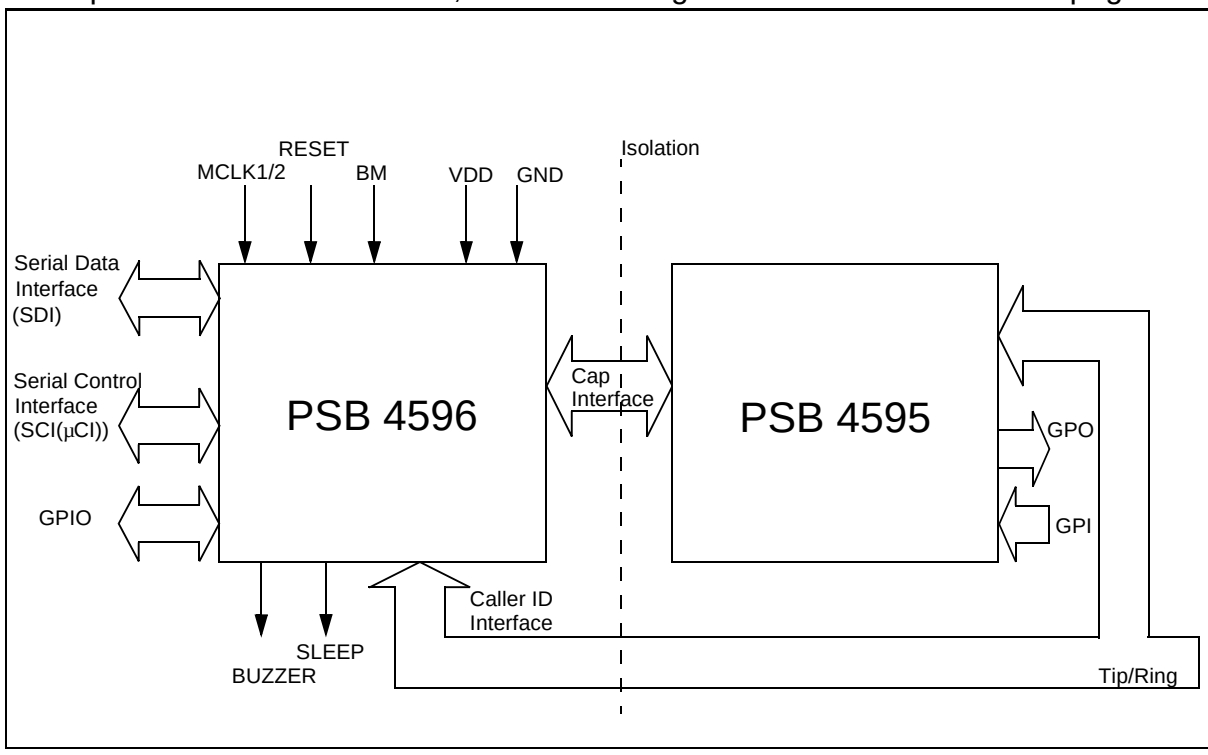


Figure 1 Block Diagram of the ALIS V3 Chip Set

The Block Diagram is described in more detail in the Functional Description.

3 Pin Configuration and Definitions

3.1 Pin Configuration

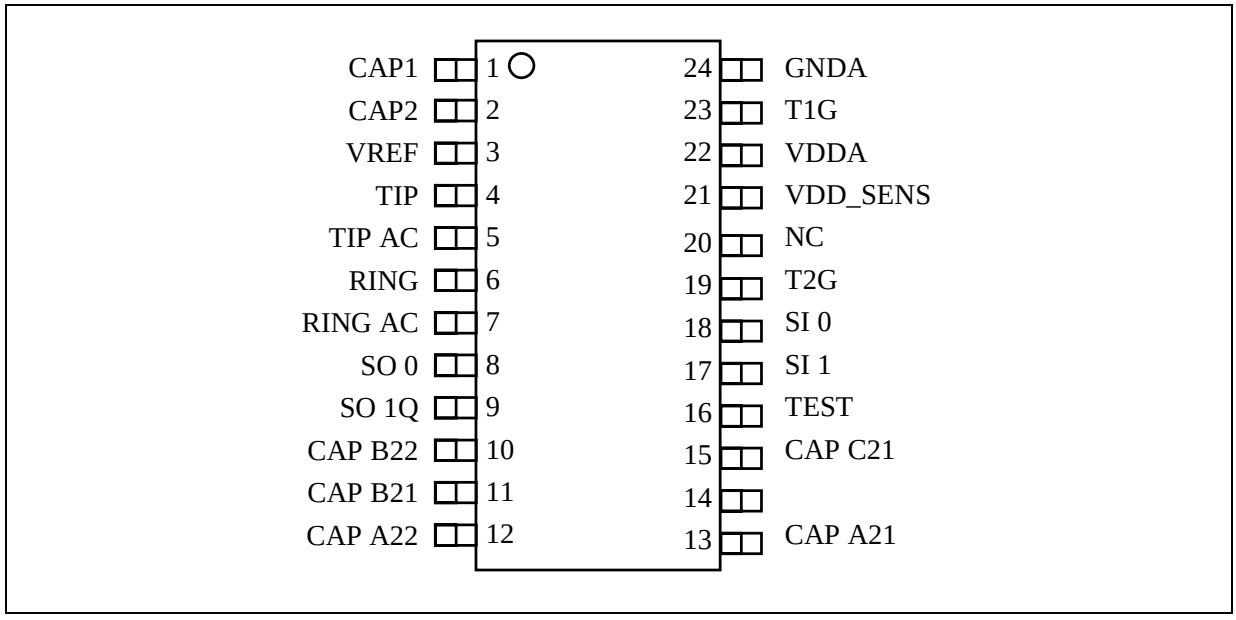


Figure 2 Pin Configuration of PSB 4595 (Top View)

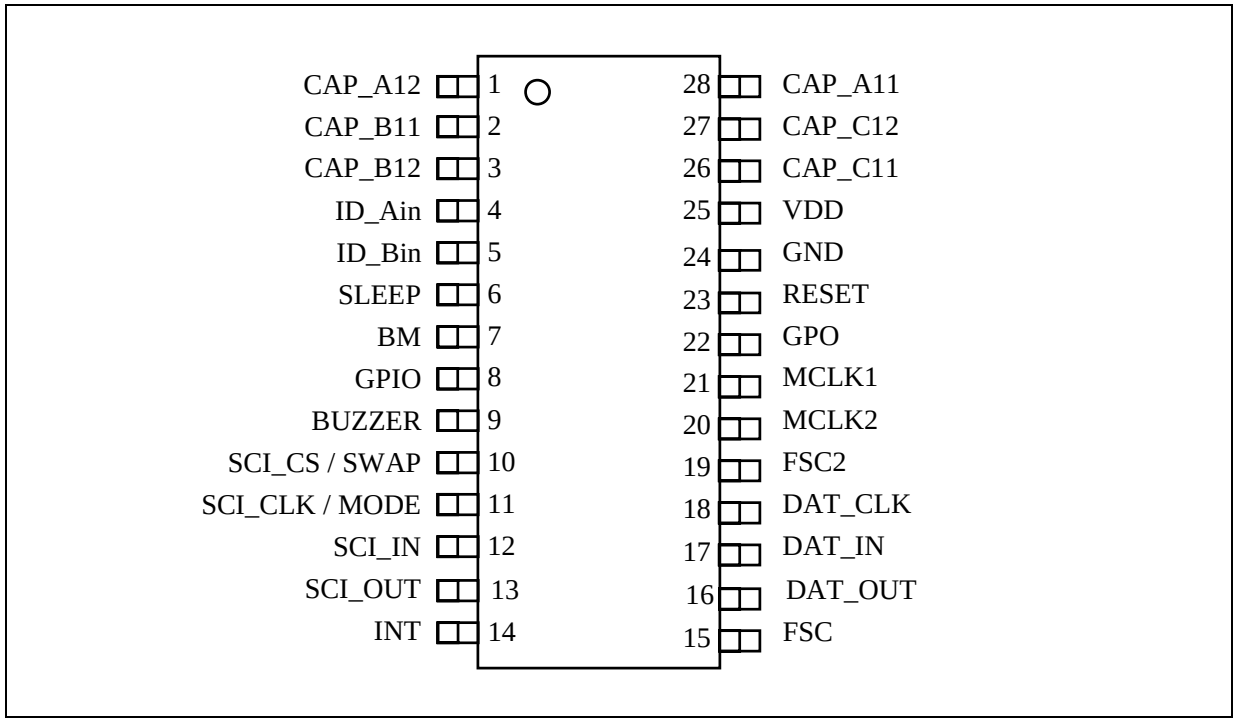


Figure 3 Pin Configuration of PSB 4596 (Top View)

3.2 Pin Definitions of PSB 4595

Table 1 PSB 4595 Pin Definitions

Pin No.	Symbol	Function	Descriptions
22	VDDA	Power	Programmable supply for the circuitry
24	GNDA	Power	Analog ground: all signals are referenced to this pin
4	TIP	I	Tip AC + DC sense input
5	TIP_AC	I	Tip AC sense input
6	RING	I	Ring AC + DC sense input
7	RING_AC	I	Ring AC sense input
23	T1G	O	Gate for external transistor T1 (AC/DC control)
19	T2G	O	Gate for external transistor T2 (VDDA control)
21	VDD_SENS	I	VDDA sense input
3	VREF	I/O	Reference voltage: must be connected to GNDA via an external capacitor of more than 10 nF (typ. 15 nF)
1	CAP1	I/O	Pin for external capacitor of more than 1 µF for DC filtering to pin CAP2
2	CAP2	I/O	See CAP1
18	SI_0	I	Auxiliary input pin 0
17	SI_1	I	Auxiliary input pin 1
8	SO_0	O	Auxiliary output pin 0
9	SO_1Q	O	Auxiliary output pin 1
16	TEST	I	Must be connected permanently to GNDA.
13	CAP_A21	I	Must be connected via a capacitor of more than 5pF to CAP_A11 (PSB 4596).
12	CAP_A22	I	Must be connected via a capacitor of more than 5pF to CAP_A12 (PSB 4596).
11	CAP_B21	O	Must be connected via a capacitor of more than 5pF to CAP_B11 (PSB 4596).

Table 1 PSB 4595 Pin Definitions

Pin No.	Symbol	Function	Descriptions
10	CAP_B22	O	Must be connected via a capacitor of more than 5pF to CAP_B12 (PSB 4596)
15	CAP_C21	I	Must be connected via a capacitor of more than 5pF to CAP_C11(PSB 4596).
14	CAP_C22	I	Must be connected via a capacitor of more than 5pF to CAP_C12 (PSB 4596).
20	NC		Not Connected.

3.3 Pin Definitions of PSB 4596

Table 2 PSB 4596 Pin Definitions

Pin No.	Symbol	Function	Description
25	VDD	Power	+3.3 Volt supply for the digital circuitry.
24	GND	Power	Ground digital: all signals are referenced to this pin.
21	MCLK1	I	Master Clock1: one pin of a 16.384-MHz-to-50-MHz crystal is connected. This pin can also be driven by an external clock.
20	MCLK2	O	Master Clock2: other pin of crystal is connected. When MCLK1 is driven by an external clock, this pin should be left open.
23	RESET	I	Reset input: resets the device (low active).
15	FSC	IO	As input: Frame Synchronization Clock, identifies the beginning of the frame, FSC must be synchronous with DAT_CLK. As output: indicates the beginning of a new frame.
17	DAT_IN	I	Serial Data Interface (SDI) : receive data Parallel Mode:16-bit line data MUX Mode: 16-bit line data plus 16-bit control data every FSC.

Table 2 PSB 4596 Pin Definitions

Pin No.	Symbol	Function	Description
16	DAT_OUT	O	Serial Data Interface (SDI) : transmit data, tristate if not active Parallel Mode: 16-bit line data MUX Mode: 16-bit line data plus 16-bit control data every FSC.
18	DAT_CLK	IO	Data clock 256 to 2048 kHz: determines the rate at which data is transferred to and from the serial data interface (SDI).
19	FSC2	O	Second FSC to synchronize slave devices.
14	INT	O	Interrupt output pin (open drain, low active).
7	BM	I	Bus Master pin (master or slave mode). '1' at the rising edge of RESET activates Master Mode.
6	SLEEP	O	Indicates that PSB 4596 is in the Deep Sleep Mode.
11	SCI_CLK/ MODE	I	Serial Control Interface (SCI): clock for control data. '1' at the rising edge of RESET activates MUX Mode.
10	SCI_CS/ SWAP	I	Parallel Mode: Serial Control Interface (SCI): chip select MUX Mode: to swap 16-bit control data with 16-bit line data.
12	SCI_IN	I	Serial Control Interface (SCI): receive control data from the µC/DSP (not used in MUX Mode).
13	SCI_OUT	O	Serial Control Interface (SCI): transmit control data to the µC/DSP (not used in MUX Mode).
4	ID_Ain	I	Input for Caller ID comparator A (connection to TIP).
5	ID_Bin	I	Input for Caller ID comparator B (connection to RING).
9	BUZZER	O	Output for line monitoring.

Table 2 PSB 4596 Pin Definitions

Pin No.	Symbol	Function	Description
28	CAP_A11	O	Must be connected via a capacitor of more than 5pF to CAP_A21 (PSB 4595).
1	CAP_A12	O	Must be connected via a capacitor of more than 5pF to CAP_A22 (PSB 4595).
2	CAP_B11	I	Must be connected via a capacitor of more than 5pF to CAP_B21 (PSB 4595).
3	CAP_B12	I	Must be connected via a capacitor of more than 5pF to CAP_B22 (PSB 4595).
26	CAP_C11	O	Must be connected via a capacitor of more than 5pF to CAP_C21 (PSB 4595).
27	CAP_C12	O	Must be connected via a capacitor of more than 5pF to CAP_C22 (PSB 4595).
22	GPO	O	General purpose output pin. (e.g. to control the hook switch)
8	GPIO	IO	General purpose I/O pin.

Note: All unused input pins should be connected either to GND or VDD

4 Typical Applications

As mentioned in the introduction, the ALIS V3 chip set is typically implemented in modems and fax machines.

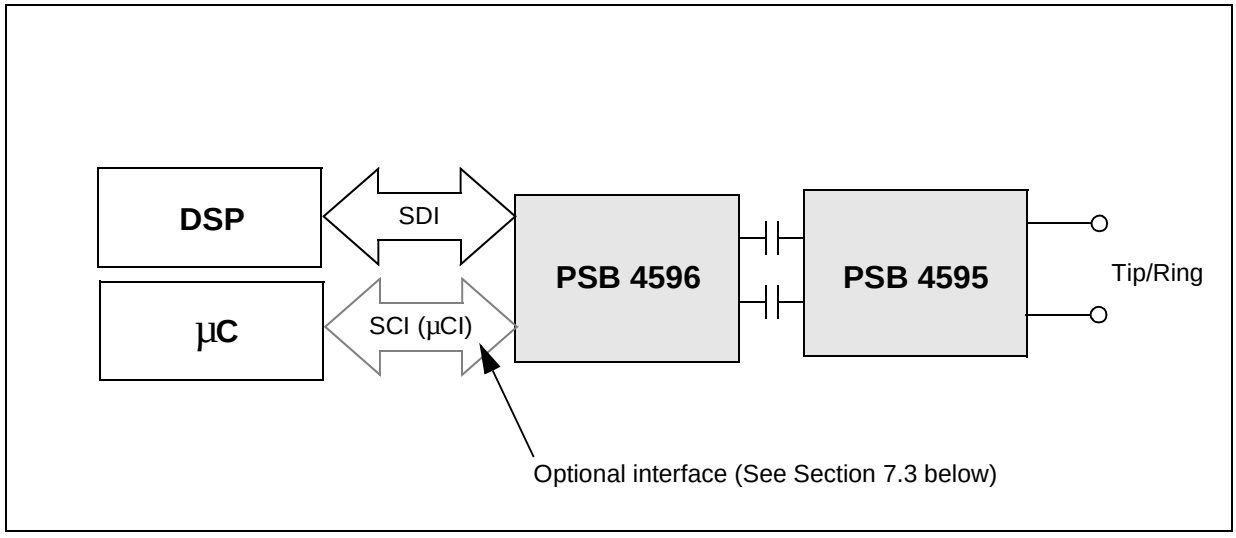
We present below four different types of modem where the ALIS V3 chip set is an ideal solution:

- DSP-based modem (V.34, V.90)
- Host-based software modem (V.34, V90 on the host)
- Hybrid modem
- Modem with speaker path

In all the typical implementations, the innovative capacitor interface renders a transformer redundant, cutting weight and space requirements in the modems.

4.1 The ALIS V3 Chip Set with Digital Signal Processor(DSP)-based Modem

The ALIS V3 chip set forms the front end between a DSP-based modem and the Tip/ Ring line.



Legend:
SDI: Serial Data Interface
SCI: Serial Control Interface (= µCI: Microcontroller Interface)

Figure 4 DSP-based Modem Application

The DSP data pump is both source and destination of digital signals which are transferred to and from the digital chip PSB 4596 via the Serial Data Interface (SDI) and Serial Control Interface (SCI). The optional SCI enables external control of the ALIS V3 chip set (see also Section 7.3 below). The SCI gives transparent access to ALIS V3 commands and signaling pins so that precalculated coefficient sets can be downloaded

from the system to the on-chip coefficient RAM (CRAM, located in the DSP) to program the filters.

Digital signals are then converted by oversampling converters to analog signals. Oversampling converters ensure the required conversion accuracy. The converted signals are applied to the capacitor interface which transfers them to the analog chip PSB4595 and thus to the Tip/Ring wires in the telephone line. Since the capacitor interface means there is no longer a transformer, it is now possible to achieve a very flat frequency response over the entire voice band, even at low frequencies.The process is reversed for incoming analog signals from the Tip/Ring wires.

4.2 The ALIS V3 Chip Set with Host-based Software Modem

The ALIS V3 chip set can also be used as a front end between V.34 and V.90 software modem applications running on a host and the Tip/Ring wires in a telephone line.

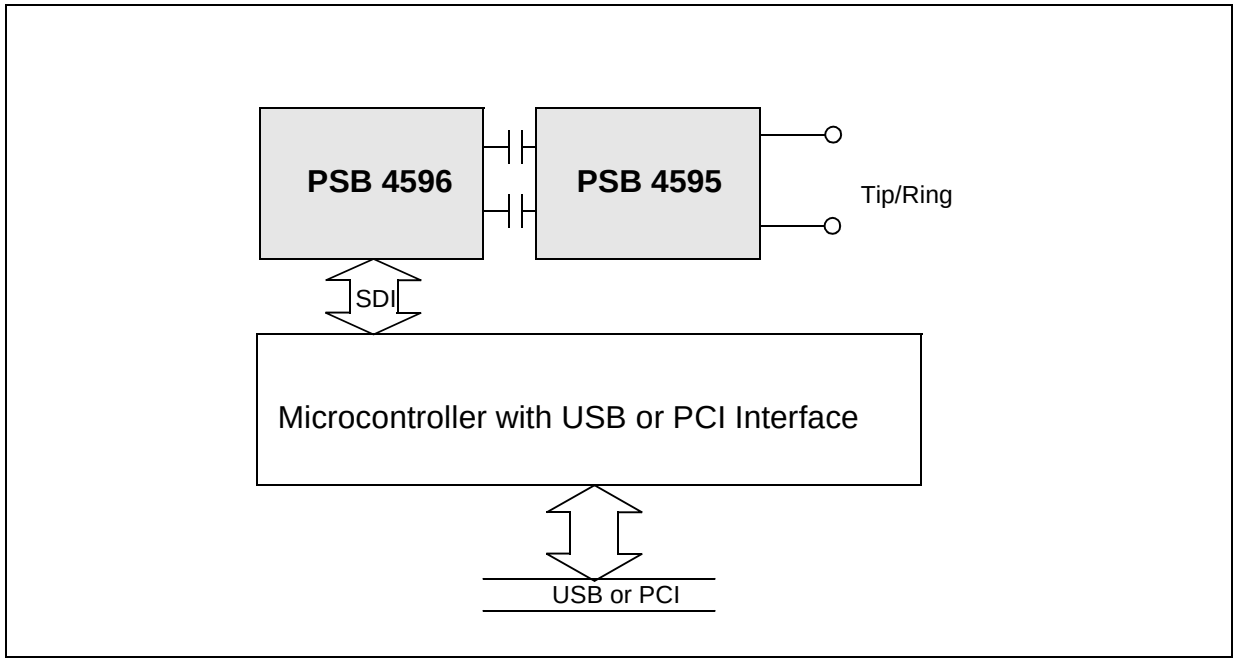


Figure 5 Software Modem Application

The digital signals travel on the USB or PCI bus and then via a FIFO structure to an SDI which carries signals to and from the digital chip PSB 4596. The digital signals are then converted by oversampling converters, as above for a DSP-based modem, and on to the Tip/Ring wires in the telephone line. The process is reversed for incoming analog signals from the Tip/Ring wires.

4.3 Hybrid Modem (ISDN plus Analog)

The ALIS V3 chip set can be combined with a ISDN chip set to support hybrid modems, with both Tip/Ring and ISDN (S- or U-interface) connections.

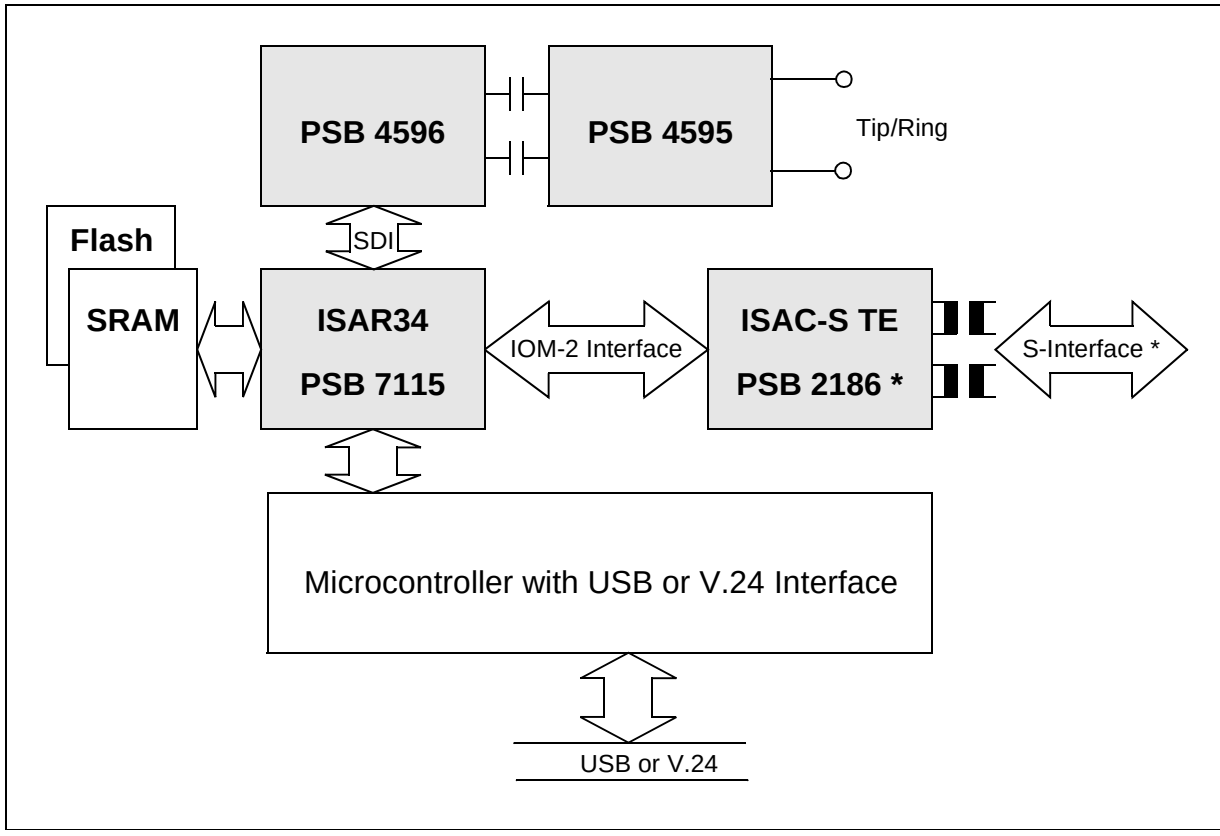


Figure 6 Hybrid Modem Application, with ISDN S-Interface

The example above is shown with the ISAR34 Enhanced Data Access Controller (PSB 7115) and the ISAC-S TE ISDN Access Controller (PSB 2186) for an S-bus.

Note: If you use an ISDN U-Interface instead of an ISDN S-Interface, you must change over the ISDN chips. Replace chip ISAC-S TE PSB 2186 with IEC-Q TE PSB 2191.

4.4 Modem plus Speaker Phone

The ALIS V3 chip set could be applied as the front end for a modem plus speaker phone.

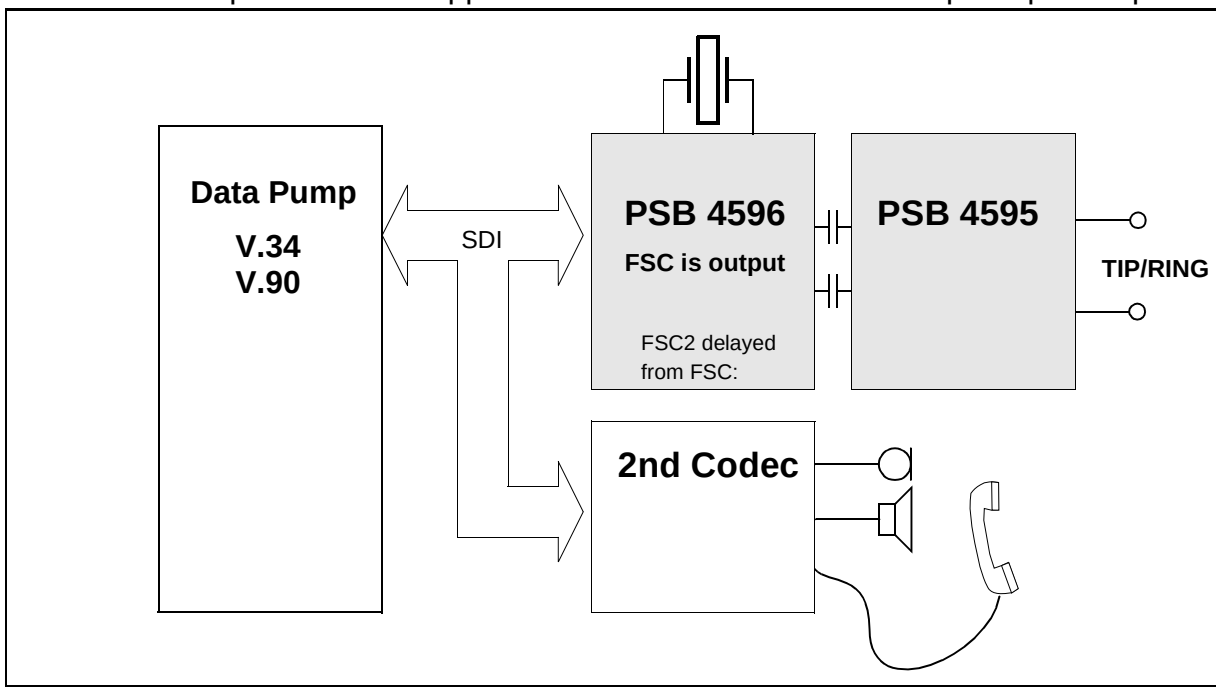


Figure 7 Application with Speaker Phone

The example here includes an 2nd Codec connected on the same SDI as the PSB 4596. This Codec is synchronised by the FSC2 (further explanation see section “Host Interface” on page 22).

5 Functional Description

The functional description consists of a block diagram with explanation of the building blocks followed by a description of the chip set's basic principles of operation.

5.1 Functional Block Diagram

The chip set consists of two chips, PSB 4595 and PSB 4596. The following illustration shows the main building blocks:

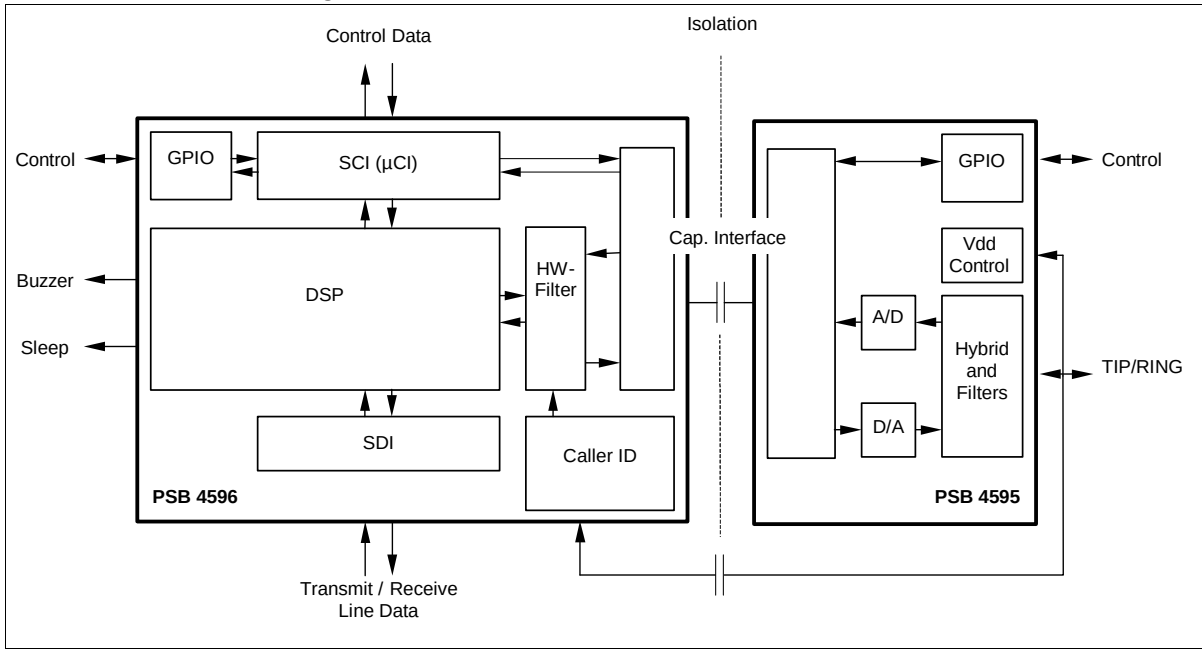


Figure 8 Functional Block Diagram of the PSB 4596/4595 Chip Set

At PSB 4595 (on the right of the diagram), the Tip/Ring line interfaces with:

VDD Control: this sets the level of the supply voltage for the PSB 4595. The level is selected via a program.
Hybrid and Filters: the hybrid provides two-wire to four-wire conversion, and the analog anti-aliasing pre-filters and smoothing post-filters provide signal conditioning.
The line data path is routed from the filters to the capacitor interface through the **Analog-to-Digital** (A/D) or the **Digital-to-Analog** (D/A) converters. These are over-sampling converters, to ensure the required conversion accuracy.
Capacitor Interface isolates PSB 4596 from PSB 4595.
There are two pairs of general purpose **I/Os** (GPIOs) at PSB 4595.

At PSB 4596, the Tip/Ring interfaces through two capacitors to the **Caller ID** input pins.

The **hardware filters** (HW Filter) handle interpolation and decimation for both Caller ID and data, before these signals travel to the digital filter structure (located in the DSP) which does equalization, gain adjustment, impedance matching, and other DAA

functions, in accordance with the downloaded coefficient set.
Transmit and Receive data are transferred between the PSB 4596 and the data pump through the Serial Data Interface (**SDI**).
The Serial Control Interface (**SCI)** allows external control of the ALIS V3 features and provides transparent access to ALIS V3 commands and signaling pins, so that pre-calculated coefficient sets can be downloaded from the system to the on-chip Coefficient RAM (CRAM, located in the DSP) to program the filters.
There is one General Purpose Output pin (**GPO**) to control the hook switch and one General Purpose IO (**GPIO**) pin.
The SLEEP pin indicates that the PSB 4596 is in the Sleep Mode.
With the BUZZER pin an external Buzzer can be connected to monitor the TIP/RING line.

5.2 Basic Functionality

5.2.1 Receiving and Transmitting Data

The analog voltage at Tip/Ring is converted to a 1-bit data stream in the ADC (line data). After decimation in hardware filters, the line data passes to a programmable filter structure in a DSP. These filters are programmable to international standards by downloading different national sets of coefficients. The line data is then transferred to the SDI.
When transmitting the line data to the SDI, it is also processed by programmable filters for the different national requirements before it is interpolated in a hardware filter structure and converted to an analog signal by the D/A converter.

5.2.2 Input Impedance

The input impedance is also generated digitally. On the Tip/Ring side, ALIS V3 applies voltage sensing and current feeding. There is a feedback loop between the receive and the transmit path to synthesize input impedance. This means the digitized voltage is multiplied by a transfer function, converted back to analog and fed back as a current to the line. This transfer function synthesizes the ALIS V3 input impedance.

5.2.3 Caller ID

The Caller ID receiver meets Bellcore specifications TR-NWT-000030 and SR-TSV-002476 for Caller IDs. In this service, the calling party’s information (Calling Line Identification Presentation (CLIP)) is transmitted in the silent interval between the first and second ring. The ALIS V3 receives and stores up to 64 bytes of the 1200 baud FSK signal in a dual-paged buffer. The de-coding scheme meets the Bell 202 and ITU-T V.23 specifications.

6 Interfaces Overview

6.1 Clocking

Any master clock frequency within the range 16.384 MHz to 50 MHz can be input to PSB 4596. Siemens recommends a a clock frequency of 24.567 MHz.

6.2 Sampling Frequency

The sampling frequency can be programmed within the range 7.2 kHz to 16 kHz, accurate to less than 1 Hz. When programming different sampling frequencies, the pass-band behavior will also change relative to the frequency.
The diagrams below show this behavior for three example sample frequencies of 7200 Hz, 8000 Hz and 9600 Hz. (High-pass filter enabled).

Note: In V.90 modem applications, the 50/60 Hz high-pass filter can be turned off.

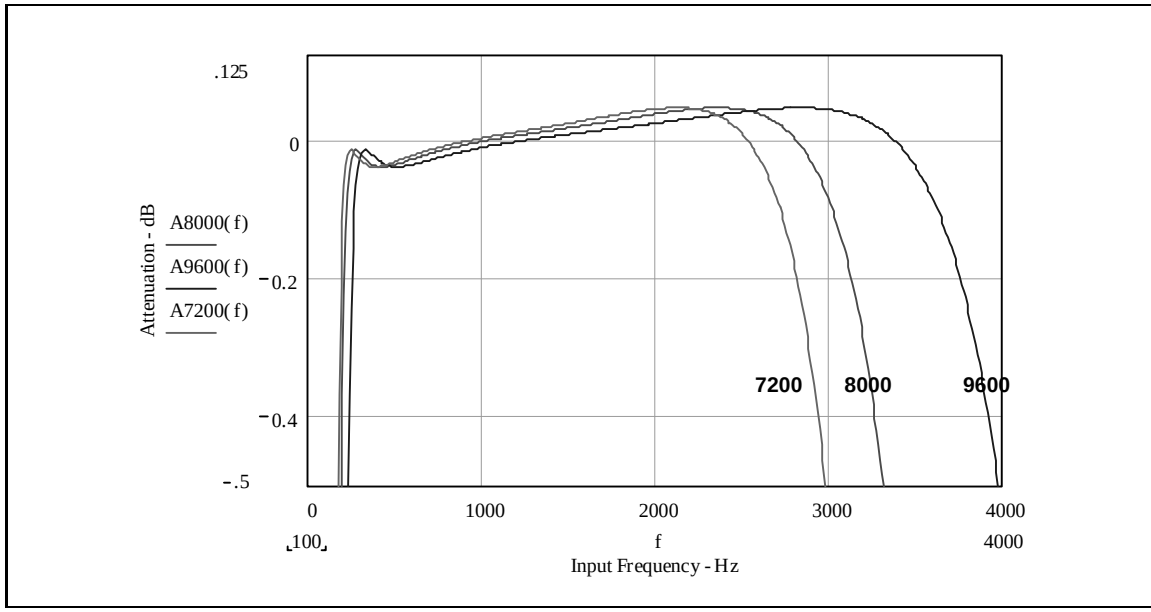


Figure 9 Receive Filter Passband Ripple

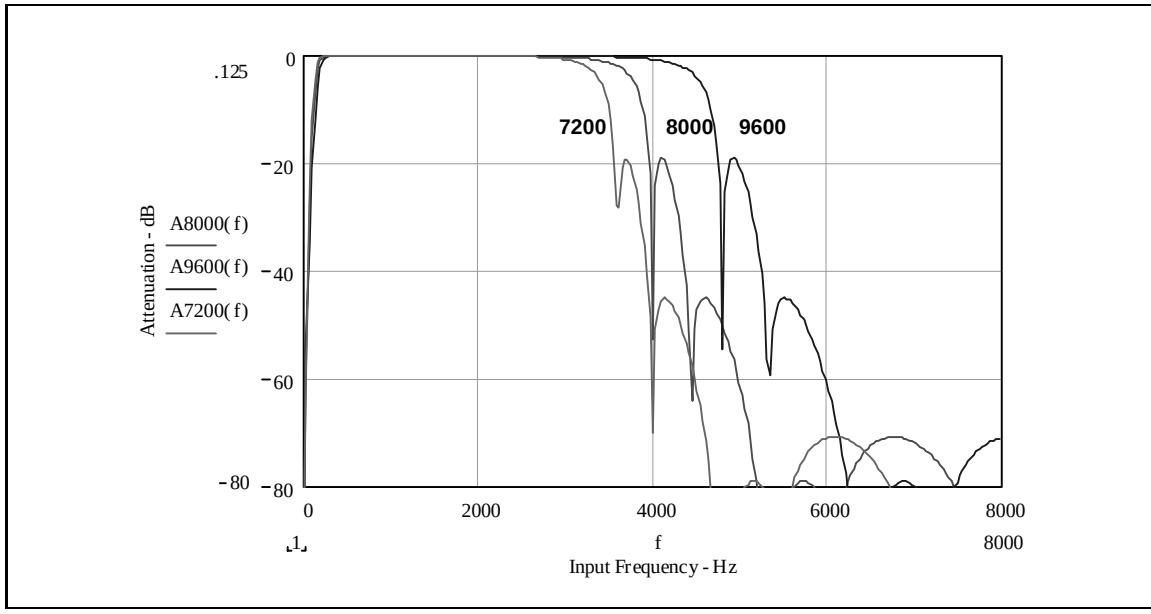


Figure 10 Receive Filter Response

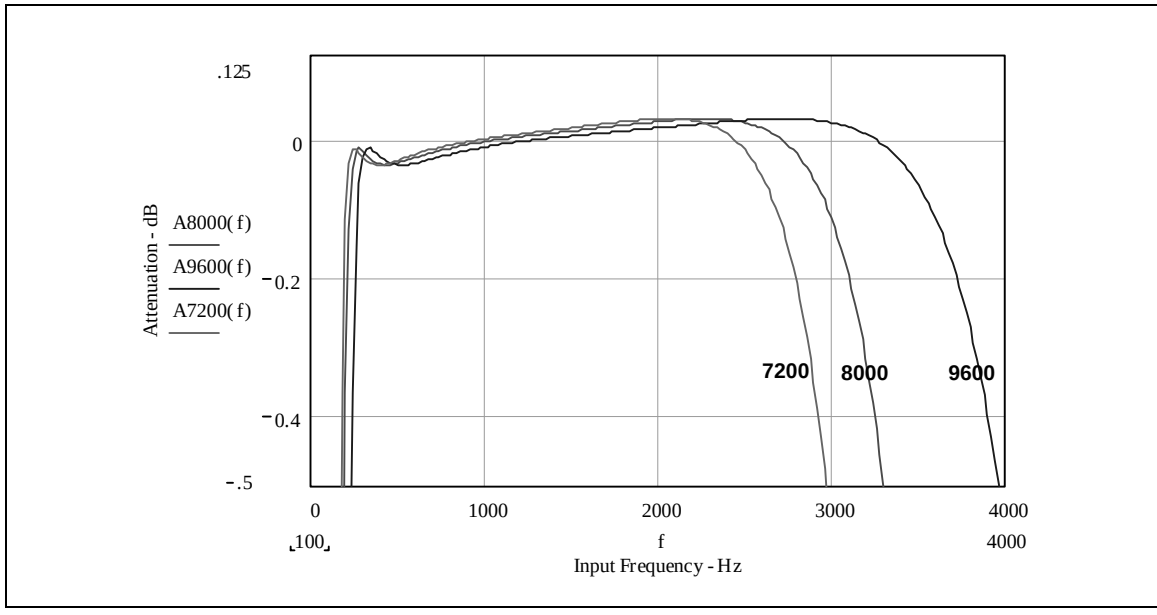


Figure 11 Transmit Filter Passband Ripple

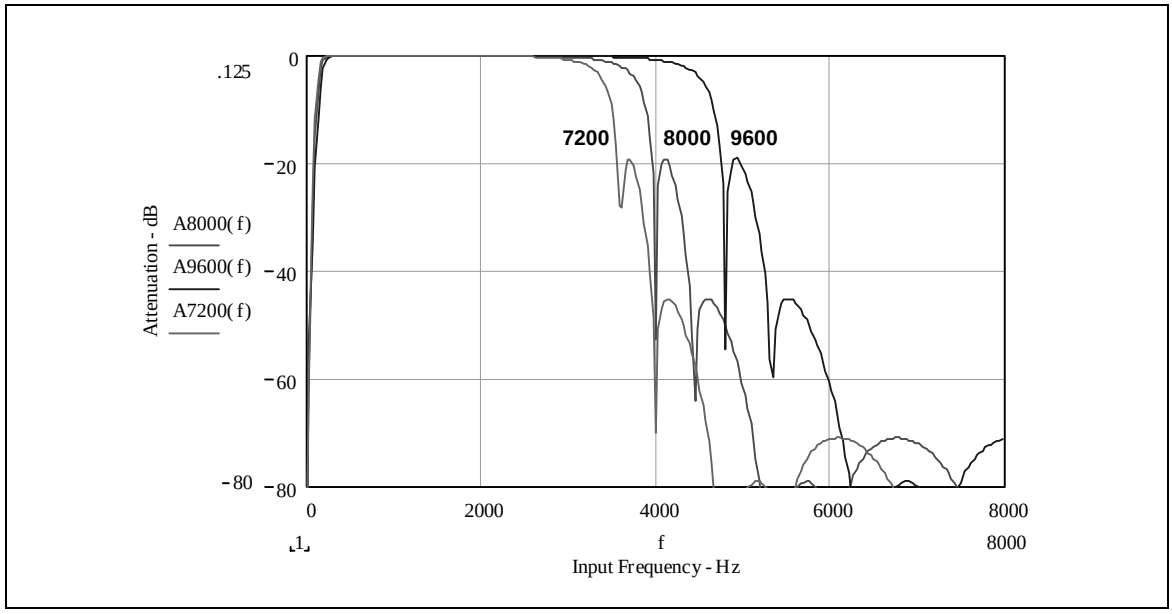


Figure 12 Transmit Filter Response

Note: The ALIS V3 chip set also can also be programmed to flatten gain down to 20 Hz by switching off the high pass and by using different coefficients

6.3 Host Interface

PSB 4596 uses 5 lines to communicate with the DSP. The direction of DAT_CLK and Frame Synchronization Clock (FSC) can be programmed by the Bus Master (BM) pin during RESET to become input or output. For modems using DSPs with embedded µC these lines are also used for control data.

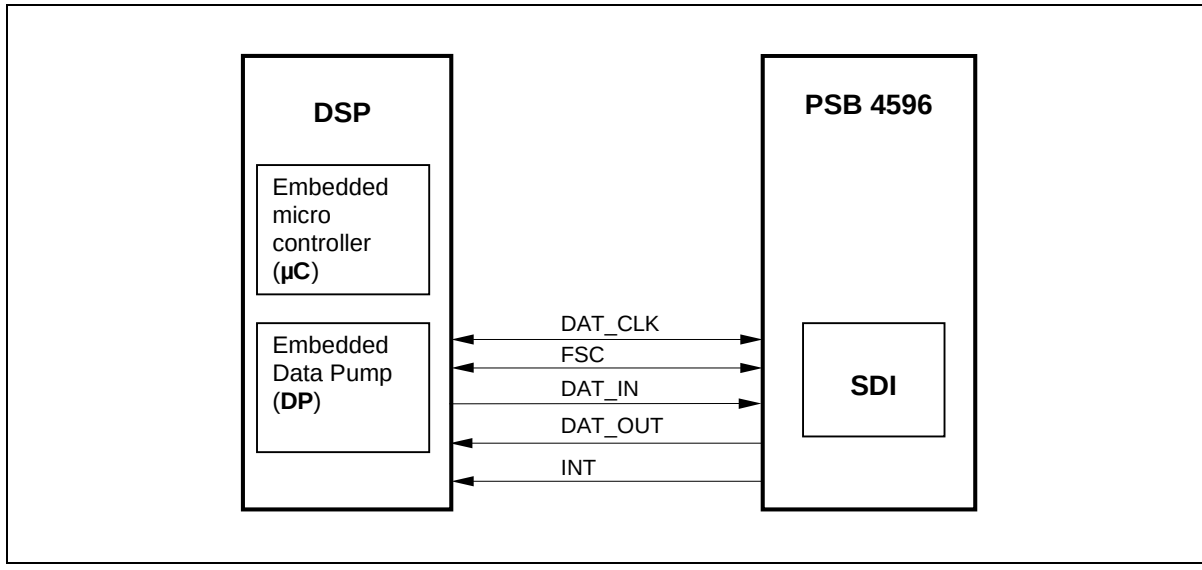


Figure 13 Connection to a DSP

For modems with an external µC, or for test purposes, PSB 4596 can be programmed to use different pins for control data and line data (Parallel Mode). In this mode, the control data is transferred via the Serial Control Interface (SCI) using 4 pins. The line data is transferred via the Serial Data Interface (SDI).

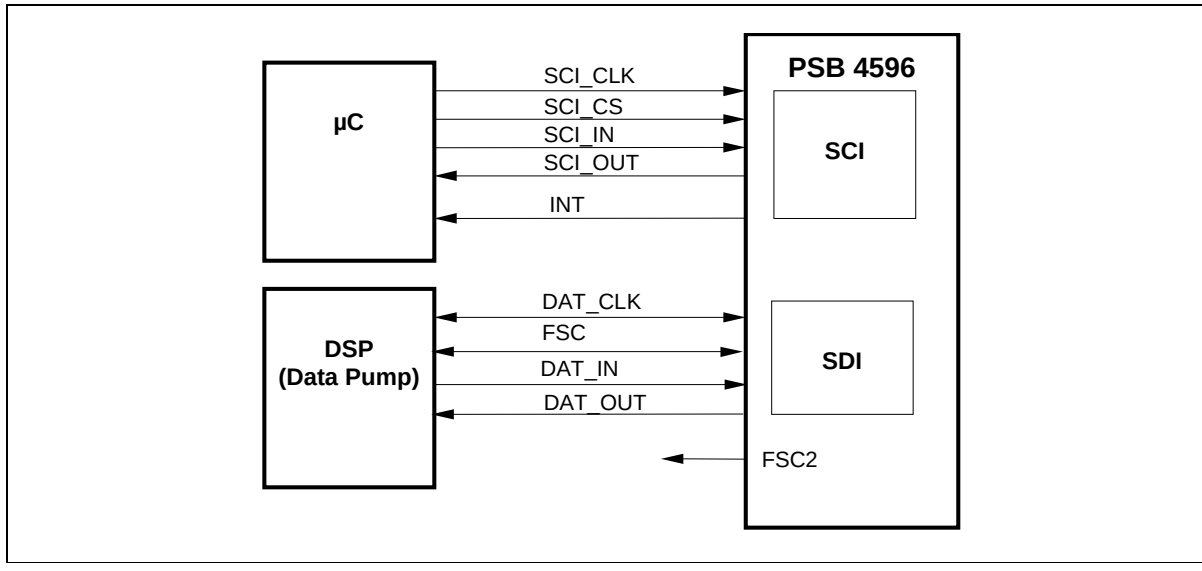


Figure 14 Connection to a DSP and a µC using Parallel Mode

PSB 4596 can be programmed to send out a secondary frame sync pulse (pin FSC2) to indicate to a 2nd device that communication at the SDI has ended. This sync pulse is high active with a duration of 1 DAT_CLK.

6.4 Connection to the Telephone Line

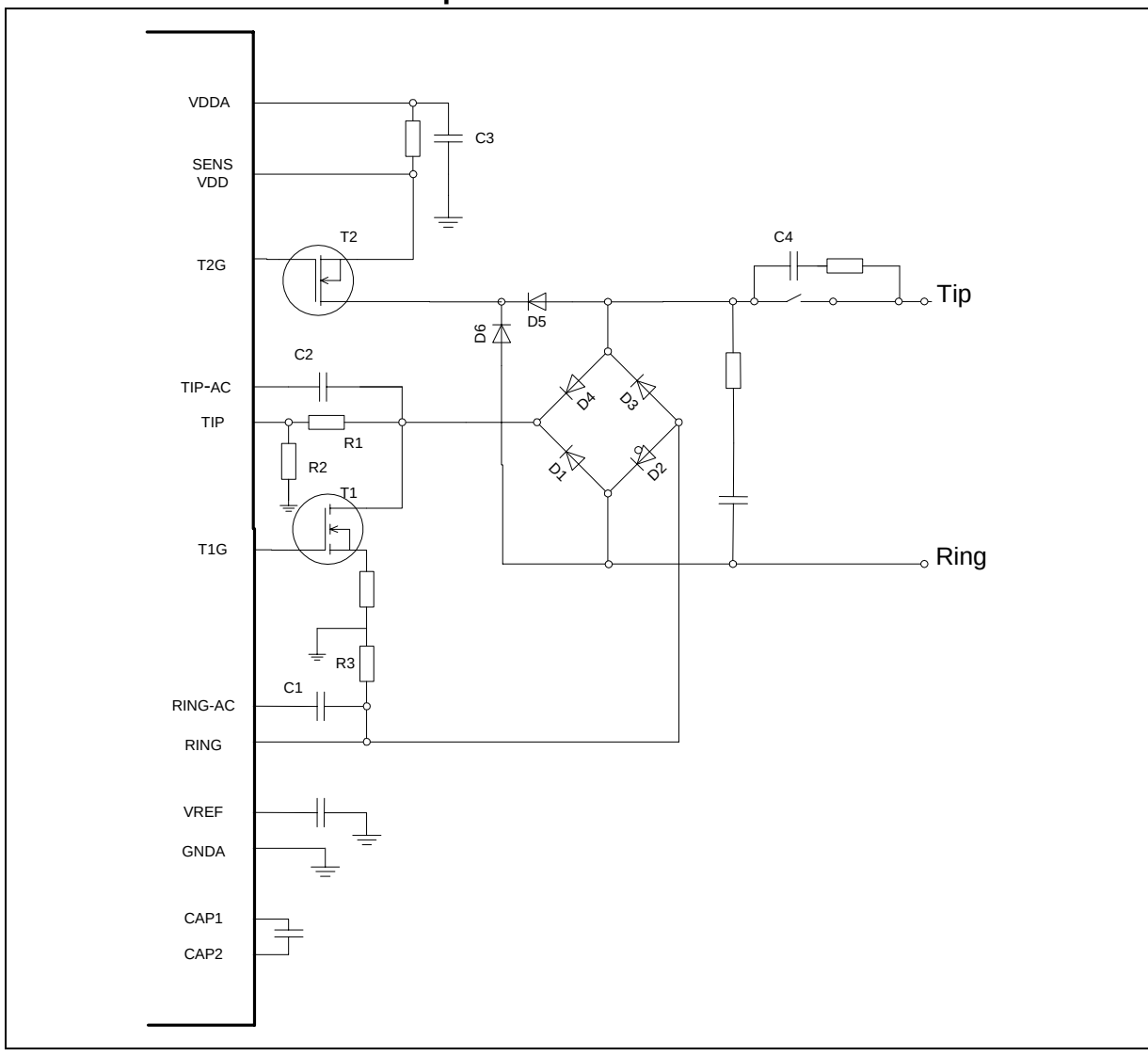


Figure 15 Connection of PSB 4595 to the Telephone Line

As shown in the figure, PSB 4595 requires minimum components to complete the DAA circuit:

- Bridge: using Schottky diodes D1, D2, D3, D4, D5 & D6 will improve the performance at low feeding conditions. Recommended: Dual Schottky diode SIEMENS BAT 240A.
- Resistors R1, R2 & R3 for current sensing.
- Capacitors C1 & C2 for AC coupling, C3 for VDD buffering and C4 as ring capacitor. Additional Capacitors for stabilizing.
- Two transistors T1 & T2 to handle the line current. T2 must be a depletion type to handle start-up. Recommended transistors: T1: SIEMENS BSP 88; T2: SIEMENS BSP 129.
- Components for EMC protection: not shown, depending on the board layout.

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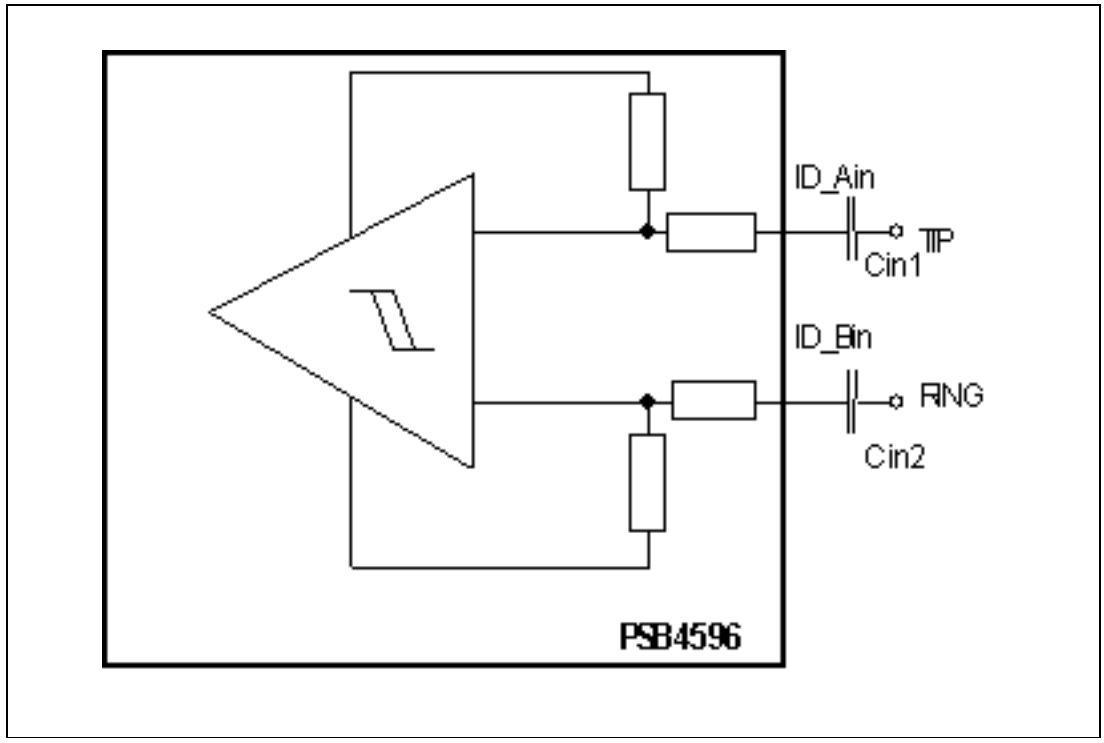
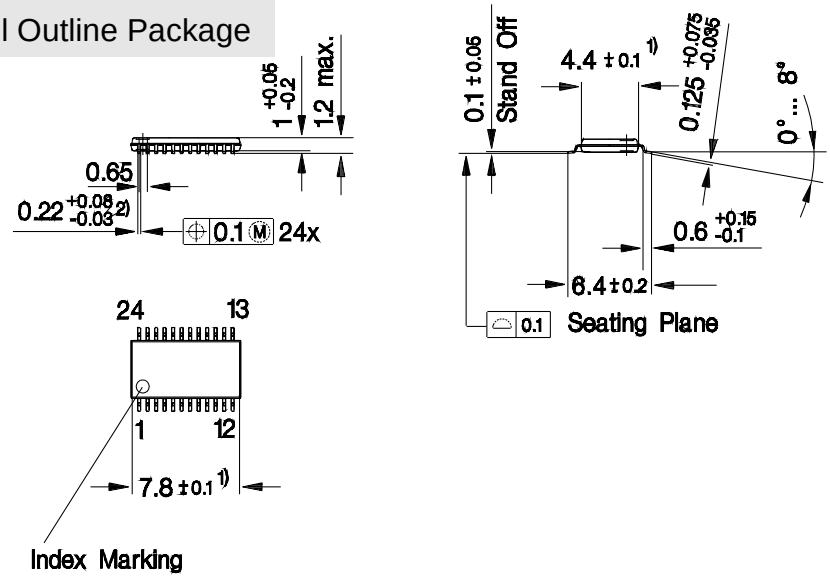


Figure 16 Caller-ID Interface Connection of the PSB 4596 to Tip/Ring

The PSB 4596 can optionally be connected to the Tip/Ring line to provide Caller-ID (CID) functions. The CID circuit requires two external capacitors.

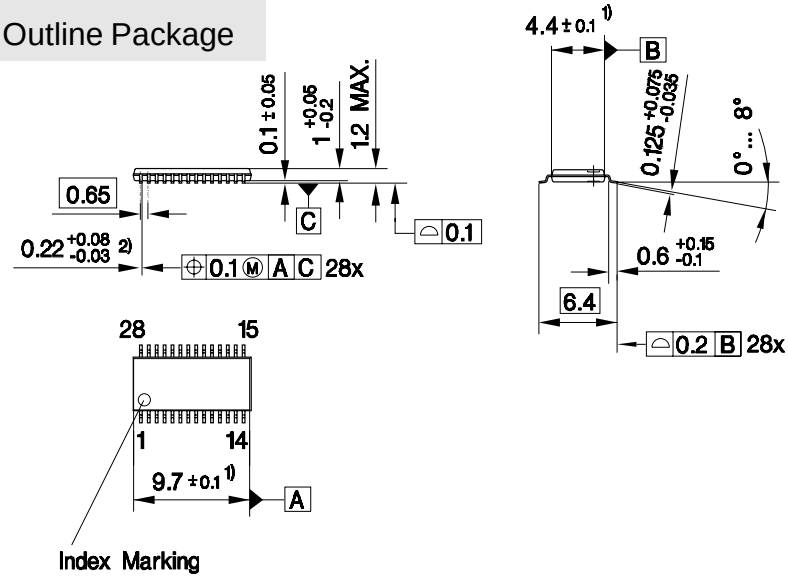
7 Package Outlines

P-TSSOP24 PSB 4595
(Plastic Thin Shrink Small Outline Package



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

P-TSSOP28 PSB 4596
(Plastic Thin Shrink Small Outline Package



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Packaging

Packaging outlines for tubes, trays etc. are found in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions are in mm

8 Glossary

ADC	Analog-to-Digital Converter
ALIS V3	Analog Line Interface Solution V3
CID	Caller ID
CODEC	Coder / Decoder
CRAM	Coefficient RAM
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processing
EMC	Electromagnetic Compatibility
ETS	European Telecommunication Standards
FCC	Federal Communications Commission
FIFO	First-In, First-Out
GPIO	General Purpose Input Output
MUX	Multiplexer
PCI	Peripheral Component Interface
PCM	Pulse Code Modulation
PC Card	Personal Computer Card (former PCMCIA)
SCI	Serial Control Interface (equivalent to µCI)
SDI	Serial Data Interface
TBR	Technical Bases for Regulation
VDD	Voltage Drain Drain
µCI	Microcontroller Interface (equivalent to SCI)

Please see also the abbreviations in the Pin Definition Tables.