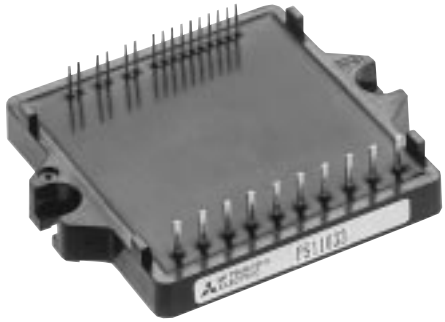
# PS11033

**FLAT-BASE TYPE**
**INSULATED TYPE**

## PS11033



### INTEGRATED FUNCTIONS AND FEATURES

- Converter bridge for 3 phase AC-to-DC power conversion.
- 3 phase IGBT inverter bridge configured by the latest 3rd. generation IGBT and diode technology.
- Inverter output current capability $I_O$ (Note 1):

| Type Name | Motor Rating | $I_O$ (100%) | $I_O$ (150%; 60sec) |
|---|---|---|---|
| PS11033 | 0.4 kW/200V AC | 3.0Arms | 4.5Arms |

(Note 1) : The inverter output current is assumed to be sinusoidal and the peak current value of each of the above loading cases is defined as : $I_{OP} = I_O \times \sqrt{2}$, $T_C < 100°C$

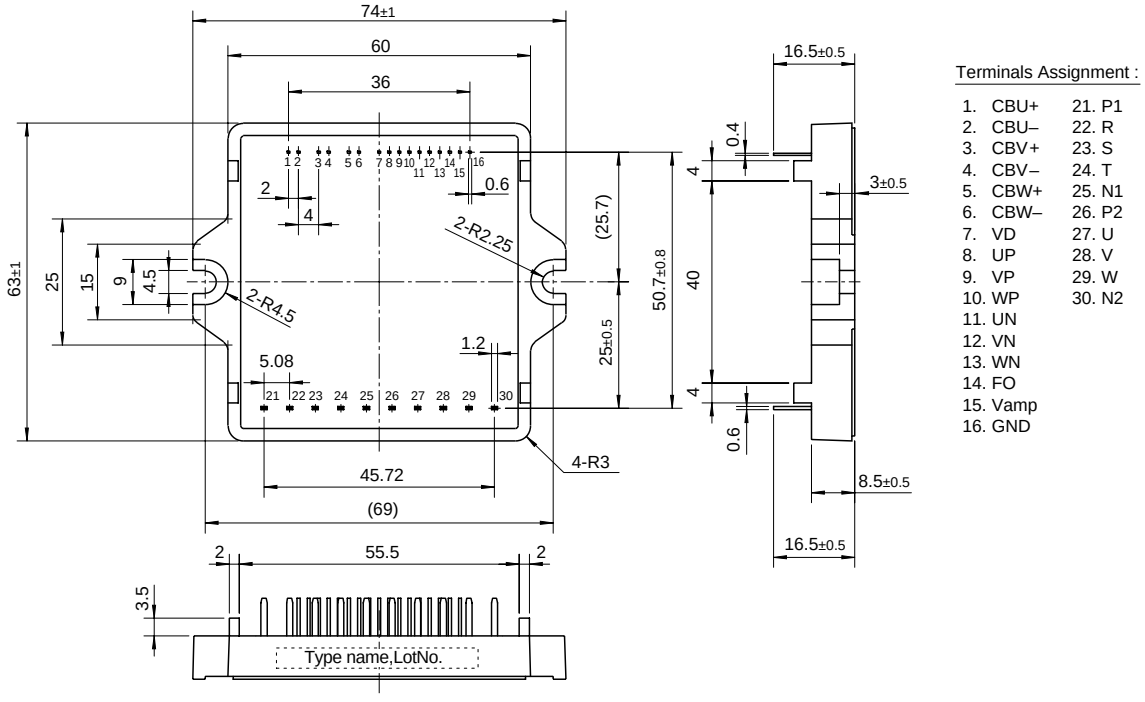
### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS:

- P-Side IGBTs : Drive circuit, high-level-shift circuit, bootstrap circuit supply scheme for Single Control-Power-Source drive, and under voltage (UV) protection.
- N-Side IGBTs : Drive circuit, DC-Link current sense and amplifier circuits for overcurrent protection, control-supply under-voltage protection (UV), and fault output ($F_O$) signaling circuit.
- Fault Output : N-side IGBT short circuit (SC), over-current (OC), and control supply under-voltage (UV).
- Inverter Analog Current Sense : N-Side IGBT DC-Link Current Sense.
- Input Interface : 5V CMOS/TTL compatible, Schmitt Trigger input, and Arm-Shoot-Through interlock protective function.

## APPLICATION

Acoustic noise-less 0.4kW/200V AC Class 3 phase inverters, motor control applications, and motors with built-in small size inverter package

### PACKAGE OUTLINES




Terminals Assignment :

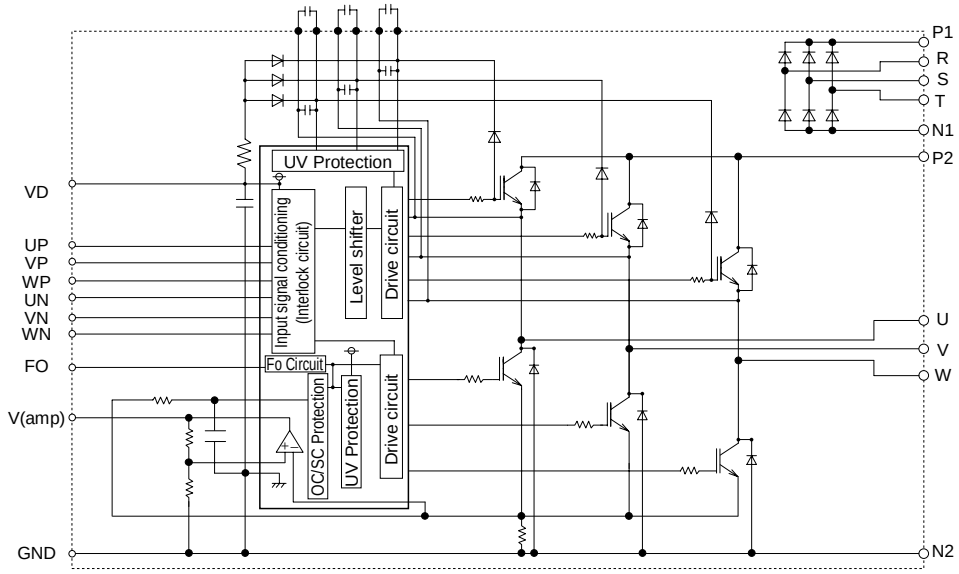
| | | | |
|---|---|---|---|
| 1. | CBU+ | 21. | P1 |
| 2. | CBU– | 22. | R |
| 3. | CBV+ | 23. | S |
| 4. | CBV– | 24. | T |
| 5. | CBW+ | 25. | N1 |
| 6. | CBW– | 26. | P2 |
| 7. | VD | 27. | U |
| 8. | UP | 28. | V |
| 9. | VP | 29. | W |
| 10. | WP | 30. | N2 |
| 11. | UN | | |
| 12. | VN | | |
| 13. | WN | | |
| 14. | FO | | |
| 15. | Vamp | | |
| 16. | GND | | |

(Fig. 1)

# PS11033

**FLAT-BASE TYPE**
**INSULATED TYPE**

**INTERNAL FUNCTIONS BLOCK DIAGRAM**




(Fig. 2)

**MAXIMUM RATINGS** (Tj = 25°C)

**INVERTER PART**

| Symbol | Item | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Applied between P2-N2 | 450 | V |
| $V_{CC(surge)}$ | Supply voltage (surge) | Applied between P2-N2, Surge-value | 500 | V |
| $V_P$ or $V_N$ | Each output IGBT collector-emitter static voltage | Applied between P2-U.V.W, U.V.W-N2 | 600 | V |
| $V_{P(S)}$ or $V_{N(S)}$ | Each output IGBT collector-emitter switching voltage | Applied between P2-U.V.W, U.V.W-N2 | 600 | V |
| ±Ic(±Icp) | Each output IGBT collector current | Tc = 25°C, "( )" means Ic peak value | ±8 (±16) | A |

**CONVERTER PART**

| Symbol | Item | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{RRM}$ | Repetitive peak reverse voltage | | 800 | V |
| Ea | Recommended AC input voltage | | 220 | Vrms |
| $I_O$ | DC output current | 3ϕ rectifying circuit | 10 | A |
| $I_{FSM}$ | Surge (non-repetitive) forward current | 1 cycle at 60Hz, peak value non-repetitive | 100 | A |
| $I^2t$ | $I^2t$ for fusing | Value for one cycle of surge current | 42 | $A^2s$ |

**CONTROL PART**

| Symbol | Item | Ratings | Unit |
|---|---|---|---|
| $V_D$, $V_{DB}$ | Supply voltage | –0.5 ~ 20 | V |
| $V_{CIN}$ | Input signal voltage | –0.5 ~ +7.5 | V |
| $V_{FO}$ | Fault output supply voltage | –0.5 ~ +7.5 | V |
| $I_{FO}$ | Fault output current | 15 | mA |
| $I_{amp}$ | DC-Link IGBT current signal Amp output current | 1 | mA |

# PS11033

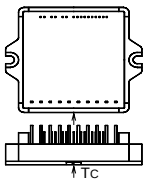
**FLAT-BASE TYPE**
**INSULATED TYPE**

## TOTAL SYSTEM

| Symbol | Item | Condition | Ratings | Unit |
|---|---|---|---|---|
| $T_j$ | Junction temperature | (Note 2) | –20 ~ +125 | °C |
| $T_{stg}$ | Storage temperature | — | –40 ~ +125 | °C |
| $T_C$ | Module case operating temperature | (Fig. 3) | –20 ~ +100 | °C |
| $V_{ISO}$ | Isolation voltage | 60 Hz sinusoidal AC applied between all terminals and the base plate for 1 minute. | 2500 | Vrms |
| — | Mounting torque | Mounting screw: M4 | 0.98 ~ 1.47 | N·m |

(Note 2) : The indicated values are specified considering the safe operation of all the parts within the ASIPM. The max. ratings for the ASIPM power chips (IGBT & FWDi) is Tj < 150.

## CASE TEMPERATURE MEASUREMENT POINT




(Fig. 3)

## THERMAL RESISTANCE

| Symbol | Item | Condition | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $R_{th(jc)Q}$ | Junction to case Thermal Resistance | Inverter IGBT (1/6) | — | — | 4.1 | °C/W |
| $R_{th(jc)F}$ | | Inverter FWDi (1/6) | — | — | 6.1 | °C/W |
| $R_{th(jc)FR}$ | | Converter Di (1/6) | — | — | 4.8 | °C/W |
| Rth(cf) | Contact Thermal Resistance | Case to fin thermal, grease applied (1 Module) | — | — | 0.074 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_j$ = 25°C, $V_D$ = 15V, $V_{DB}$ = 15V unless otherwise noted)

| Symbol | Item | Condition | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | Tj = 25°C, Input = ON, Ic = 8A, $V_D$ = $V_{DB}$ = 15V (Shunt voltage drop not included) | — | — | 2.9 | V |
| $V_{EC}$ | FWDi forward voltage | Tj = 25°C, –Ic = 8A | — | — | 2.9 | V |
| $V_{FR}$ | Converter diode voltage | Tj = 25°C, $I_{FR}$ = 5A | — | — | 1.5 | V |
| $I_{RRM}$ | Converter diode reverse current | $V_R$ = $V_{RRM}$, Tj = 125°C | — | — | 8 | mA |
| ton | Switching times | 1/2 Bridge inductive, Input = 5V ↔ 0V<br>$V_{CC}$ = 300V, Ic = 8A, Tj = 125°C<br>$V_D$ = 15V, $V_{DB}$ = 15V<br>Note: ton, toff include delay time of the internal control circuit. | 0.3 | 0.6 | 1.5 | µs |
| tc(on) | | | — | 0.43 | 0.8 | µs |
| toff | | | — | 1.6 | 2.5 | µs |
| tc(off) | | | — | 0.5 | 1.2 | µs |
| trr | FWDi reverse recovery time | | — | 0.12 | — | µs |
| Short circuit endurance (Output, Arm, and Load Short Circuit Modes) | | @$V_{CC}$ ≤ 400V, Input = 5V → 0V (One-Shot)<br>–20°C ≤ Tj (start) ≤ 125°C, 13.5V ≤ $V_D$ = $V_{DB}$ ≤ 16.5V | • No destruction<br>• $F_O$ output by protection operation | | | |
| Switching SOA | | @$V_{CC}$ ≤ 400V, Input = 5V ↔ 0V, Tj ≤ 125°C<br>Ic < OC trip level, 13.5V ≤ $V_D$ = $V_{DB}$ ≤ 16.5V | • No destruction<br>• No protecting operation<br>• No $F_O$ output | | | |



MITSUBISHI ELECTRIC

# PS11033

**FLAT-BASE TYPE**
**INSULATED TYPE**

**ELECTRICAL CHARACTERISTICS** ($T_j$ = 25°C, $V_D$ = 15V, $V_{DB}$ = 15V unless otherwise noted)

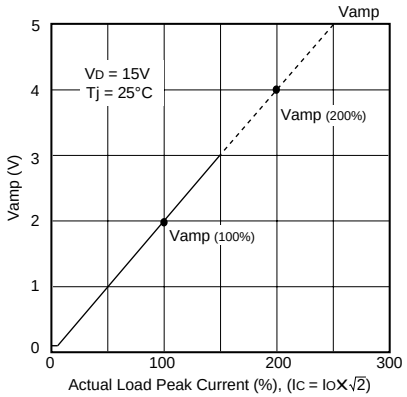
| Symbol | Item | | Condition | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $I_D$ | Circuit current (Average) | | $T_j$ = 25°C, $V_D$ = 15V, Vin = 5V | | — | — | 50 | mA |
| $I_{DB}$ | Circuit current (Average) | | $T_j$ = 25°C, $V_D$ = $V_{DB}$ = 15V, Vin = 5V | | — | — | 5 | mA |
| $V_{thon)}$ | Input on threshold voltage | | | | 0.8 | 1.4 | 2.0 | V |
| $V_{th(off)}$ | Input off threshold voltage | | | | 2.5 | 3.0 | 4.0 | V |
| $R_i$ | Input pull-up resistor | | Applied between input terminal-inside power supply | | — | 50 | — | kΩ |
| $f_{PWM}$ | PWM input frequency | | $T_C$ ≤ 100°C, $T_j$ ≤ 125°C | | 1 | — | 15 | kHz |
| $t_{dead}$ | Arm shoot-through blocking time | | Relates to corresponding inputs<br>$T_C$ = –20°C ~ +100°C (Note 3) | | 2.2 | — | — | µs |
| $t_{int}$ | Input interlock sensing | | Relates to corresponding input (Fig. 6) | | — | 100 | — | ns |
| Vamp(100%) | Inverter DC-Link IGBT current sense voltage output signal | | $I_C$ = $I_{OP(100\%)}$ | $V_D$ = 15V<br>$T_j$ = 25°C (Fig. 4) | 1.5 | 2.0 | 2.5 | V |
| Vamp(200%) | | | $I_C$ = $I_{OP(200\%)}$ | | 3.0 | 4.0 | 5.0 | V |
| Vamp(250%) | Inverter DC-Link IGBT current sense voltage output limit | | $I_C$ = $I_{OP(250\%)}$ | $V_D$ = 15V | 5.0 | — | — | V |
| Vamp(0) | | | $I_C$ = 0A | (Fig. 4) | — | 50 | 100 | mV |
| OC | Over current trip level | | $T_j$ = 25°C | (Fig. 5) | 8.5 | 10.6 | 16.0 | A |
| $t_{OC}$ | Over current delay time | | $T_j$ = 25°C | (Fig. 5) | — | 10 | — | µs |
| SC | Short circuit trip level | | $T_j$ = 25°C | (Fig. 5) | — | 16 | — | A |
| $t_{SC}$ | Short circuit delay time | | $T_j$ = 25°C | (Fig. 5) | — | 2 | — | µs |
| $UV_D$ | Supply circuit under voltage protection | Trip level | $T_C$ = $T_j$ = 25°C | (Fig. 5) | 11.0 | 12.0 | 13.0 | V |
| $UV_{Dr}$ | | Reset level | | | 11.5 | 12.5 | 13.5 | V |
| $UV_{DB}$ | | Trip level | | | 10.1 | 10.8 | 11.6 | V |
| $UV_{DBr}$ | | Reset level | | | 10.6 | 11.3 | 12.1 | V |
| tdV | | Delay time | | | — | 10 | — | µs |
| $t_{FO}$ | Fault output pulse width | | $T_j$ = 25°C | (Note 4) | 1.0 | 1.8 | — | ms |
| $I_{Fo(H)}$ | Fault output current | | Open collector output | (Note 4) | — | — | 1 | µA |
| $I_{Fo(L)}$ | | | | | — | — | 15 | mA |

(Note 3) : The dead-time has to be set externally by the CPU; it is not part of the ASIPM internal functions.
(Note 4) : Fault output signaling is given only when the internal OC, SC, & UV protection circuits are activated.
The OC, SC and UV protection (and fault output) operate for the lower arms only. The OC and SC protection Fault output is given in a pulse format while that of UV protection is maintained throughout the duration of the under-voltage condition.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Item | Condition | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage | Applied across P2-N2 terminals | — | 300 | 400 | V |
| $V_D$ | Supply voltage | Applied between $V_D$-GND | 13.5 | 15.0 | 16.5 | V |
| $V_{DB}$ | Supply voltage | Applied between CBU+ & CBU–, CBV+ & CBV–, CBW+ & CBW– | 13.5 | 15.0 | 16.5 | V |
| $\Delta V_D$, $V_{DB}$ | Supply voltage ripple | | –1 | — | +1 | V/µs |
| $V_{CIN(ON)}$ | Input on voltage | Applied between UP • VP • WP • UN • VN • WN and GND | 0 | — | 0.8 | V |
| $V_{CIN(OFF)}$ | Input off voltage | | 4.0 | — | 5.0 | V |
| $t_{dead}$ | Arm shoot-through blocking time | Relates to corresponding inputs | 2.2 | — | — | µs |
| $T_C$ | Module case operating temperature | | — | — | 100 | °C |
| $f_{PWM}$ | PWM Input frequency | $T_C$ ≤ 100°C, $T_j$ ≤ 125°C | — | — | 15 | kHz |
| $t_{XX}$ | Allowable minimum input on-pulse width | | 1 | — | — | µs |

**INVERTER DC-LINK IGBT CURRENT ANALOGUE SIGNALING OUTPUT (TYPICAL)**

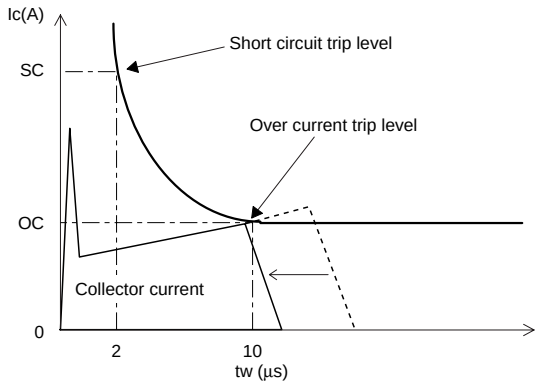



(Fig. 4)



MITSUBISHI ELECTRIC

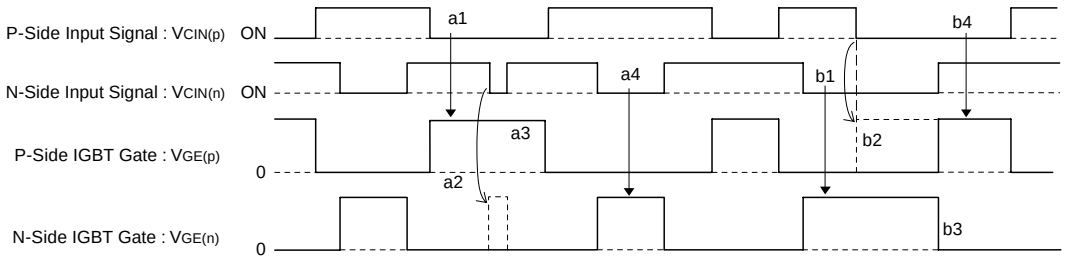
## CURRENT ABNORMALITY PROTECTIVE FUNCTIONS




(Fig. 5)

Protection is achieved by monitoring and filtering the N-side DC-Bus current. The over-current protection is activated (after allowing a filtering time of 10 μs) when the line current reaches 250% of the rated load-current Io (rms). Similarly, the short circuit protection is activated (after allowing a filtering time of 2 μs) when the line current reaches twice the rated collector-current (Ic). When a current trip-level is exceeded (OC or SC), all the N-side IGBTs are intercepted (turned OFF) and a fault-signal is output. After the fault-signal output duration (1.8 ms - typ.), the interception is Reset at the following OFF input signal. However, since the fault may be repetitive, it is recommended to stop the system after the fault-signal is received and check the fault. The trip-level settings described above are summarized in the following figure:

## ARM-SHOOT-THROUGH INTER-LOCK PROTECTIVE FUNCTION




(Fig. 6)

**Description:**

(1) During the ON-State of either of the upper-arm or the lower-arm IGBT, the inter-lock protection circuit blocks any erroneous ON pulses (resulting from input noise) from triggering the other arm IGBT and thus it prevents the arm-shoot-through situation.

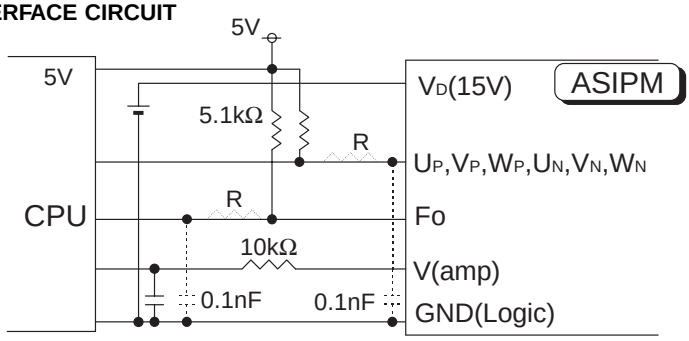
(2) When two ON-signals are received for both the upper and the lower arms, the signal received first will be passed to the IGBT and the second signal will be blocked. The second signal will be passed to its corresponding IGBT immediately after the first signal is OFF.

**Note:** This protective function provides no fault signaling output. The Dead-Time has to be set using the micro-controller (CPU).

**Operation:**

a1. P-side normal ON-signal ⇒ P-side IGBT gate turns ON.
a2. N-side erroneous ON-signal ⇒ N-side IGBT gate remains OFF.
a3. While P-side ON-signal remains ⇒ P-side IGBT gate remains ON.
a4. N-side normal ON-signal ⇒ N-side IGBT gate turns ON.
b1. N-side normal ON-signal ⇒ N-side IGBT gate turns ON.
b2. Simultaneous ON-signals ⇒ P-side IGBT gate remains OFF.
b3. N-side receives OFF-signal ⇒ N-side IGBT gate turns OFF.
b4. Immediately after (b3) ⇒ P-side IGBT gate turns ON.

## RECOMMENDED I/O INTERFACE CIRCUIT




(Fig. 7)