PN544

Near field communication (NFC) controller

Rev. 1.2 — 4 September 2007 | Objective short data sheet

134812

1. Introduction

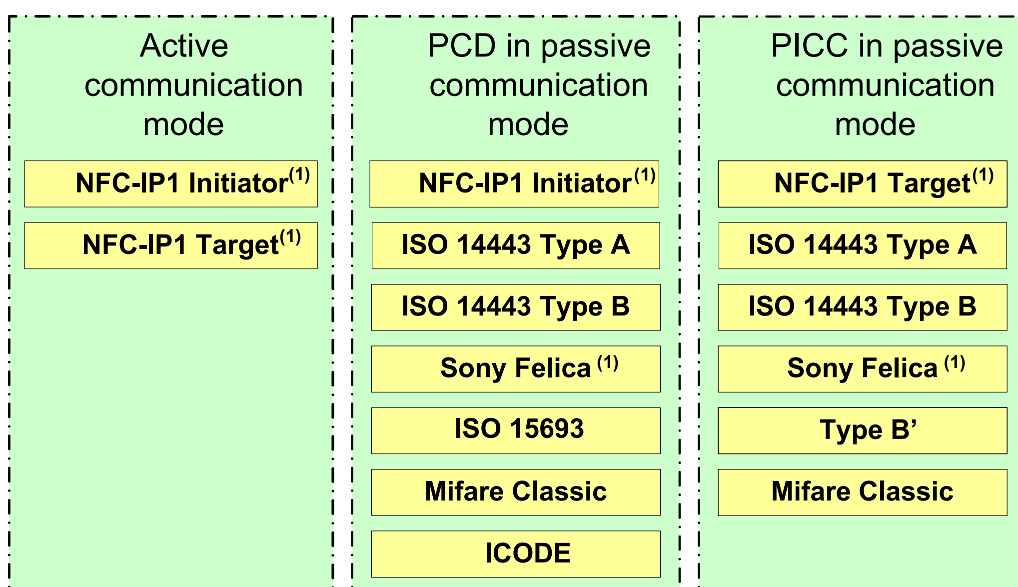
This Objective short data sheet describes the functionality of the controller IC PN544. It includes functional and electrical specifications. A complete specification will be given in the product data sheet.

2. General description

The PN544 is a highly integrated NFC controller IC for contactless communication at 13.56 MHz. This controller IC utilizes an outstanding modulation and demodulation concept for different kinds of contactless communication methods and protocols at 13.56 MHz.

The PN544 supports active mode for NFC-IP1 transmission modes. Passive mode is also supported where PN544 can act either as contactless reader or emulate an contactless card.

When configured in card emulation mode, PN544 supports both integrated Mifare Classic solution (optional) and all card modes supported by both PN544 and present phone SIM or separate secure element. Supported modes are pictured on this page.



(1) According to ISO/IEC 18092 (ECMA 340) standard (see Ref. 1)

Fig 1. PN544 transmission modes

Enabled in PCD mode for ISO/IEC 14443 Type A the PN544's internal transmitter part is able to drive a PCD antenna designed to communicate with ISO/IEC 14443 Type A cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC 14443 Type A compatible cards and transponders. The digital part handles the complete ISO/IEC 14443 Type A framing and error detection (Parity & CRC).

The PN544 supports Mifare Classic (e.g. Mifare Standard) products.

Enabled in PCD mode for FeliCa, the PN544 controller IC supports the FeliCa communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for FeliCa coded signals. The digital part handles the FeliCa framing and error detection like CRC. The PN544 supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

Enabled in PCD mode for ISO/IEC 14443-B, the PN544 supports all layers of the ISO/IEC 14443-B PCD communication scheme.

Enabled in VCD mode for ISO/IEC 15693, the PN544 supports all layers of the ISO/IEC 15693 VCD communication scheme. The PN544 supports ICODE-SLI and ICODE-EPC from the NXP ICODE product family.

The PN544 offers the possibility to communicate directly to an NFCIP-1 device in the NFCIP-1 mode. The NFCIP-1 mode offers different communication mode and transfer speeds up to 424 kbit/s. The digital part handles the complete NFCIP-1 framing and error detection. The NFC IP1 mode implementation will be in accordance with the NFC Forum requirements.

In PICC emulation mode, the PN544 is able to answer to a PCD command either according to the FeliCa, ISO/IEC 14443A/Mifare or to the ISO/IEC 14443B and Type B' PICC interface scheme. The PN544 generates the digital load modulated signals and sends the answer back to the PCD. The number of active emulated or integrated PICC emulations is configurable via the host interface, with only one PICC active at same time.

In order to fit into power requirements of mobile platform, PN544 supports various power modes, configurable both by hardware and software. PN544's power consumption behavior is fully configurable by software, but also in case of power loss PN544 is capable of maintaining subset of communication abilities if configured in such a manner. Power modes are described in more detail in Section 9 "Power supply" on page 18.

The use of this NXP IC according to ISO/IEC 14443B might infringe third party patent rights. A purchaser of this NXP IC has to take care for appropriate third party patent licenses.

Purchase of an NXP Semiconductors IC that complies with one of the NFC Standards (ISO/IEC 18.092; ISO/IEC 21.481) does not convey an implied license under any patent right on that standards.

A license for the portfolio of the NFC Standards patents of NXP B.V. needs to be obtained at Via Licensing, the pool agent of the NFC Patent Pool, e-mail: info@vialicensing.com".

3. Features

- Low power HT80C51 MX CPU core with 72 KBytes ROM, 44 KBytes non-volatile memory for code, 8 KBytes non-volatile memory for data and 4 KBytes RAM
- Buffered output drivers to connect an NFC antenna with minimum number of external components
- Integrated configurable Polling Loop for automatic device discovery
- Integrated data mode detector for automatic anticollision
- Integrated non-volatile memory to store data and executable code for customization
- Flexible clock supply concept to facilitate PN544 integration
  - Integrated FracNPLL to make use of cellular reference clock
  - 27.12 MHz direct clock input to minimize current consumption (integrated FracNPLL disabled)
  - Internal oscillator to connect an 27.12 MHz crystal (in case of absent reference clock, then FracNPLL is disabled to minimize current consumption)
- Flexible power supply concept to facilitate PN544 integration
  - Integrated power management unit to be directly connected to a mobile battery
  - 2.3 to 5.5 V power supply
  - Fully configurable power behavior
- Supporting various power saving modes per embedded firmware
  - Automatic host wake up via host control interface interfaces when PN544 is in Standby power saving mode
- Integrated self test to test external antenna matching circuit
- Highly integrated analog circuitry to modulate, demodulate, encode requests and decode responses
- Integrated RF Level detector
- Typical operating distance in PCD mode for communication to a ISO 14443A/Mifare, ISO14443B, NFC-IP1 passive target or FeliCa card up to 50 mm depending on the antenna size and tuning and power supply
- Typical operating distance in VCD mode for communication to a ISO/IEC 15693/ICODE TAG more than 50 mm depending on the antenna size and tuning, power supply and form factor of the TAG
- Typical operating distance in ISO14443A/Mifare, ISO14443B, Type B' or FeliCa card emulation mode of about 100 mm depending on the antenna size and tuning and the external field strength
- Supports Mifare Classic encryption in reader/writer mode
- Various host control interfaces
  - SPI interface
  - I^2C interface
  - High Speed Asynchronous Serial UART
- Various interfaces to secure companion chip
  - NFC-WI according to ECMA 373 standard
  - SWP
- Flexible interrupts using IRQ pin
- Power switch for secure companion chip
- Freely programmable general purpose IO ports

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Battery Supply Voltage		2.3	-	5.5	V
PV_{DD}	Pad power supply (Supply Voltage for host interface)		1.62	3.0	3.3	V
SV_{DD}	Supply Voltage for secure chip interface for NFC WI		1.62	1.8	1.98	V
V_{CC_SIM}	Supply Voltage for UICC over SWP	Class C	1.62	1.8	1.98	V
		Class B	2.7	3	3.3	V
I_{HPD}	Hard Power Down Current			5		µA
I_{MON}	Monitor Mode Current			10		µA
I_{SPD}	Soft Power down Current			50		µA
IVBAT	continuous total current consumption	PCD mode at typical 3 V		100		mA
IVBAT	continuous total current consumption	integrated card mode at typical 3 V		100		µA
T_{amb}	operating ambient temperature		-30		+70	°C

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls; body 4.5 x 4.5 x 0.8 mm	SOT962-1

6. Block diagram

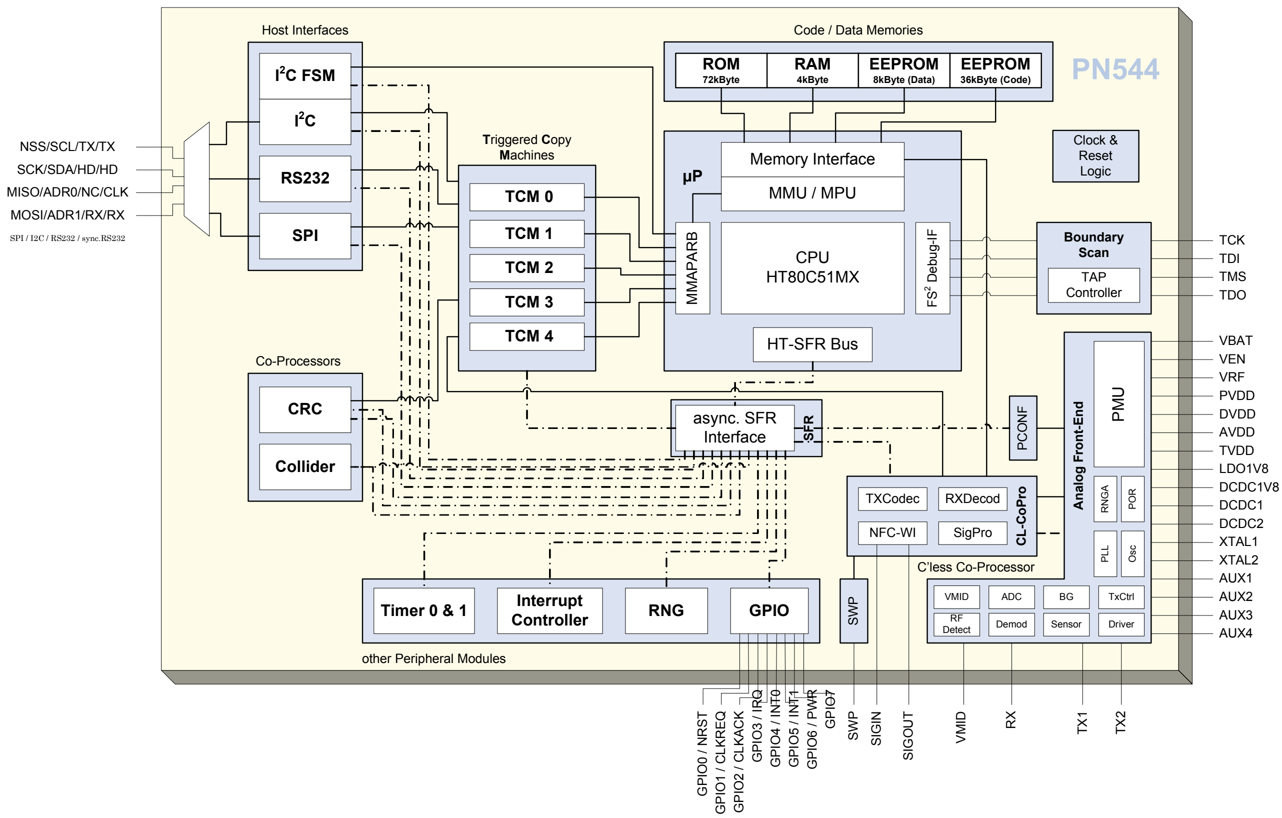


Fig 2. Block diagram of PN544

7. Pinning information

7.1 Pinning

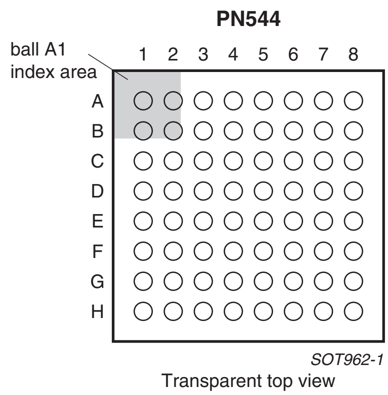


Fig 3. Pinning of PN544 in TFBGA64 (SOT962-1)

7.2 Pin description

Table 3: PN532 Pin description

Symbol	Pin	Type	Ref Voltage	Description
GPIO7	A1	IO	PVDD, DVDD	General purpose IO / Digital testbus signal
IFSEL0	A2	IO	PVDD, DVDD	Host interface select input
IRQ	A3	O	PVDD, DVDD	IRQ output
PVDD	A4	Power		Pad supply voltage input ($V_{I/O}$)
DVDD	A5	Power		Digital supply voltage output for decoupling
TMS	A6	I	PVDD, DVDD	JTAG
RFU1	A7			Reserved for future use
PMUVCC	A8	Power		SIM Power in from mobile PMU
GPIO4	B1	IO	PVDD, DVDD	General purpose IO / Digital testbus signal
GPIO5	B2	IO	PVDD, DVDD	General purpose IO / Digital testbus signal
GPIO6	B3	IO	PVDD, DVDD	General purpose IO / Digital testbus signal
IF1	B4	IO	PVDD, DVDD	Host interface pin - functionality depends on selected interface
PVSS	B5	Ground		Pad VSS
nOCI	B6	I	PVDD, DVDD	Selection between OCI and Boundary Scan functionality
VEN	B7	V_{BAT}		Enable/disable LDO regulator / Reset
SIMVCC	B8	Power		SIM Power out to UICC
VDHF	C1	Power		Monitor rectifier output voltage
GPIO3	C2	IO	PVDD, DVDD	General purpose IO / Digital testbus signal
GPIO2	C3	IO	PVDD, DVDD	General purpose IO / Digital testbus signal
IF2	C4	IO	PVDD, DVDD	Host interface pin - functionality depends on selected interface
TCK	C5	I	PVDD, DVDD	JTAG
NRESET	C6	I	PVDD, DVDD	Reset input (active low)
SWP	C7	PWR		SWP connection
SVDD	C8	Power		SE power; fixed to 1.8V
VCO_VDD	D1	Power		FracN supply voltage input
DVSS	D2	Ground		Digital VSS
GPIO1	D3	IO	PVDD, DVDD	General purpose IO / Digital testbus signal
IF3	D4	IO	PVDD, DVDD	Host interface pin - functionality depends on selected interface
TDI	D5	I	PVDD, DVDD	JTAG
EXT_SW_CTRL	D6	PWR		Control output signal for external UICC power switch
SIGOUT	D7	O	SVDD, PVSS	NFC-WI
VBAT	D8	Power		Battery voltage
XTAL1	E1	I	AVDD, AVSS	Oscillator input
AVSS1	E2	Ground		Analog VSS
GPIO0	E3	IO	PVDD, DVDD	General purpose IO / Digital testbus signal
IF0	E4	IO	PVDD, DVDD	Host interface pin - functionality depends on selected interface
TDO	E5	O	PVDD, DVDD	JTAG
RFU2	E6			Reserved for future use
SIGIN	E7	I	SVDD, PVSS	NFC-WI

Table 3: PN532 Pin description *…continued*

Symbol	Pin	Type	Ref Voltage	Description
LX	E8	Power		DCDC coil
XTAL2	F1	O	AVDD, AVSS	Oscillator output
AVDD_out	F2	Power		Analog supply voltage output for decoupling
AUX3	F3	O	AVDD, AVSS	Auxiliary Output: this pin delivers analog and digital test signals
IFSEL1	F4	IO	PVDD, DVDD	Host interface select input
IFSEL2	F5	IO	PVDD, DVDD	Host interface select input
DCDC_VSS	F6	Ground		DCDC VSS
TVDD_OUT	F7	Power		Driver supply voltage output for decoupling
VUP	F8	Power		DCDC output voltage for decoupling
AVDD_in	G1	Power		Analog supply voltage input after decoupling
AUX1	G2	O	AVDD, AVSS	Auxiliary Output: this pin delivers analog and digital test signals
AUX4	G3	O	AVDD, AVSS	Auxiliary Output: this pin delivers analog and digital test signals
VMID	G4	O	AVDD, AVSS	Antenna mid voltage, AVDD/2
PF1	G5	Power		Powered by the field contact
PF2	G6	Power		Powered by the field contact
PMU_GND	G7	Ground		PMU VSS
TVDD	G8	Power		Driver supply voltage input after decoupling
RFU3	H1			Reserved for future use
AUX2	H2	O	AVDD, AVSS	Auxiliary Output: this pin delivers analog and digital test signals
AVSS2	H3	Ground		Analog VSS
RX	H4	I	AVDD, AVSS	Receiver input
TVSS1	H5	Ground		Driver VSS
TX1	H6	O	TVDD, TVSS	Antenna driver
TX2	H7	O	TVDD, TVSS	Antenna driver
TVSS2	H8	Ground		Driver VSS

8. Communication modes

The PN544 supports various communication modes at different transfer speeds and modulation schemes. The following chapters give more detailed overview of selected communication modes.

Note: All indicated modulation indices and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

8.1 Reader/Writer modes

Generally 4 Reader/Writer modes are supported:

- PCD reader/writer for ISO/IEC 14443A/Mifare
- PCD reader/writer for FeliCa cards
- PCD reader/writer for ISO/IEC 14443B
- VCD reader/writer for ISO/IEC 15693/ICODE.

8.1.1 ISO/IEC 14443-A/Mifare PCD mode

The ISO/IEC 14443-A/Mifare PCD mode is the general reader to card communication scheme according to the ISO/IEC 14443-A/Mifare specification.The following diagram describes the communication on a physical level, the communication table describes the physical parameters.

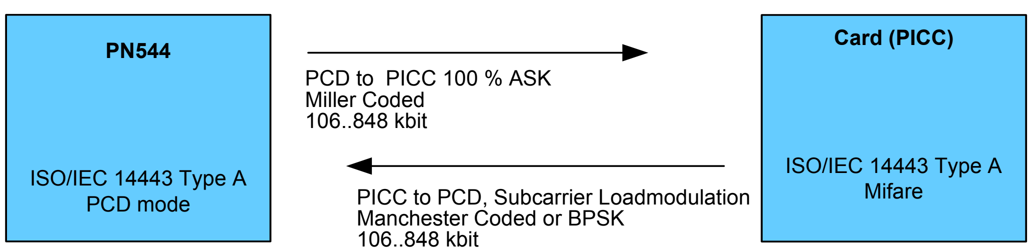


Fig 4. ISO/IEC 14443A/Mifare Reader/Writer mode communication diagram

Table 4. Communication overview for ISO/IEC 14443A/Mifare reader/writer

Communication direction		ISO 14443A/ Mifare	ISO 14443A higher transfer speeds		
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
PN544 → PICC (send data from the PN544 to a card)	Modulation on reader side	100% ASK	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
	Bitlength	(128/13.56) μs	(64/13.56) μs	(32/13.56) μs	(16/13.56) μs
PICC → PN544 (receive data from a card)	modulation on card side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester coding	BPSK	BPSK	BPSK

The contactless UART and the on-chip CPU of the PN544 handle the complete ISO/IEC 14443-A/Mifare RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

8.1.2 FeliCa PCD mode

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The following diagram describes the communication on a physical level, the communication overview describes the physical parameters.

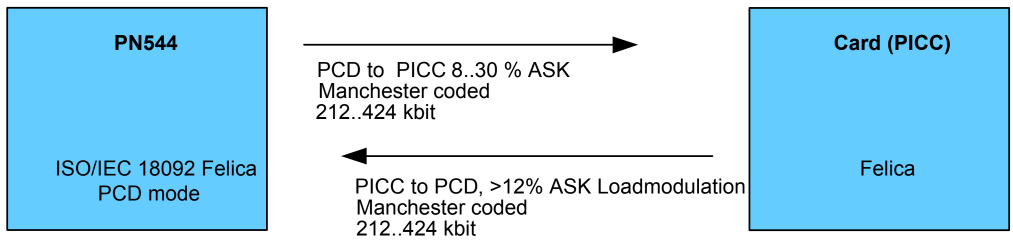


Fig 5. FeliCa reader/writer Communication Diagram

Table 5. Communication overview for FeliCa reader/writer

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
PN544 → card	Modulation on reader side	8-30% ASK	8-30% ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) μs	(32/13.56) μs
card → PN544	Loadmodulation on card side	>12% ASK	>12% ASK
	bit coding	Manchester coding	Manchester coding

The contactless UART of PN544 and the on-chip CPU handle the FeliCa protocol. Nevertheless a dedicated external host has to handle the application layer communication.

8.1.3 ISO/IEC 14443B PCD mode

The ISO/IEC 14443-B PCD mode is the general reader to card communication scheme according to the ISO/IEC 14443-B specification.The following diagram describes the communication on a physical level, the communication table describes the physical parameters.

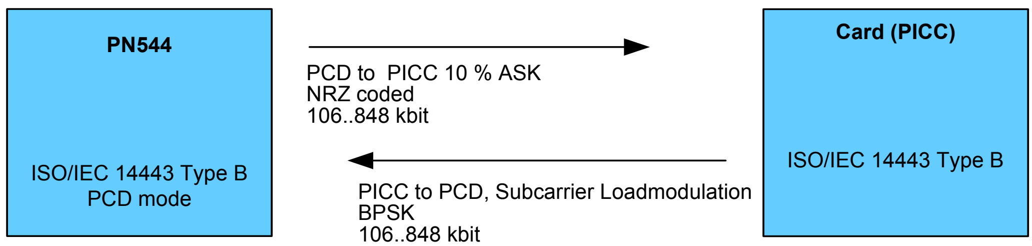


Fig 6. ISO/IEC 14443B reader/writer communication diagram

Table 6. Communication overview for ISO/IEC 14443B reader/writer

Communication direction		ISO 14443B	ISO 14443B higher transfer speeds		
	transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
reader/writer → PN544	Modulation on reader side	10% ASK	10% ASK	10% ASK	10% ASK
	bit coding	NRZ	NRZ	NRZ	NRZ
	Bitlength	(128/13.56) μs	(64/13.56) μs	(32/13.56) μs	(16/13.56) μs
PN544 → reader/writer	Modulation on PN544 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK	BPSK

The contactless UART and the on-chip CPU of the PN544 handle the complete ISO/IEC 14443-B RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

8.1.4 ISO/IEC 15693 VCD mode

The ISO/IEC 15693 VCD reader/writer mode is the general reader to card communication scheme according to the ISO/IEC 15693 specification. The ISO/IEC 15693-3 specification defines four sets of commands: mandatory, optional, custom, proprietary commands. The PN544 supports all mandatory and optional commands.

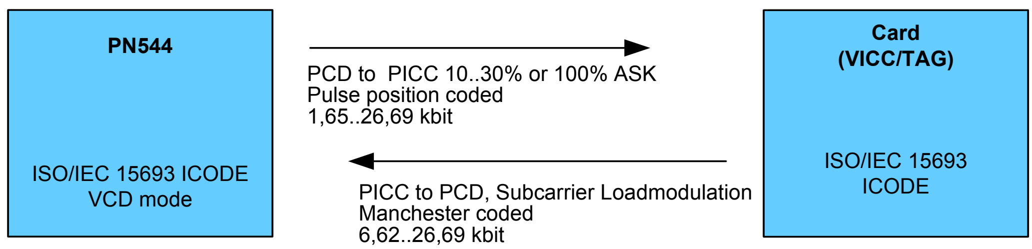


Fig 7. ISO/IEC 14443B reader/writer communication diagram

Table 7. Communication overview for ISO/IEC 14443B reader/writer

Communication direction					
PN544 → TAG	**Transfer speed**	**1.65 kbit/s**		**26.48 kbit/s**	
	Modulation on reader side	10-30% or 10% ASK		10-30% or 10% ASK	
	bit coding	Pulse Position Modulation1 out of 256 mode		Pulse Position Modulation1 out of 4 mode	
	Bitlength	(8192/13.56) µs		(512/13.56) µs	
TAG → PN544	**Transfer speed**	**1.65 kbit/s**	**6.67 kbit/s**	**26.48 kbit/s**	**26.69 kbit/s**
	Subcarrier	Single Subcarrier		Single Subcarrier	
	Loadmodulation on card side	load modulation amplitude shall be at least 10 mV			
	bit coding	Manchester coding			

8.2 NFCIP-1 mode

The NFCIP-1 communication differentiates between an active and a Passive Communication mode.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data.

  Note: *The active communication mode will only be implemented on hardware level as the NFC Forum might require only the support of the passive communication mode.*
- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication
  - Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
  - Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

In order to support the NFCIP-1 standard the PN544 supports the Passive Communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard and defined by the NFC Forum.

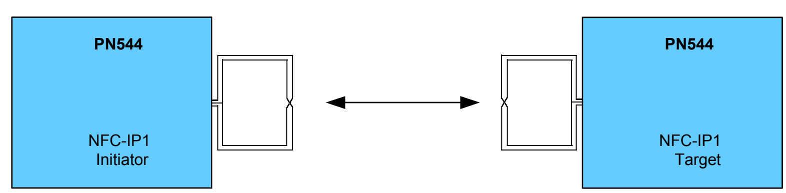


Fig 8. NFCIP-1 mode

8.2.1 Passive Communication mode

Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active meaning generating the RF field.

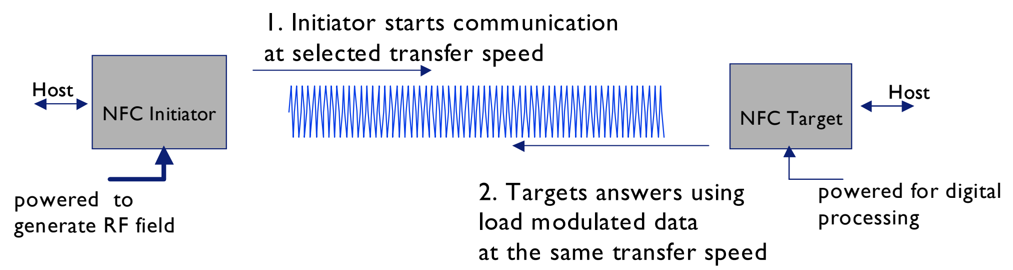


Fig 9. Passive Communication mode

Table 8. Communication Overview for Passive Communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s
Initiator → Target	According to ISO 14443A 100% ASK, Modified Miller Coded	According to FeliCa, 8-30% ASK Manchester Coded	
Target → Initiator	According to ISO 14443A subcarrier load modulation, Manchester Coded	According to FeliCa, >12% ASK Manchester Coded	

The contactless UART and the on-chip CPU of the PN544 handle the complete NFC-IP1 RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

8.2.2 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Passive Communication mode is defined in the NFCIP-1 standard.

Table 9. Framing and Coding Overview

Transfer speed	Framing and Coding
106 kbit/s	According to the ISO 14443A/Mifare scheme
212 kbit/s	According to the FeliCa scheme
424 kbit/s	According to the FeliCa scheme

8.3 Card Operation mode

The PN544 can be addressed like a FeliCa, ISO/IEC 14443 A or ISO/IEC 14443 B card. This means that the PN544 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A, ISO/IEC 14443B or FeliCa interface description.

Mifare is supported as an integrated Mifare card or via NFC-WI or via SWP CLT. Integrated Mifare functionality is accesible via RF field only.

Note: The PN544 does not support a complete card protocol. This has to be handled either by a connected companion secure chip or the host controller.

8.3.1 Mifare Card Operation mode

Table 10. Mifare Card Operation mode

Communication direction		ISO 14443A/ Mifare	ISO 14443A higher transfer speeds		
	transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
reader / writer → PN544	Modulation on reader side	100% ASK	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller	Modified Miller
	Bitlength	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN544 → reader/ writer	Modulation on PN544 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester coding	BPSK	BPSK	BPSK

8.3.2 FeliCa Card Operation mode

Table 11. FeliCa Card Operation mode

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	212 kbit/s	424 kbit/s
reader/writer → PN544	Modulation on reader side	8-30% ASK	8-30% ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) µs	(32/13.56) µs
PN544 → reader/ writer	Load modulation on PN544 side	>12% ASK load modulation	>12% ASK load modulation
	bit coding	Manchester coding	Manchester coding

8.3.3 Type B Card Operation mode

Table 12. ISO/IEC 14443 B Card Operation mode

Communication direction		ISO 14443B	ISO 14443B higher transfer speeds		
	transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
reader / writer → PN544	Modulation on reader side	10% ASK	10% ASK	10% ASK	10% ASK
	bit coding	NRZ	NRZ	NRZ	NRZ
	Bitlength	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN544 → reader/ writer	Modulation on PN544 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK	BPSK

9. Power supply

Main idea behind PN544's power concept is full host control over both PN544's power consumption and active communication modes. This controller is designed to adapt his current consumption to the available system energy and host controlled configuration.

As long as host controller is on, it has full control over PN544's behavior and indirectly over it's current consumption.

With host controller turned off, PN544 makes it's power state dependent on battery voltage, HW configuration pins and internal software configuration.

9.1 Power modes

Different power modes are implemented in order to optimize phone battery and contactless performance depending on the mobile state and battery charge status. Without host control PN544 acts autonomously based on SW pre-configuration, battery charge status and RF field existence.

With active host control and/or according system integration PN544 can be forced to low power mode, limiting its communication capabilities but also minimizing impact on phone battery life.

If sufficient energy is provided by RF field, in host controlled power down mode PN544 reduces current consumption from battery to minimum without limiting its communication capabilities in UICC emulation mode.

9.1.1 Functional power modes

From the system point of view and only with according SW configuration, PN544 supports following functional power modes (see also Figure 10):

9.1.1.1 Active mode

This mode can be either battery (Active BAT) or antenna (Active ANT) supplied. All card emulation modes configured by the host are allowed in this mode. In this mode, all PN544 modules are powered.

This is also the default mode for PN544. Note that the current consumption in this mode can vary depending on operation executed.

9.1.1.2 Standby mode

Standby mode is used to save energy when battery is still available for PN544. This mode is trade-off between functionality and current consumption and can be entered either automatically or after dedicated host command.

9.1.1.3 Active reader/writer mode

In this mode PN544 generates RF field and thus has maximum power consumption. This mode is possible only if sufficient energy from phone battery is available.

This mode can be entered automatically by PN544 in polling mode, appropriate host configuration is needed.

The PN544 features integrated DC/DC converter in order to ensure 3 V on transmitter path to keep same RF distance performance even when the battery level goes below 3 V.

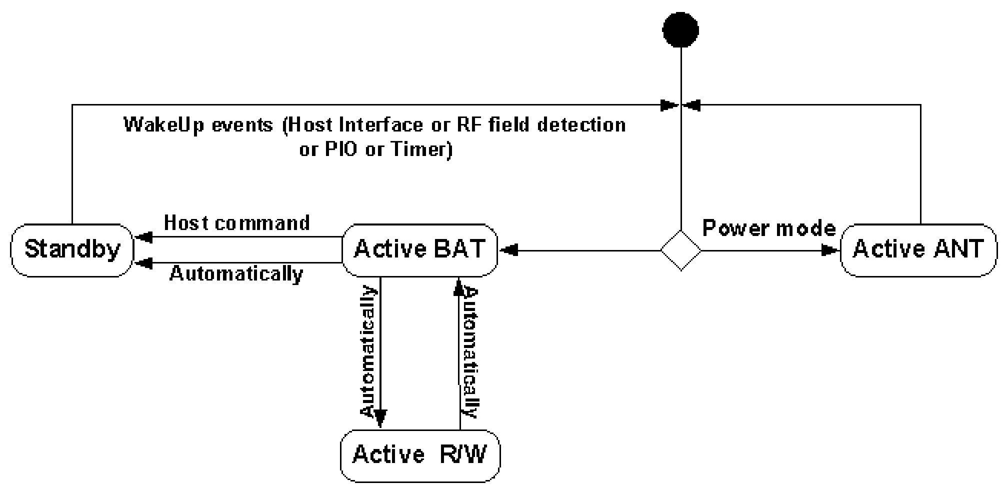


Fig 10. Functional power modes

9.1.2 Hardware power modes

Additionally, PN544 has two HW power modes which are not configurable by software and depend solely on HW signals and voltage levels.

9.1.2.1 Hard power-down mode

PN544 is set to hard power-down mode by host via VEN pin. If enabled, Powered by the field mode is possible upon RF field entry. No voltage monitoring is performed in this mode. No autonomous recovery from this mode is possible.

9.1.2.2 Monitor mode

In this mode phone battery voltage is below fixed[1] threshold. All interfaces are turned off for power savings, but battery voltage is still monitored. Only dedicated low-power circuitry is powered in this mode. Until phone battery voltage raises above critical threshold no recovery by host is possible. Powered by the field is possible if configured by host.

1. Threshold voltage is a hardware feature and can be changed in different product versions.

9.2 PN544 Supply

This controller is supplied with two different supply voltages: $V_{I/O}$ and V_{BAT}. This ensures independence between contactless core, supplied by V_{BAT}, and interface with baseband, supplied by $V_{I/O}$.

V_{BAT} supply is either connected directly to the phone battery or to LDO from host PMU. Depending on connection, PN544 can be configured to operate without host presence or even without battery presence.

With optional Powered by the field antenna matching circuit, PN544 can be operated without battery present. PN544 detects field entry automatically and can, as long sufficient energy is provided by the field[2], operate autonomously and supply phone SIM or separate secure element connected via NFC-WI.

9.3 Supply of a secure element

PN544 provides integrated PMU to ensure supply voltage for both secure elements connected via SWP or NFC WI interface.

9.3.1 Supply of SIM with SWP interface

According to ETSI SWP specification, NFC controller can be the source of SIM supply (VCC pin). PN544 will offer this possibility wherever the SIM power comes from (PMU, battery, field).

In case SIM supply is routed via PN544, it will supply the SIM if configured so by host in active battery mode or if SIM is needed by PN544 in all other modes.

The PN544 will route the SIM supply from the host PMU without taking care of the voltage ramp, it is in host responsibility to ensure that SIM supply is according to current standards. PN544 will support Class B voltage range providing 50 mA and Class C voltage range providing 30 mA.

Class A is not supported.

9.3.2 Supply of secure element connected over NFC-WI

A switch is implemented to control power supply of secure element connected via NFC-WI. Only Class C voltage range is supported for secure element connected via NFC-WI.

2. This is highly dependent on distance to reader, antenna geometry, matching circuit used and phone integration constraints.

10. Clock Supply

The PN544 features internal low power oscillator (~300kHz) and thus does not require connection of 32 kHz clock for very low power mode.

In operation modes where PN544 is clock reference for other devices, PN544 requires more accurate external clock which has to be provided by the system. In this case, PN544 will either use the clock provided by external oscillator or request the clock from the mobile platform.

If external oscillator is used, 27.12 MHz reference is expected. If clock is provided by the mobile platform, there are 4 discrete supported frequency values:

13/19.2/26 or 38.4 MHz

In this case, integrated FracNPLL of PN544 reduces the BOM of NFC solution, eliminating the need for external circuitry for clock generation.

The PN544 supports two different modes for requesting clock from the mobile platform:

10.1 Clock request via HW

In this mode, PN544 will request the clock by setting the pin CLK_REQ to high. Two different scenarios for clock settling signaling are possible.

10.1.1 Clock settling time with configurable time-out

After setting the pin, PN544 will wait up to 10ms (configurable in 1ms steps) for clock to stabilize and use clock available on the CLK pin. In this scenario, no CLK_ACK pin is needed and will be ignored by PN544. Refer to Figure 11 for details.

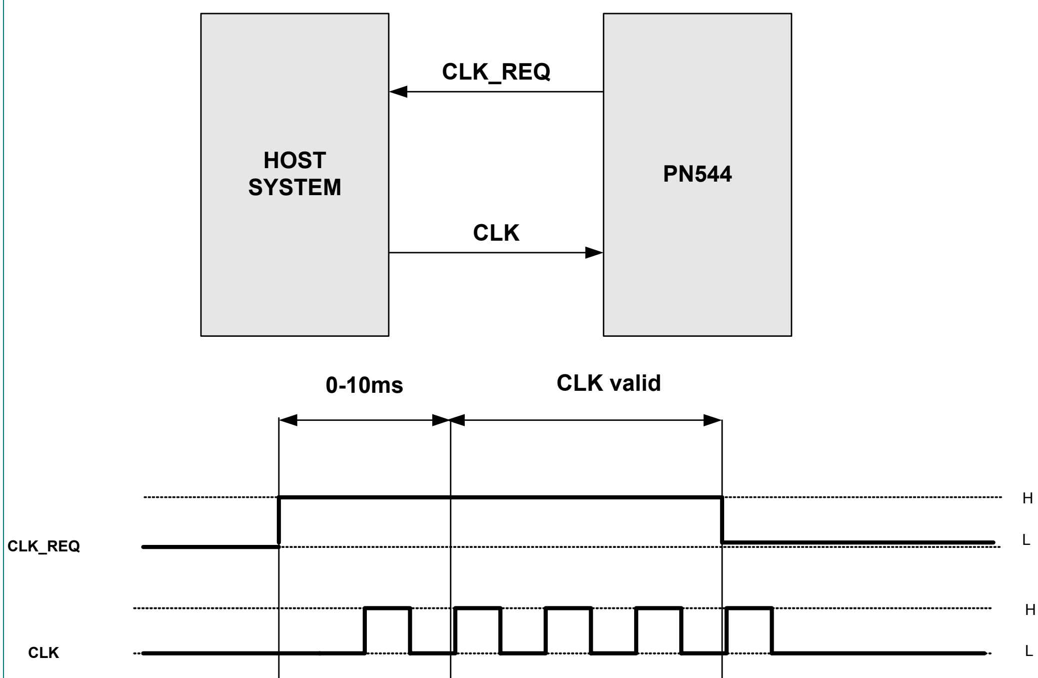


Fig 11. Clock settling time with dedicated CLK_ACK pin

10.1.2 Clock settling time with dedicated CLK_ACK pin

The PN544 will set CLK_REQ pin and wait for CLK_ACK to get to high state. This can be controlled by either baseband or dedicated clock generation IC. Refer to Figure 12 for details.

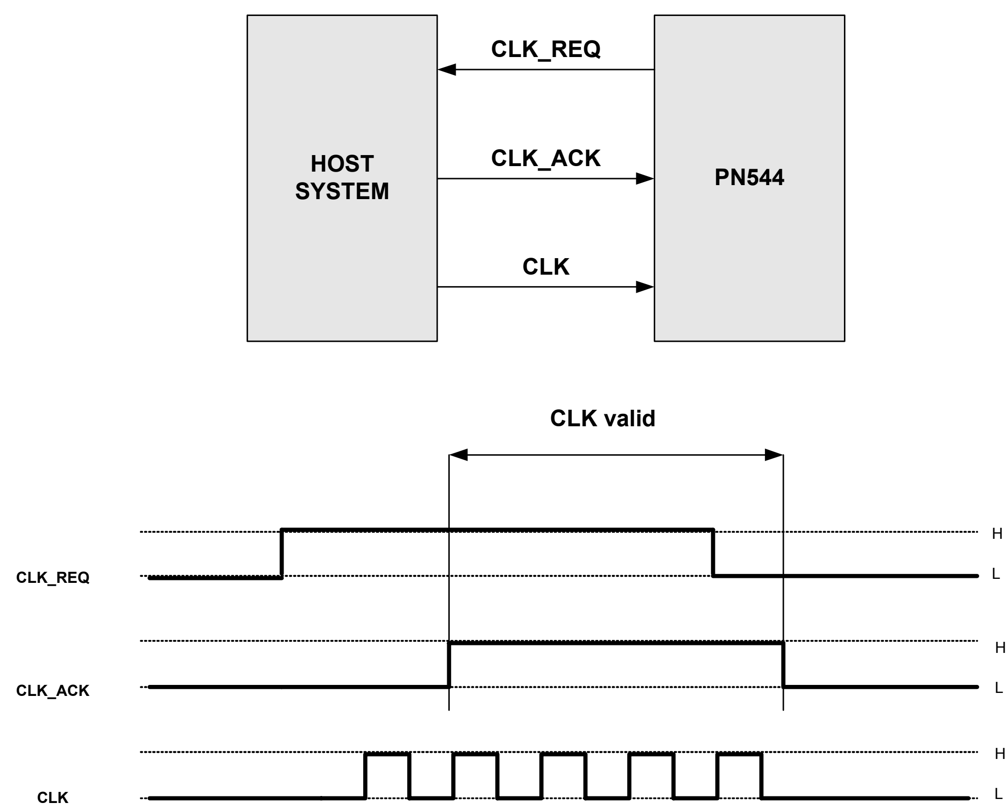


Fig 12. Clock settling time with dedicated CLK_ACK pin

10.2 Clock request via baseband interrupt

In this software controlled mode, clock is generated by baseband. The PN544 will generate an interrupt requesting baseband wake up and signalling clock demand. Baseband will read out the interrupt status register from PN544 and enable the clock. Once clock is stable, baseband informs PN544 via SW command.

11. Interfaces

The PN544 features multiple interface options for connecting both host controller and secure elements. For the host controller three different interfaces are integrated, but only one can be used in a system as PN544 is configured for selected interface and pins of PN544 are shared between different host interfaces.

11.1 Host interfaces

The PN544 supports the following host interfaces:

- HSU Slave Interface, up to 1.28 MBaud
- SPI Slave Interface, up to 10 MBaud
- I^2C Slave Interface, up to 400 kBaud

Only one host interface can be active at same time as pins are shared for all interfaces[3]. The host interfaces are activated in the following way:

- HSU: Wake-up after multiple pulses on RX line
- SPI: Transition of NSS Serial
- I^2C: Wake-up on I^2C address

To enable and ensure data flow control between PN544 and host controller additional dedicated interrupt line is also used.

11.2 Interfaces to secure elements

The PN544 supports the following interfaces to secure elements to enable applications hosted by a secure element

- SWP. The PN544 is targeted to be compliant with ETSI SWP specification[4].
- NFC WI in card emulation mode

The PN544 has as target to be compliant with HCI 2.0 ETSI specification[5]. This implies also the support for all tunneling modes as specified in ETSI (e.g. Mifare via CLT).

3. **Remark:** Pin layout would allow simultaneous connection of HSU and I2C, but this is not supported by PN544.
4. The SWP specification is currently under discussion of the ETSI SCP and not finalized yet
5. The HCI specification is currently under discussion of the ETSI SCP and not finalized yet. Therefore, the SW layer regarding HCI functionality will be implemented in EEPROM in order to ensure implementation of the final specification.

12. Application design-in information

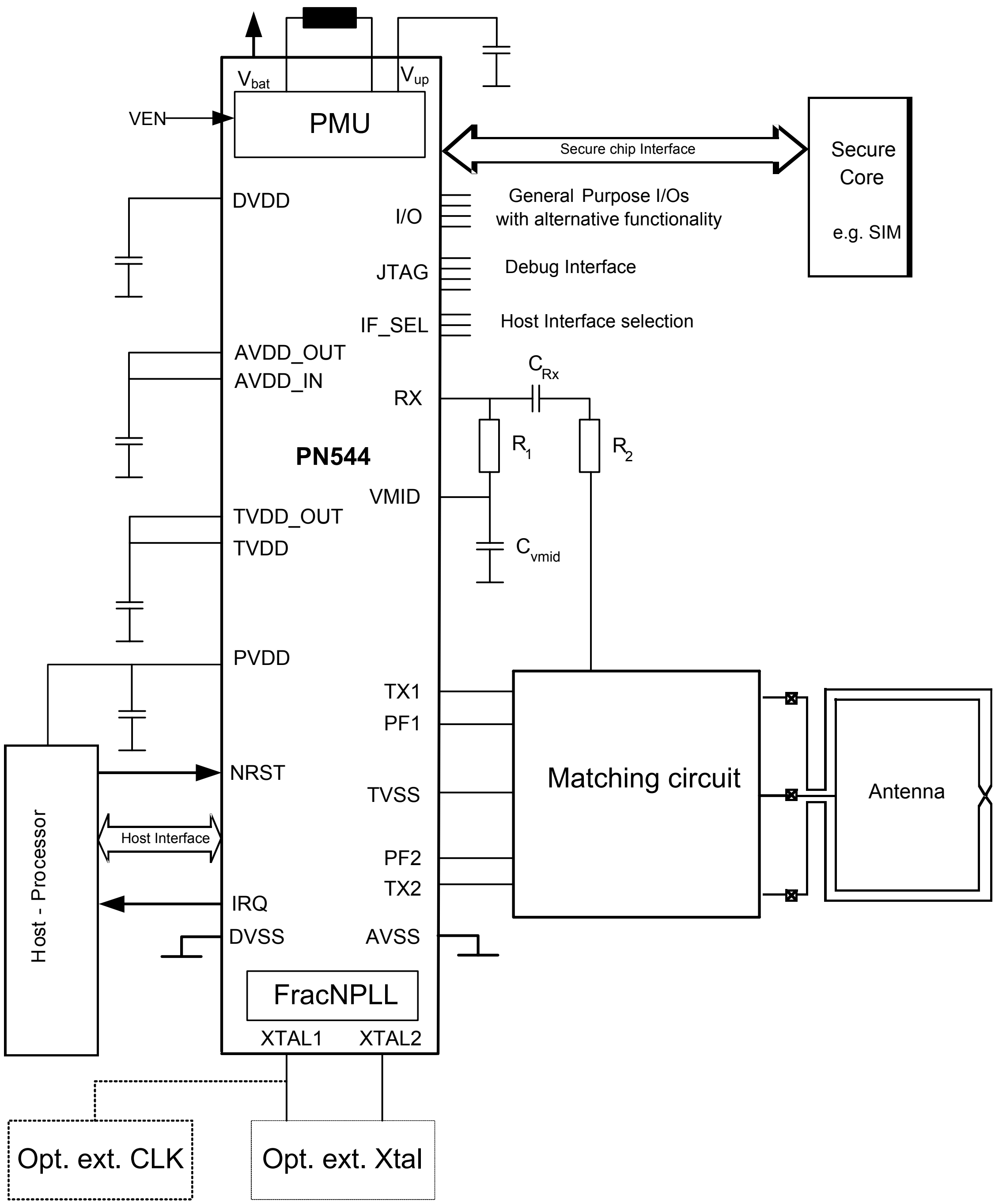
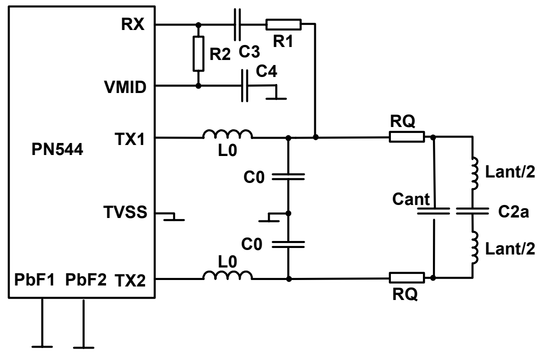
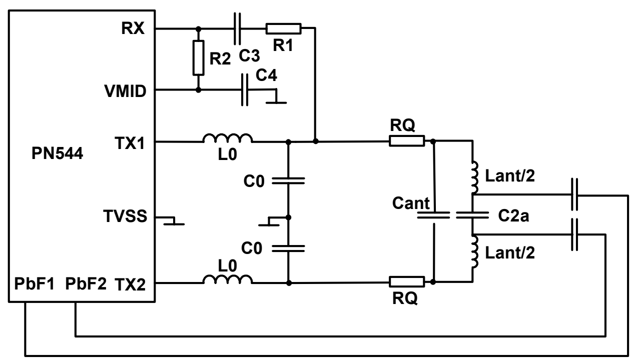


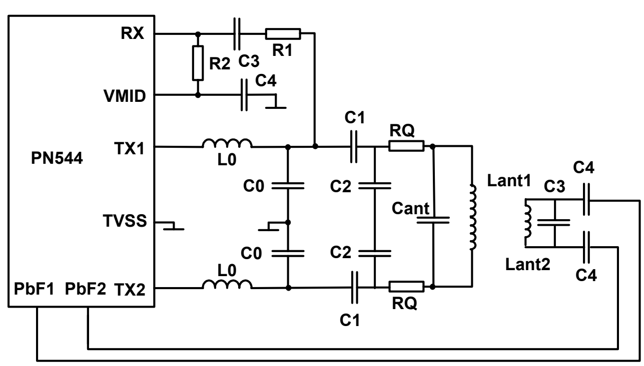
Fig 13. Typical application circuit diagram of PN544



Powered by the field not supported



Powered by the field concept



Powered by the field, alternative concept

Fig 14. Typical application connection of PN544

13. Limiting values

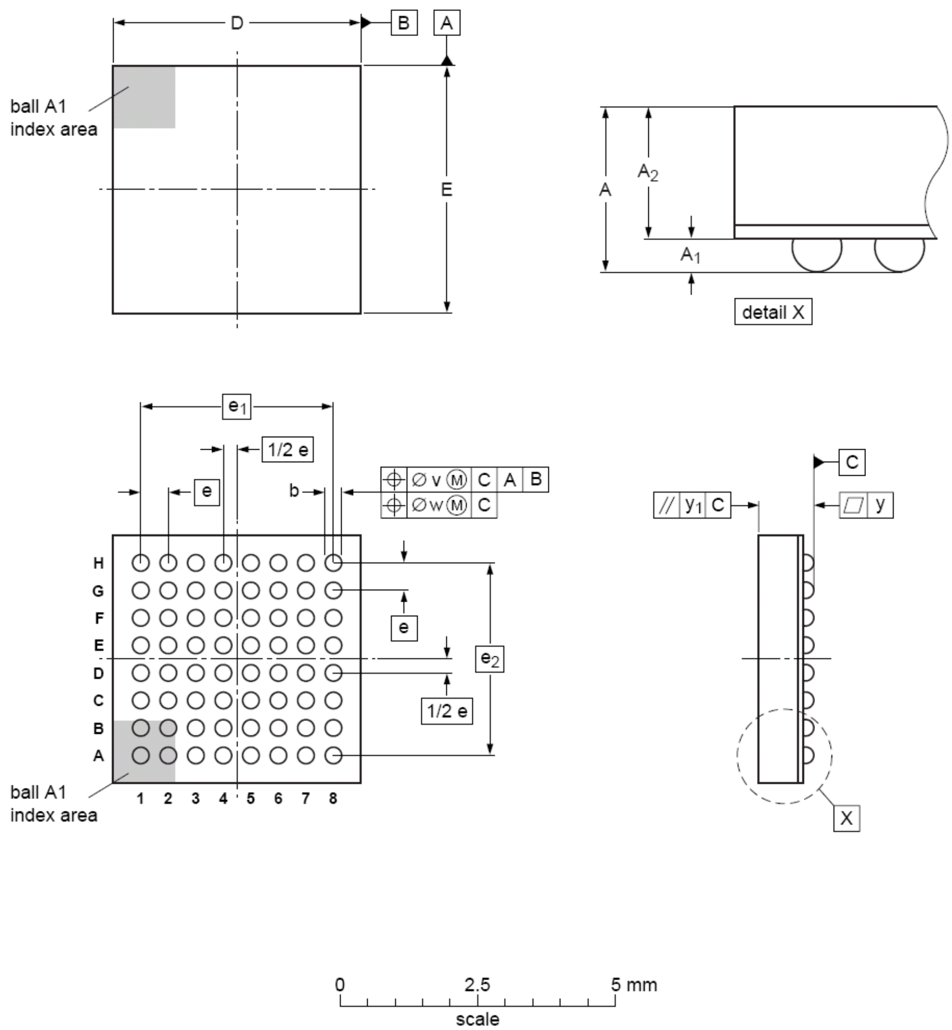
Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Tstg	Storage temperature range		-30	+85	°C
ESDH	ESD Susceptibility (Human Body model)	1500 W, 100 pF; JESD22-A114-B		2000	V
ESDM	ESD Susceptibility (Machine model)	0.75 mH, 200 pF; JESD22-A114-A		200	V
ESDC	ESD Susceptibility (Charge Device model)	Field induced model; JESC22-C101-A		1000	V

14. Package outline

TFBGA64: plastic thin fine-pitch ball grid array package; 64 balls; body 4.5 x 4.5 x 0.8 mm **SOT962-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.1	0.25 0.15	0.85 0.75	0.35 0.25	4.6 4.4	4.6 4.4	0.5	3.5	3.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT962-1	- - -	- - -	- - -			~~06-07-07~~ 06-08-01

Fig 15. Package outline of SOT962-1

15. Abbreviations

Table 14. Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
Automatic anticollision	Detect and recognize requests from any NFC initiator or reader/writer device, like NFC-Target, ISO/IEC 14443, Type A PICC (identical to NFC -Target) or ISO/IEC 14443, Type B PICC
Automatic device discovery	Detect and recognize any NFC peer devices (initiator or target) like: NFC initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, Mifare Standard and UltraLight PICC, ISO/IEC 15693 VICC
Autonomous tag communication	Detect and recognize any NFC peer devices (initiator or target) like: NFC initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, Mifare Standard and UltraLight PICC, ISO/IEC 15693 VICC
Initiator	Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
Integrated PICC	A full PICC (e.g. Mifare Std. or Ultralight, NFC forum tag) is completely integrated in the IC meaning that the application is handled by the NFC IC as well.
Loadmodulation Index	The load modulation index is defined as the card's voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) measured at the card's coil.
Modulation Index	The modulation index is defined as the voltage ratio (Vmax - Vmin)/ (Vmax + Vmin).
PCD	Proximity Coupling Device. Definition for a Card reader/writer device according to the ISO 14443 specification.
PCD -> PICC	Communication flow between a PCD and a PICC according to the ISO 14443A/Mifare
PICC	Proximity Interface Coupling Card. Definition for a contactless Smart Card according to the ISO 14443 specification.
PICC emulation	The IC is capable of handling a PICC emulation on the RF interface including part of the protocol management. The application handling is done by the host controller.
PICC-> PCD	Communication flow between a PICC and a PCD according to the ISO 14443A/Mifare.
Powered by the field mode	A contactless device supports powered-by-the-field mode if it is capable of performing PICC emulation mode transactions while extracting the required power from the electromagnetic RF-field generated by a coupled PCD. Example: contactless plastic smart cards.
Target	Responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator).
VCD	Vicinity Coupling Device. Definition for a reader/writer device according to the ISO 15693 specification.

16. References

[1] Standard ECMA-340, Near Field Communication Interface and Protocol (NFCIP-1) This 2nd Edition is harmonized with ISO/IEC 18092:2004, and refers to the NFCIP-1 test method standards ECMA-356 and ECMA-362.

[2] Standard ECMA-352, Near Field Communication Interface and Protocol -2 (NFCIP-2). ECMA-352 is harmonized with ISO/IEC 21481:2005, and refers to the NFCIP-1 test method standards ECMA-356 and ECMA-362

[3] International Standard ISO/IEC 14443 Identification cards — Contactless integrated circuit(s) cards — Proximity cards — Part 1-4

[4] International Standard ISO/IEC 15693 Identification cards — Contactless integrated circuit(s) cards — Vicinity cards — Part 1-3

[5] NFC Data Exchange Format (NDEF) Technical Specification

[6] NFC Record Type Definition (RTD) Technical Specification

17. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
134812	4 September 2007	Objective short data sheet		Revision 1.1
Modifications:	• Section 9.1.1 "Functional power modes" on page 18 corrected reference of Figure 10 • Section 9.1.2.2 "Monitor mode" on page 19 corrected typo: All interfaces are turned **off**			
134811	17 August 2007	Objective short data sheet		Revision 1.0
Modifications:	• HVQFN package removed, TFBGA package updated • Integrated on-chip NFC Type-2 Tag in powered-by-the-field mode removed • Autonomous tag communication (mandated NFC Forum tags and Mifare1k) removed • Antenna matching circuit integrated • Updated Abbreviations • Figure 2 "Block diagram of PN544" on page 5 updated • Chapter General description updated • Figure 1 "PN544 transmission modes" on page 1 updated • Section 3 "Features" on page 3 updated • Section 4 "Quick reference data" on page 4 updated • Section 7 "Pinning information" on page 6 added • Updated tables in Section 8 "Communication modes" • Updated Figure 5 "FeliCa reader/writer Communication Diagram" on page 11 • Chapters Power Supply, clock supply and Interfaces integrated			
134810	19 January 2007	Objective short data sheet		Revision 0.2
Modifications:				
134802	09 January 2007	Draft		Revision 0.1
Modifications:	• Figure 1 "PN544 transmission modes" on page 1 inserted • Feature list reworked: Section 3 "Features" on page 3 • VCD mode description inserted: Section 8.1.4 "ISO/IEC 15693 VCD mode" on page 13			
134801	21 November 2006	Initial version	First version	none

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

18.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Mifare — is a trademark of NXP B.V.

19. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

20. Tables

21. Figures

continued >>

22. Contents

Date of release: 4 September 2007
Document identifier: 134812