

PMB 2100
GSM LO1 VCO



Wireless Components



Never stop thinking.

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GSM LO1 VCO

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Specification

Revision History: **2001-07-30**

PMB 2100

Previous Version: **May 2001**

Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
	15ff	AC/DC Characteristics specified vs temperature
	15	Supply current: 15.5mA max. added
	14	Supply current: 24.5mA max. at $V_{tune} < 0.5V$ added
	15/17	Control Voltage: 0.85V min. changed to 0.8V min.

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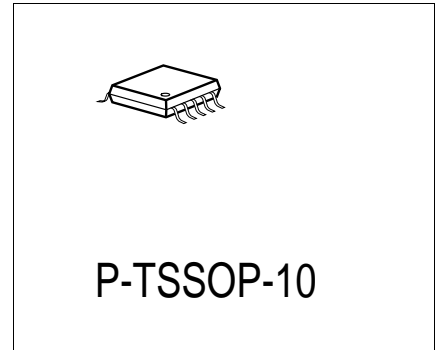
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Product Info

General Description

- The PMB 2100 is a VCO designed to be used as L01 in Dualband GSM applications with Infineon's SMARTi / SMARTi+ chipset.



Features

- Fully integrated, monolithic solution
- Very small outline and low profile P-TSSOP10 package
- Balanced outputs
- Power down function
- Supply voltage range from 2.65 - 2.95V
- -20°C to +75°C operational temperature range

Application

- L01 for GSM transceiver SMARTi/ SMARTi+

Type	Ordering Code	Package
PMB 2100	Q67034-H0003	P-TSSOP-10

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1 Product Description

1.1 Overview

- The PMB 2100 is a VCO designed to be used in Dualband GSM applications with Infineon's SMARTi/SMARTi+ chipset.

1.2 Features

- Fully integrated, monolithic solution
- Very small outline and low profile TSSOP10 package.
- Balanced outputs
- Power down function
- Supply voltage 2.65 - 2.95V
- -20°C to +75°C operational temperature range

1.3 Application

- LO1 for Dualband GSM transceivers with SMARTi/SMARTi+

1.4 Package Outlines

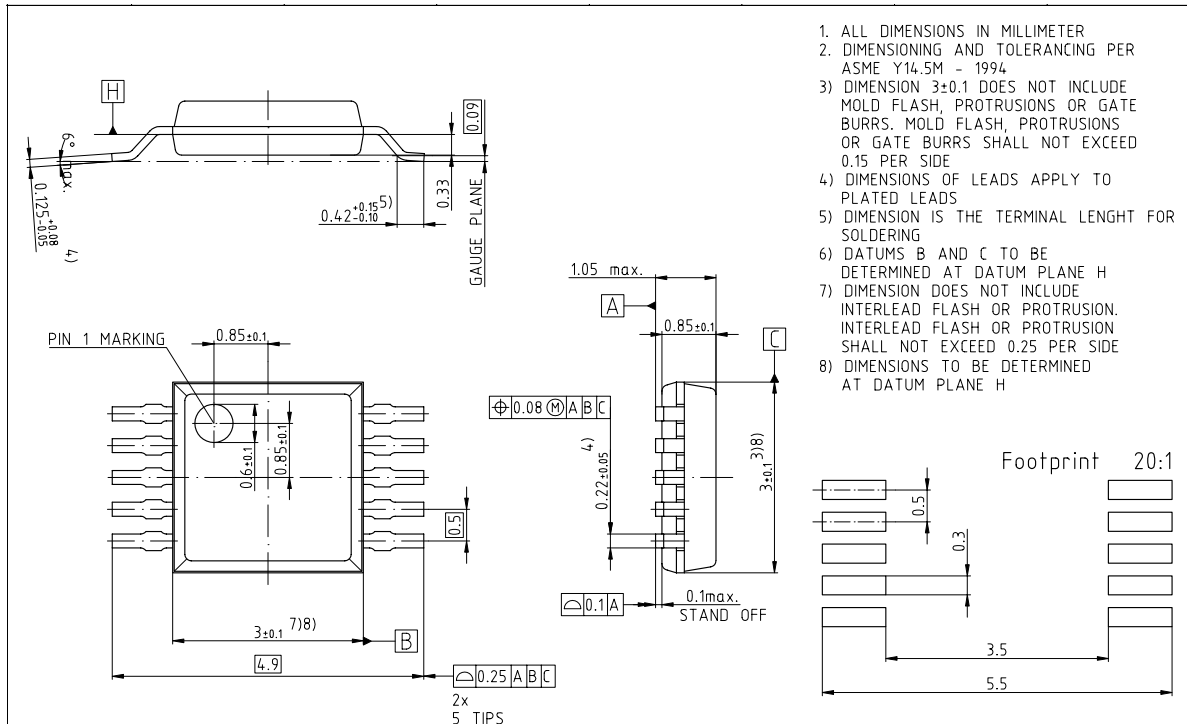
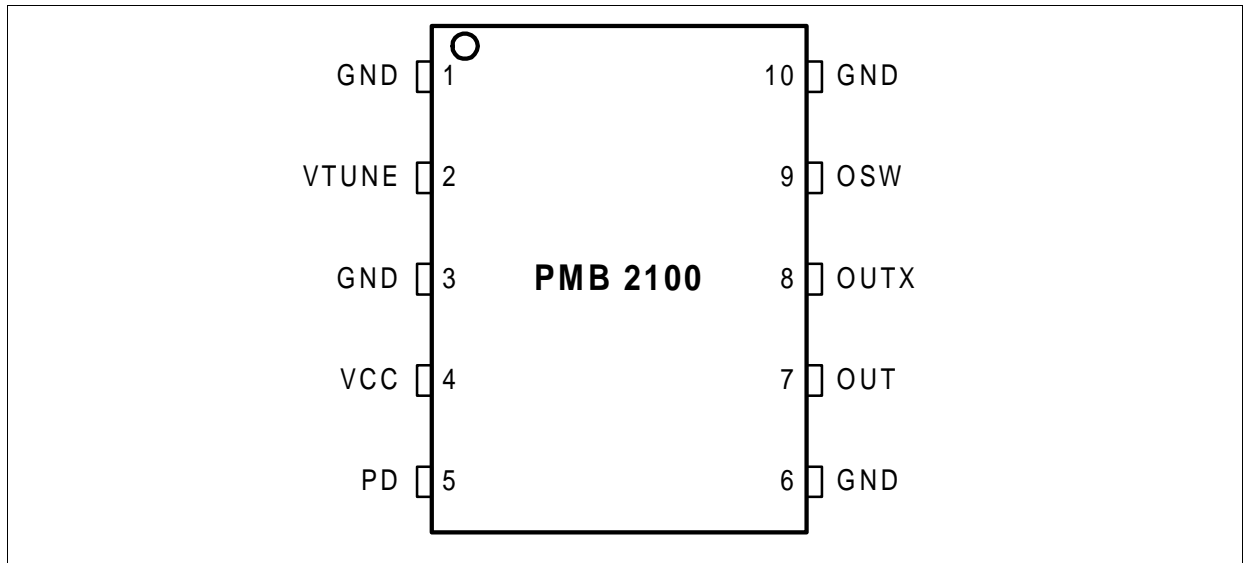


Figure 1-1 Package Outline P-TSSOP-10

2 Functional Description

2.1 Pin Configuration



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Figure 2-1 Pin Configuration

2.2 Pin Definitions and Functions

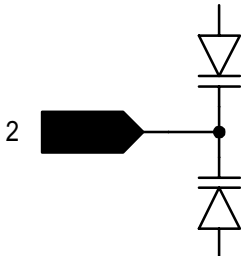
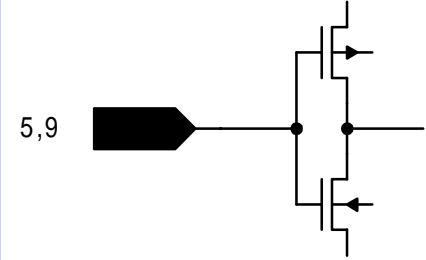
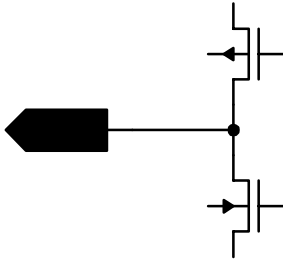
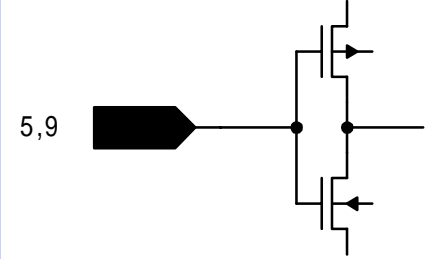
Table 2-1 Pin Definition and Function			
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	GND		Ground
2	VTUNE		Frequency control voltage input
3	GND		Ground
4	VCC		Supply voltage

Table 2-1 Pin Definition and Function (continued)			
Pin No.	Symbol	Equivalent I/O-Schematic	Function
5	PD		Power down PD=Low: VCO off PD=High: VCO on
6	GND		Ground
7	OUT		RF output
8	OUTX		RF output, inverted
9	OSW		Band select control OSW=Low: Lower Band enabled OSW=High: Higher Band enabled
10	GND		Ground

2.3 Functional Block Diagram

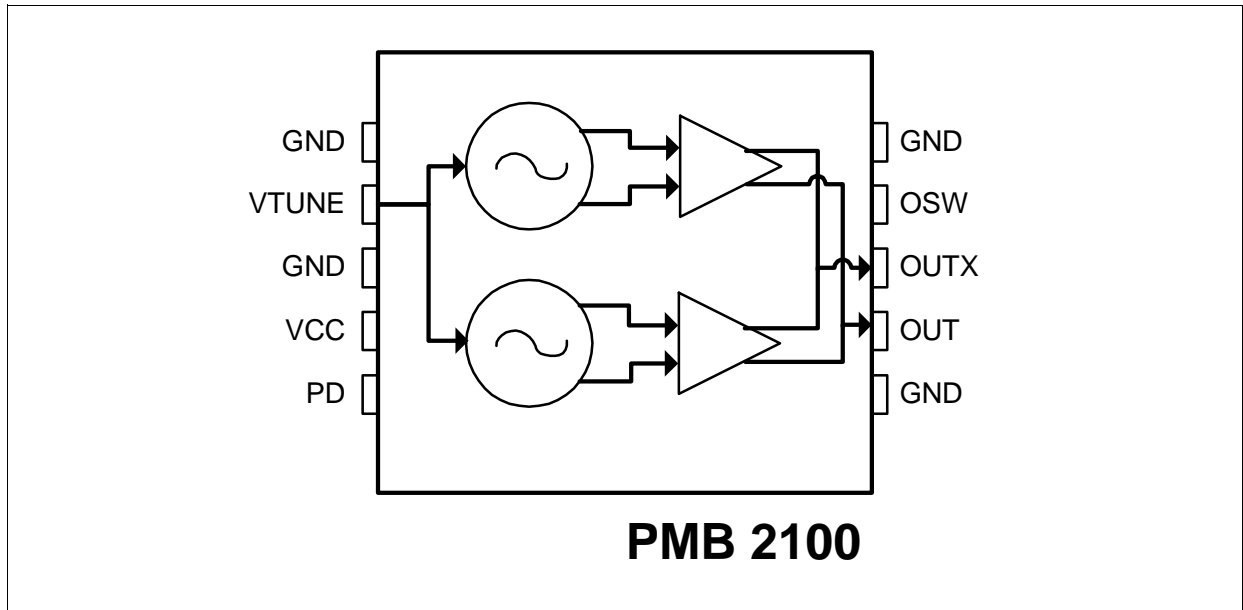


Figure 2-2 Block Diagram

2.4 Functional Block Description

The PMB 2100 contains all circuits including resonators required for a LO1 VCO for a dualband transceiver.

2.4.1 VCO core

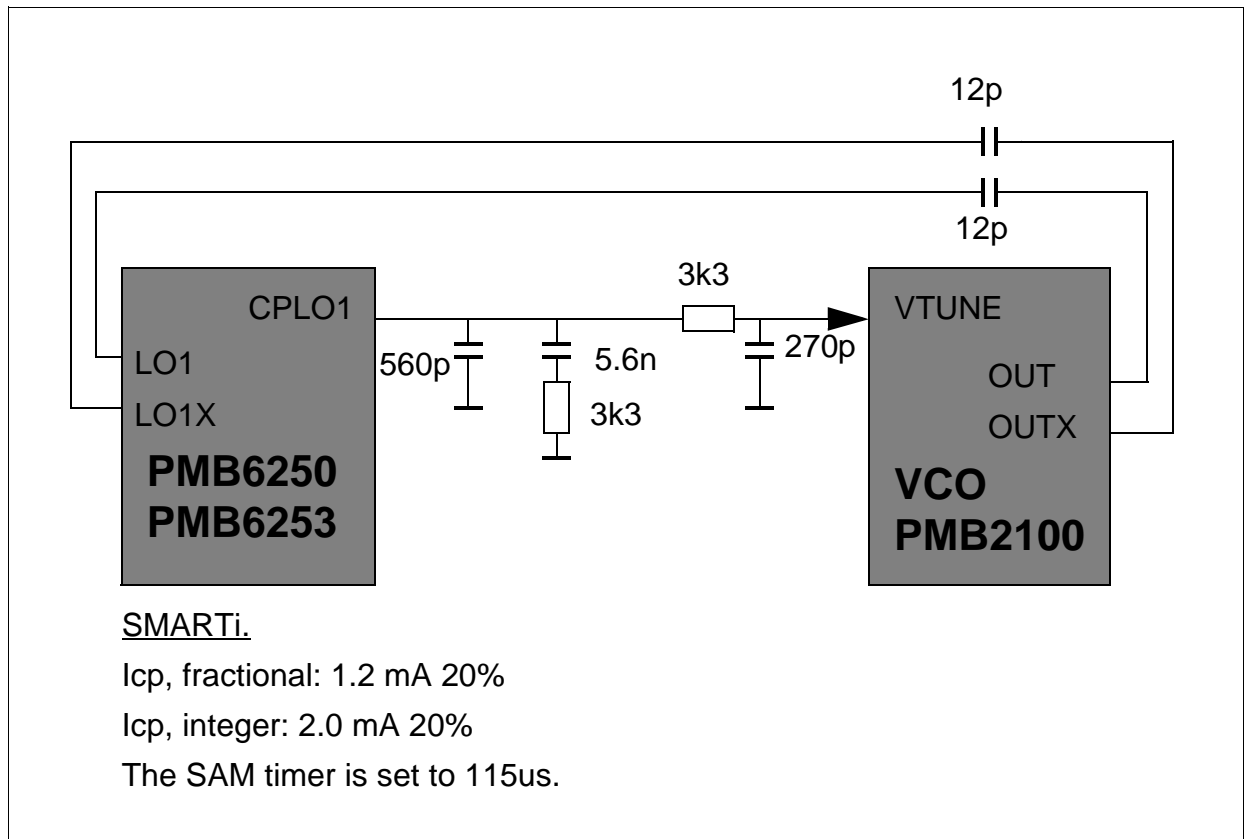
Separate VCO cores are used for the two frequency bands. The band required can be selected with the OSW pin. Both VCOs have a common frequency control input VTUNE and a common voltage supply pin VCC.

2.4.2 VCO Buffer

Separate buffers are used for both cores to amplify the VCO signals. The Outputs are combined into one output of the IC. A balanced Configuration is used for excellent even harmonic suppression. The VCO can be connected to a chip out of the Infineon SMARTi family with a minimum number of components.

3 Application

3.1 Application Circuit



Appl_circuit.wmf

Figure 3-1 Application Circuit

Locking times of less than 200us for 10° peak phase error, more than -50dB of loop suppression at 400kHz offset, a RMS phase error less than 1.5° without other impacts are typical values reached with this design.

3.2 Hints

DC blocking capacitors must be used between RF outputs and SMARTi LO1 inputs.

4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings



WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 4-1 Absolute Maximum Ratings, $T_{AMB} = -30^{\circ}\text{C} \dots + 85^{\circ}\text{C}$

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min	max		
1	Supply voltage	V_{CC}	-0.3	4.0	V	
2	Input voltage	$V_{Tune}, V_{PD}, V_{OSW}$	-0.3	$V_{CC} + 0.3$ max. 4.0V	V	
3	Output voltage	V_{Out}		V_{CC}	V	
4	Junction Temperature	T_J		125	$^{\circ}\text{C}$	
5	Storage Temperature	T_S	-40	125	$^{\circ}\text{C}$	
6	Thermal Resistance	R_{thJA}		200	K/W	
7	ESD integrity	V_{ESD}		1	kV	Human body model acc. EIA/JESD22-A114-B

4.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description.
Supply voltage $V_{CC} = 2.65$ to $2.95V$, ambient temperature $T_A = -20$ to $75^{\circ}C$, $V_{Tune}=0.8$ to $2.0V$, Output $V_{SWR}<2:1$

Table 4-2 Operating Range

#	Parameter	Symbol	Limit Values		Unit	Test Conditions	■	Item
			min	max				
Frequency								
1	Frequency Range	f_L	1285	1361	MHz	OSW=Low *)	■	
2	Frequency Range	f_H	1445	1520	MHz	OSW=High *)	■	
Control inputs								
3	Frequency Control Voltage	V_{in}	0	V_{cc}	V	Oscillation Signal available, but Frequency can be outside specified range. The AC/DC characteristic limits are not guaranteed.	■	
4	Supply current			24.5	mA	$V_{tune}<0.5V$	■	
5	Control inputs OSW, PD		0	V_{cc}	V			
6	Input capacitance OSW, PD	C_{Input}		2	pF		■	

*) Minimum frequency range covered under all operating range conditions

■ This value is guaranteed by design.

4.1.3 Current Consumption and Operation Modes

Mode	Logic		Current (typ.) [mA]		
	PD	OSW			total
Off	L	X			< 10 μ A
Low Band	H	L			12.5
High Band	H	H			12.5

All current values are measured with $V_{CC}=2.8V$.

4.1.4 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range.

Typical characteristics are the median of the production at $T_A=25^{\circ}C$.

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	Item
			min	typ	max			
VCO Core								
OSW=Low (Lower Frequency Range)								
1	Supply Current	I_{total}		12.5	15.5	mA	$T_a=-20^{\circ}C..75^{\circ}C$	1.1
2	Frequency Range	f_L	1285		1361	MHz	$T_a=-20^{\circ}C..75^{\circ}C$	2.1
3	Control Voltage	V_{Tune}	0.8		2.0	V	$T_a=-20^{\circ}C..75^{\circ}C$	3.1
4	Tuning Sensitivity $f_{OP} = 1285MHz$ $f_{OP} = 1361MHz$ (f_{OP} =operating frequency)	K_{VCO}	110 84	120 90	130 98	MHz/V	dV_{tune} measured within a $\pm 5MHz$ frequency step.	4.1
4a	Tuning Sensitivity $f_{OP} = 1285MHz$ $f_{OP} = 1361MHz$	K_{VCO}	106 81	120 90	134 101	MHz/V	dV_{tune} measured within a $\pm 5MHz$ frequency step. $T_a=-20^{\circ}C..75^{\circ}C$	4.2

Table 4-4 AC/DC Characteristics with $T_A = 25^\circ\text{C}$, $V_{CC} = 2.65\text{V}$ to 2.95V valid within the specified frequency range.

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	Item
			min	typ	max			
5	Frequency Pushing	Δf_{Push}			1.0	MHz	$V_{CC}=2.8\pm 0.1\text{V}$ $T_a=-20^\circ\text{C}..75^\circ\text{C}$	■ 5.1
6	Load Pulling	Δf_{Pull}			1.0	MHz	VSWR=2:1, all phases, reference impedance 100Ω $T_a=-20^\circ\text{C}..75^\circ\text{C}$	■ 6.1
7	SSB Phase Noise @ Δf 10kHz 400kHz 3000kHz	L_ϕ				dBc/Hz	$T_a=-20^\circ\text{C}..75^\circ\text{C}$	■ 7.1
8	Differential output power	P_{out}	-3	0	3	dBm	Load impedance 100Ω	8.1
8a	Differential output power	P_{out}	-4	0	4	dBm	Load impedance 100Ω $T_a=-20^\circ\text{C}..75^\circ\text{C}$	■ 8.2

Table 4-4 AC/DC Characteristics with $T_A = 25^\circ\text{C}$, $V_{CC} = 2.65\text{V}$ to 2.95V valid within the specified frequency range.

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	Item
			min	typ	max			
VCO core OSW=High (Higher Frequency Range)								
9	Supply Current	I_{total}		12.5	15.5	mA	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	9.1
10	Frequency Range	fH	1445		1520	MHz	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	10.1
11	Control Voltage	V_{Tune}	0.8		2.0	V	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	11.1
12	Tuning Sensitivity $f_{\text{OP}} = 1445\text{MHz}$ $f_{\text{OP}} = 1520\text{MHz}$ (f_{OP} =operating frequency)	K_{VCO}	121 94	132 101	144 110	MHz/V	dVtune measured within a $\pm 5\text{MHz}$ frequency step.	12.1
12a	Tuning Sensitivity $f_{\text{OP}} = 1445\text{MHz}$ $f_{\text{OP}} = 1520\text{MHz}$ (f_{OP} =operating frequency)	K_{VCO}	117 91	132 101	148 113	MHz/V	dVtune measured within a $\pm 5\text{MHz}$ frequency step. $T_a = -20^\circ\text{C}..75^\circ\text{C}$	12.2
13	Frequency Pushing	Δf_{Push}			1.0	MHz	$V_{\text{CC}} = 2.8 \pm 0.1\text{V}$ $T_a = -20^\circ\text{C}..75^\circ\text{C}$	13.1
14	Load Pulling	Δf_{Pull}			1.0	MHz	VSWR=2:1, all phases, reference impedance 100Ω $T_a = -20^\circ\text{C}..75^\circ\text{C}$	14.1
15	SSB Phase Noise @ Δf 10kHz 400kHz 3000kHz	L_ϕ				dBc/Hz	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	15.1
					-88 -125 -142			
					-121 -138			

Table 4-4 AC/DC Characteristics with $T_A = 25^\circ\text{C}$, $V_{CC} = 2.65\text{V}$ to 2.95V valid within the specified frequency range.

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	Item
			min	typ	max			
16	Differential output power	P_{out}	-4	-1	2	dBm	Load impedance 100Ω	16.1
16a	Differential output power	P_{out}	-5	-1	3	dBm	Load impedance 100Ω $T_a = -20^\circ\text{C}..75^\circ\text{C}$	16.2

VCO output

17	Differential output impedance	Z_{out}		100		Ω	measurement condition	17.1
18	Harmonics				-15	dBc	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	18.1
19	Non Harmonics (>20MHz)				-70	dBc	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	19.1

Control inputs

20	Frequency Control Input Current	I_{Tune}			2	nA	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	20.1
21	Control Voltage Input Capacitance	C_{Tune}	4		10	pF	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	21.1
22	Digital control inputs H-Input Voltage	V_{IH}	0.8V _{CC}			V	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	22.1
23	Digital control inputs L-Input Voltage	V_{IL}	0		0.5	V	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	23.1

Table 4-4 AC/DC Characteristics with $T_A = 25^\circ\text{C}$, $V_{CC} = 2.65\text{V}$ to 2.95V valid within the specified frequency range.

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■ Item
			min	typ	max			
24	Digital control inputs H-Input Current	I_{IH}			30	μA	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	24.1
25	Digital control inputs L-Input Current	I_{IL}	-30			μA	$T_a = -20^\circ\text{C}..75^\circ\text{C}$	25.1
26	Tswitch	t_{swON}			4	μs	Oscillation signal available after Power on or change of band $T_a = -20^\circ\text{C}..75^\circ\text{C}$	■ 26.1
27	Tswitch	t_{swOFF}			4	μs	Output power < -20dBm $T_a = -20^\circ\text{C}..75^\circ\text{C}$	■ 27.1

■ guaranteed by design.

4.2 Output Impedance

Table 4-5 Output Impedance

Pin	f	
OUT	1400	$(20-j37)\Omega$
OUTX	1400	$(20-j37)\Omega$

Note: Values are simulated.

Differential output impedances are single ended impedances for each pin.

4.3 Test Conditions

Unless otherwise specified, the performance indicated in this section shall be achievable using an FR4 circuit board, with a solid ground plane as the secondary layer.

4.4 Test Circuit

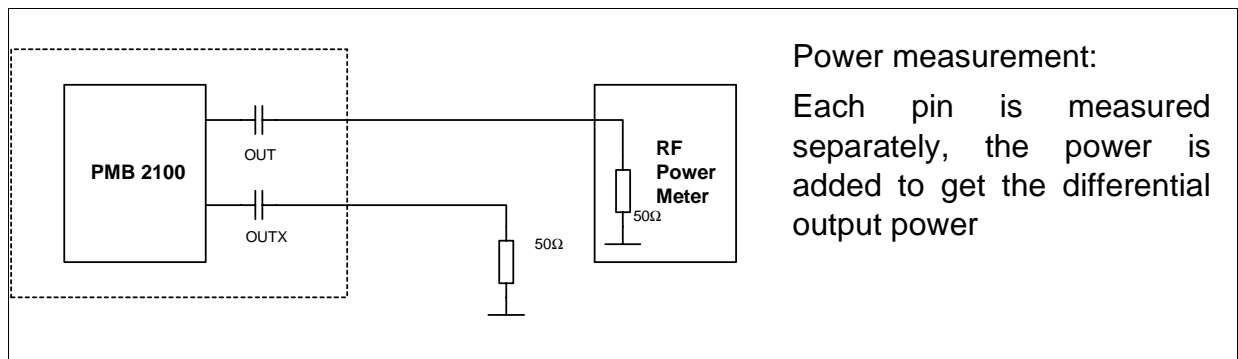


Figure 4-1 Test Circuit