Dual Serial Link, PHY Multiplexer

FEATURES

- Integrated analog/digital device that interfaces a UTOPIA L2 bus to a serial backplane with optional 1:1 protection using high speed Low Voltage Differential Signal (LVDS) serial links.
- For framers or modems without UTOPIA bus interfaces: optionally provides cell delineation (I.432) across 16 clock and data (bit serial) interfaces.
- Interworks with PM7351 S/UNI-VORTEX devices to implement a point-to-multipoint serial backplane architecture, with optional 1:1 protection of the common card.
- Interfaces to another S/UNI-DUPLEX device (via a single LVDS link) to create a simple point-to-point "UTOPIA bus extension" capability.
- Interfaces to two S/UNI-DUPLEX devices to create a 1:1 protected bus extension.
- Requires no external memory devices.
- Low power 3.3V CMOS technology.
- Standard 5 pin P1149 JTAG port.
- 160 ball PBGA, 15mm x 15mm.
- In the LVDS receive direction: selects traffic from the LVDS link marked active and demultiplexes the individual cell streams to the appropriate PHY device.
- In the LVDS transmit direction: accepts 52-56 byte cell streams from up to 32 UTOPIA L2 compatible PHY devices, multiplexing into a single cell stream carried over two high speed LVDS serial interfaces.
- Cell read/write to both LVDS links available through the processor port. Provides optional hardware assisted CRC32 calculation across cells to support an embedded inter-processor communication channel across the LVDS links.

PHY/FRAMER INTERFACES

One of three modes can be selected:

- 8/16 bit, 33 MHz UTOPIA L2 bus master (also supports expanded length cells).
- 8/16 bit, 52 MHz extended UTOPIA L2 bus slave (compatible with PM7351 S/UNI-VORTEX).
- 16 port, 4 pin clocked serial data interface (Tx & Rx), with integrated I.432 ATM cell delineation.

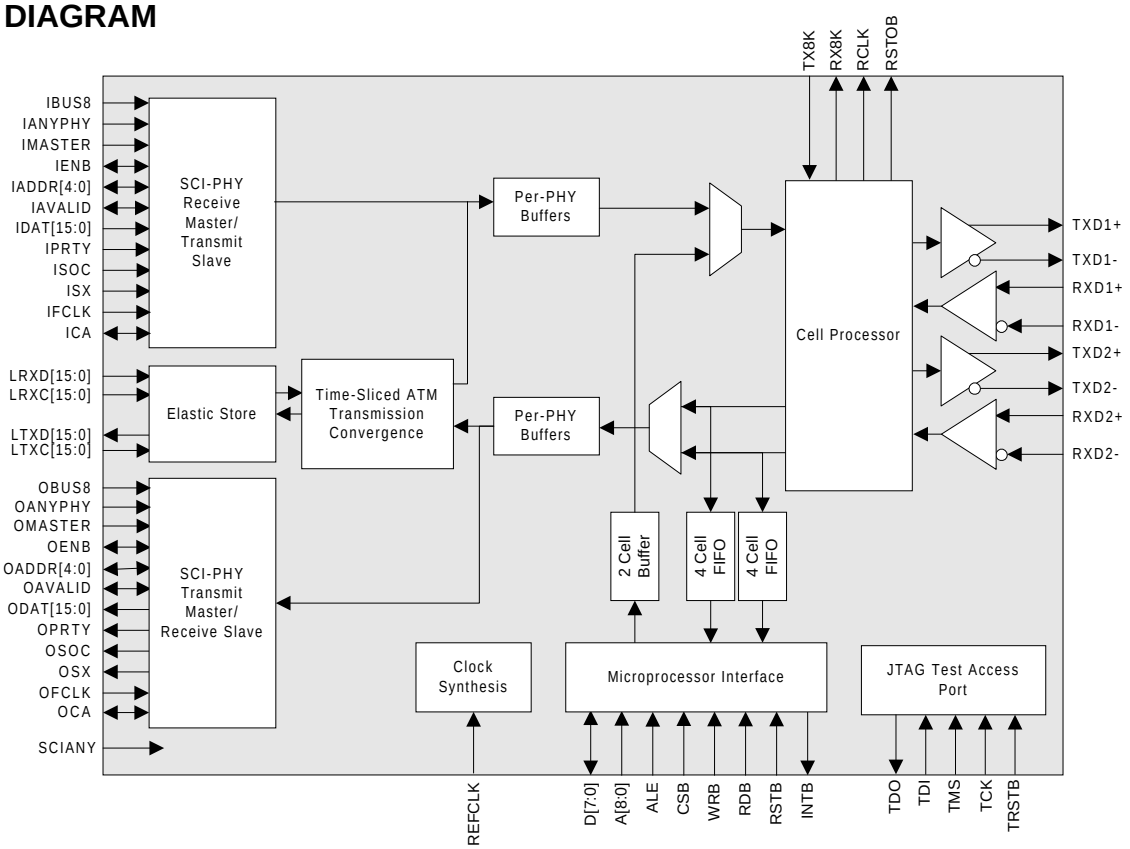
LVDS INTERFACES

- Dual 4 wire LVDS serial transceivers each operating at up to 200 Mb/s.
- Operates across PCB or backplane traces, or across up to 10 meters of 4 wire twisted pair cabling for inter-shelf communications.
- Fully integrated LVDS clock synthesis and recovery. No external analog components are required.
- Usable bandwidth (excludes system overhead) of 186 Mb/s.

LVDS TRANSMIT DIRECTION

- Simple round-robin multiplex of up to 32 PHYs (or 16 clock/data interfaces) plus the microprocessor port's cell transfer buffer.
- Multiplexed cell stream broadcast to both LVDS simultaneously.

BLOCK DIAGRAM



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- 6 bit port ID prepended to each cell for use by ATM layer to identify cell source (1 of 32 PHYs or processor).
- Back-pressure provided by far end (active link only) to prevent overflow of far end receiver.

LVDS RECEIVE DIRECTION

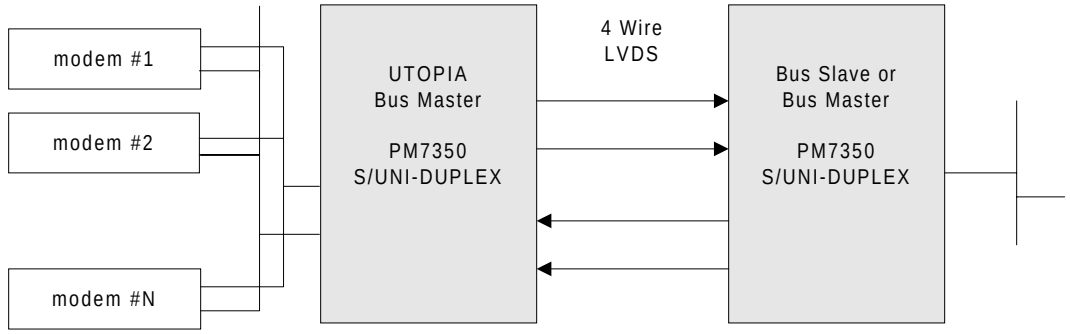
- The LVDS link marked as "spare" is monitored for errors, PHY cells are discarded, microprocessor port cells are accepted.
- Individual PHY and microprocessor FIFO back-pressure indications are sent to the far end to prevent FIFO overflows. Per stream backpressure prevents head-of-line blocking.
- Cells received from the active LVDS link are forwarded to the appropriate PHY, bit serial interface, or the microprocessor port as specified by a 6 bit port ID added to each cell at the far end device.

APPLICATIONS

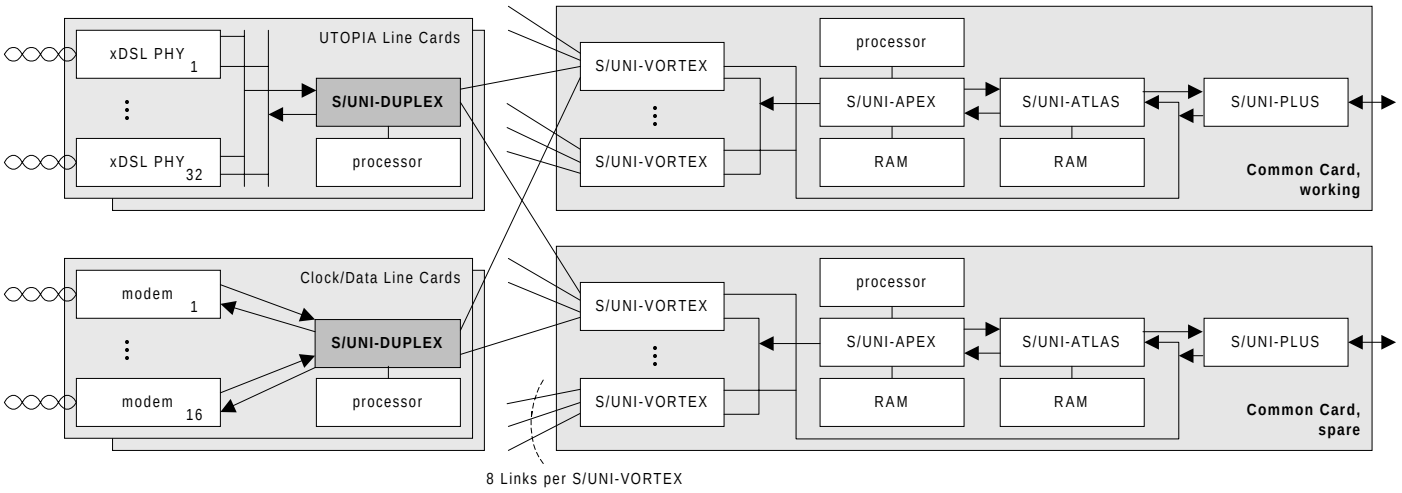
- Single shelf or multi-shelf Digital Subscriber Loop Access Multiplexer (DSLAM).
- ATM/frame/IP switch or multiservice access multiplexer.
- UMTS wireless base station and base station controller.

TYPICAL APPLICATIONS

INTER-SHELF UTOPIA BUS EXTENSION



MULTI-SHELF 1024 LINE ATM DSLAM



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