PM7350

S/UNI-DUPLEX™

S/UNI-DUPLEX

DUAL SERIAL LINK, PHY MULTIPLEXER

DATA SHEET

RELEASED

ISSUE 5: APRIL 2000

REVISION HISTORY

Issue No.	Issue Date	Originator	Details of Change
Issue 5	April 2000	Phil Walston	Updated analog parameters, I_{DDOP}, thermal info and corrected register description typos. Release to production.
Issue 4	February 2000	Phil Walston	Updated to incorporate Revision B changes outinled in previous Errata. Change bars highlight specific changes.
Issue 3	June 1999	James Lamothe	Changed confidentiality notices for document's public release.
Issue 2	May, 1999	Jeff Brown	Extensive updates throughout
Issue 1	May, 1998	Jeff Brown	First release

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1 FEATURES

- Integrated analog/digital device that interfaces a high-speed parallel bus to a high speed Low Voltage Differential Signal (LVDS) serial link with optional 1:1 protection.
- For framers or modems without Utopia bus interfaces the S/UNI-DUPLEX provides cell delineation (I.432) across 16 clock and data (bit serial) interfaces.
- Fault detection, redundancy, protection switching, and inserting/removing cards while the system is running (hot swap).
- Interface to other S/UNI-DUPLEX or S/UNI-VORTEX, to satisfy a full set of system level requirements for backplane interconnect:
    - Transports user data by providing the inter-card data-path.
    - Inter-processor communication by providing an integrated inter-card control channel.
    - Exchanges flow control information (back-pressure) to prevent data loss.
    - Provides embedded command and control signals across the backplane: system reset, error indications, protection switching commands, etc.
    - Clock/timing distribution (system clocks as well as reference clocks such as 8 kHz timing references).
- When used as a parallel bus slave device, can be configured to share the bus with other S/UNI-DUPLEX bus slave devices.
- Can interface to another S/UNI-DUPLEX device (via a single LVDS link) to create a simple point-to-point "Utopia bus extension" capability.
- Can interface to two S/UNI-DUPLEX devices to create a 1:1 protected bus extension.
- Interworks with PM7351 S/UNI-VORTEX devices to implement a point-to-multipoint serial backplane architecture, with optional 1:1 protection of the common card.
- In the LVDS receive direction: selects traffic from the LVDS link marked active and demultiplexes the individual cell streams to the appropriate PHY device.

- Cell read/write to both LVDS links available through the processor port. Provides optional hardware assisted CRC32 calculation across cells to support an embedded inter-processor communication channel across the LVDS links.
- Requires no external memories.
- Standard 5 pin P1149.1 JTAG test port.
- Low-power, 3.3V CMOS technology.
- 160-pin high-performance plastic ball grid array (PBGA) package.

2 APPLICATIONS

- Single shelf or multi-shelf Digital Subscriber Loop Access Multiplexer (DSLAM).
- ATM, frame relay, IP switch.
- Multiservice access multiplexer.
- Universal Mobile Telecommunication System (UMTS) wireless base stations.
- 16 channel cell delineation (I.432 transmission convergence processing).

3 REFERENCES

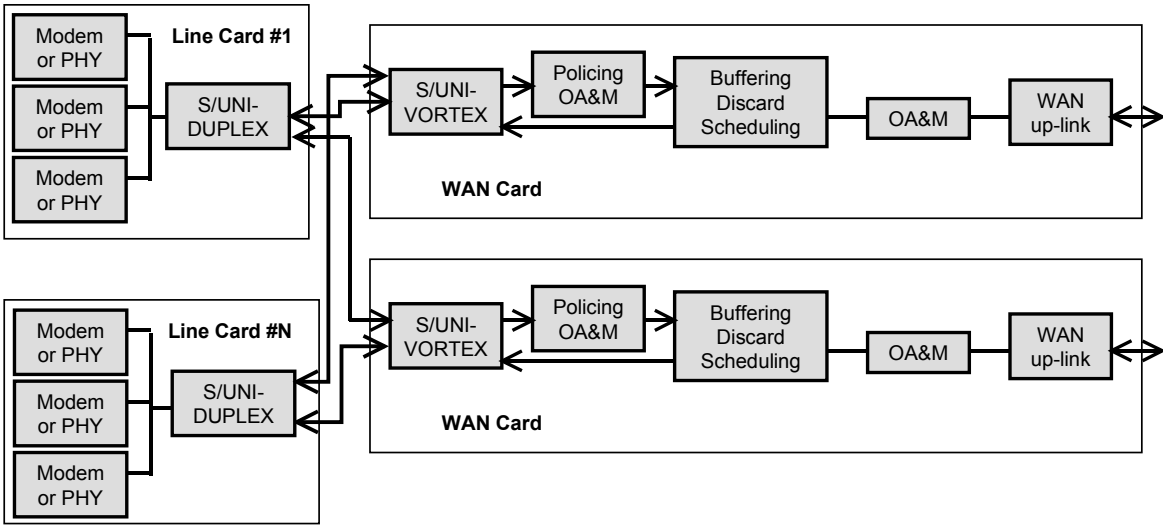
- PMC-Sierra; “Saturn Compatible Interface For ATM PHY Layer And ATM Layer Devices, Level 2”; PMC-940212; Dec. 8, 1995
- ATM Forum, “Universal Test & Operations PHY Interface for ATM (UTOPIA), Level 2”, Version 1.0, af-phy-0039.000, June 1995
- PMC-Sierra; “Saturn Interface Specification And Interoperability Framework For Packet And Cell Transfer Between Physical Layer And Link Layer Devices”, PMC-980902, Draft
- Draft American National Standard for Telecommunications T1.413 Issue 2, “Network and Customer Installation Interfaces - Asymmetric Digital Subscriber Line (ADSL) Metallic Interface”, ANSI T1.413-1998, November 1998
- ITU-T Recommendation I.432.1, “B-ISDN user-network interface – Physical layer specification: General characteristics”, 08/96

4 APPLICATION EXAMPLES

When designing communication equipment such as access switches, multiplexers, wireless base stations, and base station controllers the equipment architect is faced with a common problem: how to efficiently connect a large number of lower speed ports to a small number of high speed ports? Typically, a number of line-side ports (analog modems, xDSL modems ATM PHYs, or RF modems) are terminated on each line card. Numerous line cards are then slotted into one or more shelves and backplane traces or inter-shelf cables are used to connect the line cards to a centralized (often 1:1 protected) common card, hereafter referred to as the core card. The core card normally includes one or more high speed WAN up-link ports that transport traffic to and from a high speed broadband network.

A block diagram of a 1:1 redundant system is shown in Fig. 1.

Fig. 1 Typical Target Application



In this type of equipment the majority (perhaps all) user traffic goes from WAN port to line port, or from line port to WAN port. Although the individual ports on the line cards are often relatively low speed interfaces such as T1, E1, or xDSL, there may be many ports per line card and many line cards per system, resulting in hundreds or even thousands of lines terminating on a single WAN up-link. In the upstream direction (from line card to WAN up-link), the equipment must have capacity to buffer and intelligently manage bursts of upstream traffic simultaneously from numerous line cards.

In the downstream direction the equipment must handle a similar issue, the “big pipe feeding little pipe” problem. When a large burst of traffic destined for a single line port is received at the high speed WAN port it must be buffered and managed as it queues up waiting for the much lower speed line port to clear.

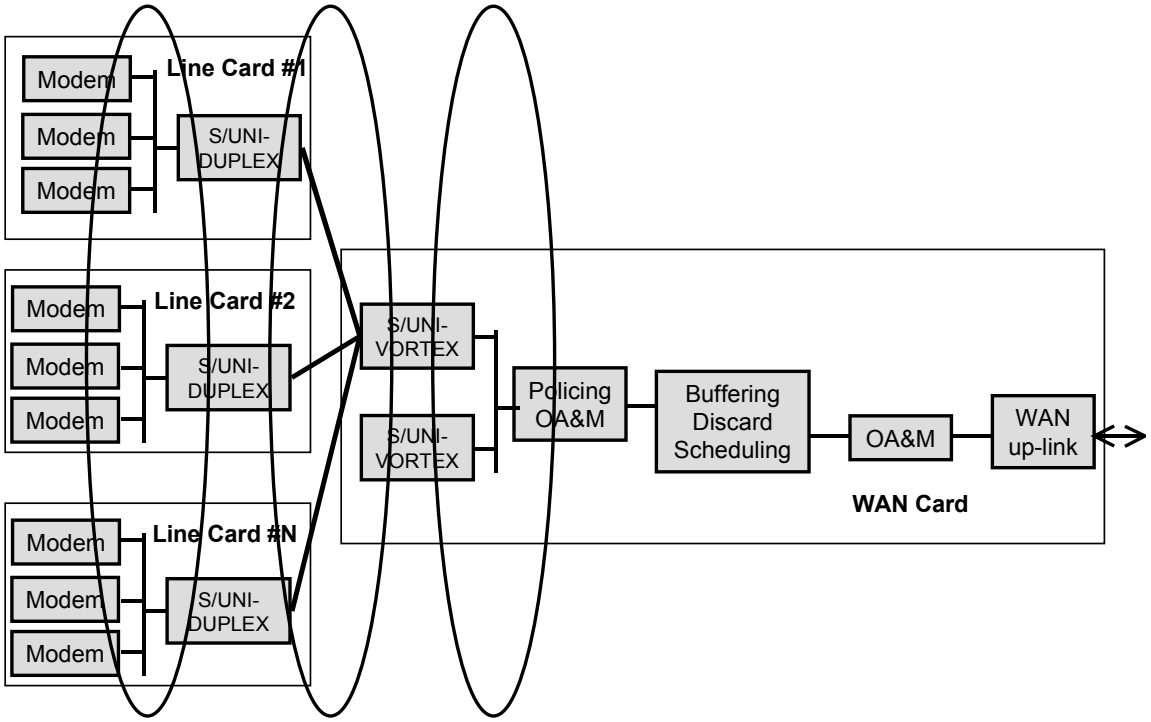
The line cards are always the most numerous cards in this type of equipment. An individual line card, even if it terminates a few dozen low speed ports, does not generate or receive enough traffic to justify putting complex buffering and traffic management devices on it. The ideal architecture has low cost “dumb” line cards and a feature rich, “smart” core card. In order to enhance fault tolerance, the architecture should also inherently support 1:1 protection using a redundant core card and WAN up-link without significantly increasing line card complexity.

A system architecture that keeps buffering and traffic management off the line card with typically exhibit the following features:

1. Connection setup is simpler both in terms of programming and during execution because there is minimal or no requirement for line intervention during the connection setup process.
2. In-service feature upgrades are simpler because feature complexity is limited to the common equipment.
3. Component costs are reduced, while system reliability increases due to reduced component count.

In this type of architecture there are often three stages of signal concentration or multiplexing, as shown in Fig 2.

Fig. 2 Three Stage Multiplex Architecture



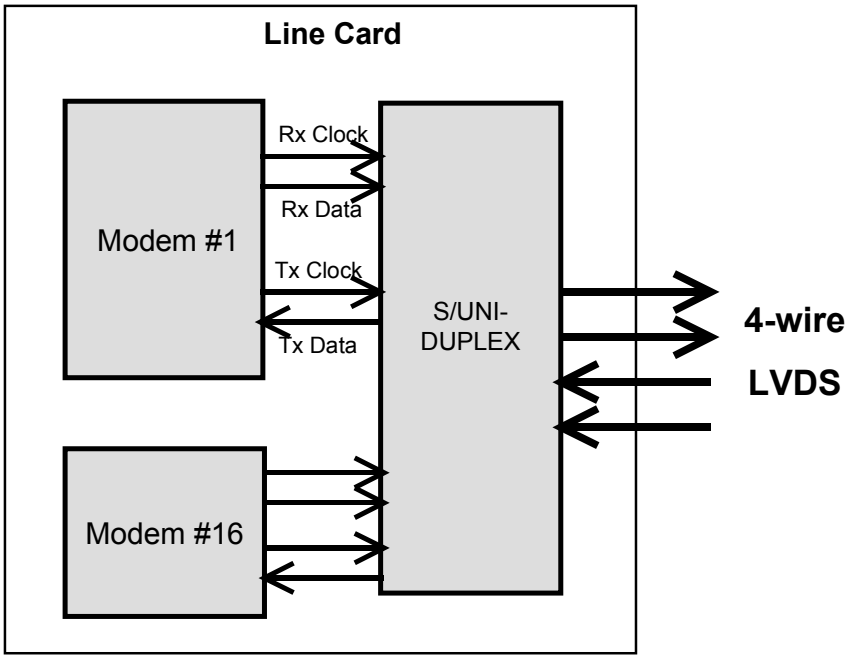
The first stage resides on the line card and spans only those ports physically terminated by that card. Since it is confined to a single card, this first stage of multiplexing readily lends itself to the simple parallel bus based multiplex topology implemented by the S/UNI-DUPLEX. The second stage of concentration occurs between the core card(s) and the line cards, including line cards that are on a separate shelf. This second stage is best served by a redundant serial point-to-point technology. The third stage of multiplexing is optional and resides on the core card. This third stage is used in systems with a large number of line cards that require several devices to terminate the second stage of aggregation. Since the third stage of aggregation is confined to the core card, it lends itself readily to a parallel bus implementation. This three stage approach is implemented directly by the S/UNI-DUPLEX and its sister device, the S/UNI-VORTEX.

The S/UNI-DUPLEX acts as the line card's bus master. It implements the first stage of multiplexing by routing traffic from the PHYs and transmitting the traffic simultaneously over two high speed (200 Mbps) serial 4-wire LVDS links. One serial link attaches to the active core card, the other to the standby core card. In the downstream direction the S/UNI-DUPLEX demultiplexes traffic from the active core card's LVDS serial link and routes this traffic to the appropriate PHYs. If the active core card (or its LVDS link) should fail, protection switching commands embedded in the spare LVDS link will direct the S/UNI-DUPLEX to start receiving its traffic from this spare link.

The S/UNI-VORTEX resides on the core card and terminates up to 8 LVDS links connected to 8 S/UNI-DUPLEX devices. The S/UNI-VORTEX implements the second stage of multiplexing. More than one S/UNI-VORTEX will be required if more than 8 links are required – as will be the case for a system with more than 8 line cards. The S/UNI-VORTEX device(s) share a high speed parallel bus with the core card's traffic management and OA&M layers, as implemented by devices such as PMC-Sierra's S/UNI-APEX and the S/UNI-ATLAS.

Some applications use framer or modem devices without integrated I.432 processing[1] normally support a clock and data interface, and rely on external circuitry to detect and generate ATM cell framing and overhead. To support these applications, the S/UNI-DUPLEX provides a clock and data mode[2]. In this mode, the input/output pins that normally interface to the Utopia bus are configured to support up to 16 clock and data serial interfaces. This type of line card is shown in Fig. 3. The I.432 processing is transparent to the far end device, which implies that a single S/UNI-VORTEX can simultaneously interface to line cards that implement the Utopia bus and to line cards that use clock and data interfaces.

Fig. 3 Clock and Data PHY Interface



Some PHY devices provide a 3-line interface consisting of clock, data, and overhead indication. For these PHYs external circuitry can be used to adapt to the S/UNI-DUPLEX's 2-line interface.

[1] Cell delineation, payload scrambling-descrambling, idle cell generation/discard, etc..

[2] Either Utopia mode or clock and data mode can be selected, but not both at once.

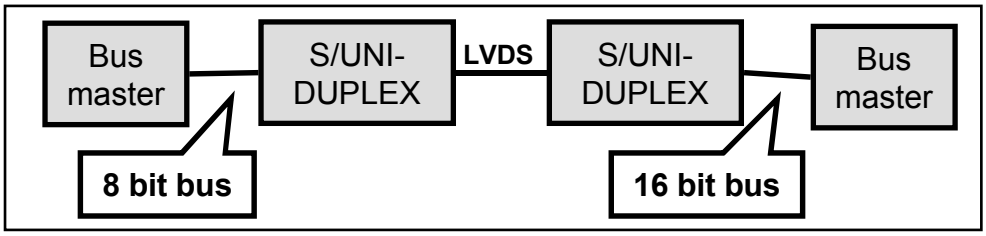
In the clock and data receive direction the S/UNI-DUPLEX performs bit level ATM cell delineation function. In the transmit direction the S/UNI-DUPLEX can operate in either bit or frame aligned mode. In frame mode (also called byte aligned mode) the two wire transmit interface continuously monitors for gaps in the transmit clock to determine where the frame or byte alignment should occur. The circuitry assumes that when a gap in the transmit clock is detected this is either the framing bit position (e.g. the DS-1 framing bit) or an overhead byte (e.g. ADSL modem). In either case the next clock period after the gap is assumed to represent the byte alignment position.

In the multiplexer application discussed previously the S/UNI-DUPLEX's LVDS interfaces are connected to one or two S/UNI-VORTEX devices. It is also possible to interface S/UNI-DUPLEX to S/UNI-DUPLEX via the LVDS link. Since the S/UNI-DUPLEX bus interface can be configured in several ways (clock and data, 8/16 bits bus master, 8/16 bit bus slave) there are various applications where two S/UNI-DUPLEX devices can be used "back-to-back" in order to perform one or more of the following functions:

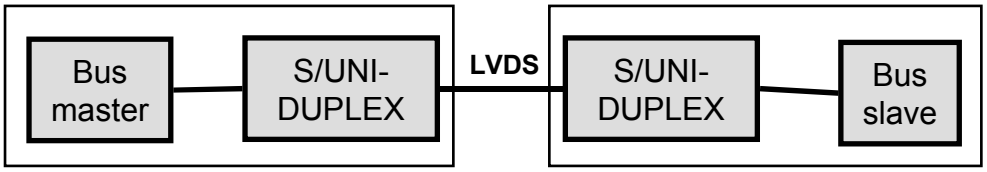
1. Interfacing a bus master device to another bus master.
2. Interfacing a bus slave device to another bus slave.
3. Converting between 8 bit and 16 bit buses.
4. Off card or off shelf bus extension.
5. Cell delineation (I.432 processing).
6. Protection switching.

Examples of these types of configurations are shown in Fig. 4 and Fig. 5.

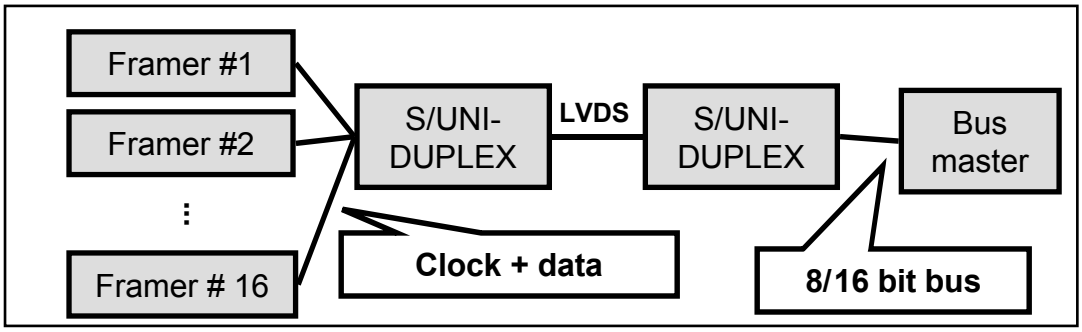
Fig. 4 S/UNI-DUPLEX to S/UNI-DUPLEX Applications



Example of on-card bus conversion:
8 bit bus master to 16 bit bus master

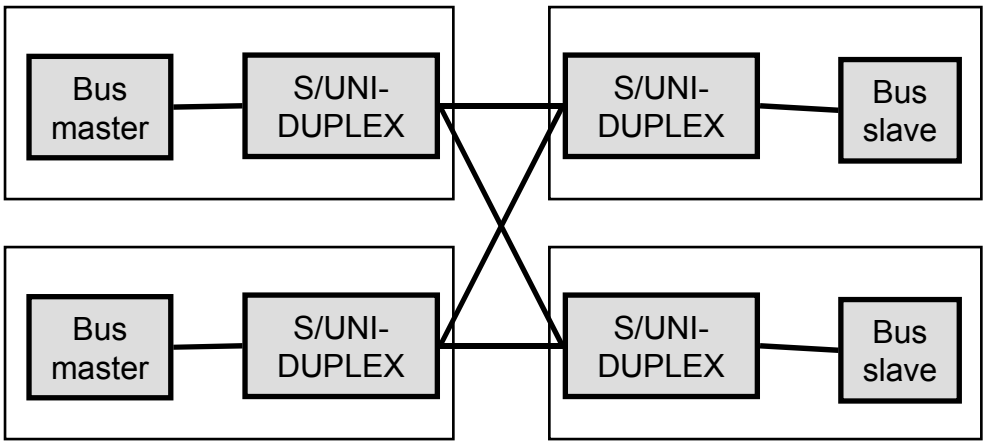


Example of basic bus extension between cards



Example of on-card I.432 processing

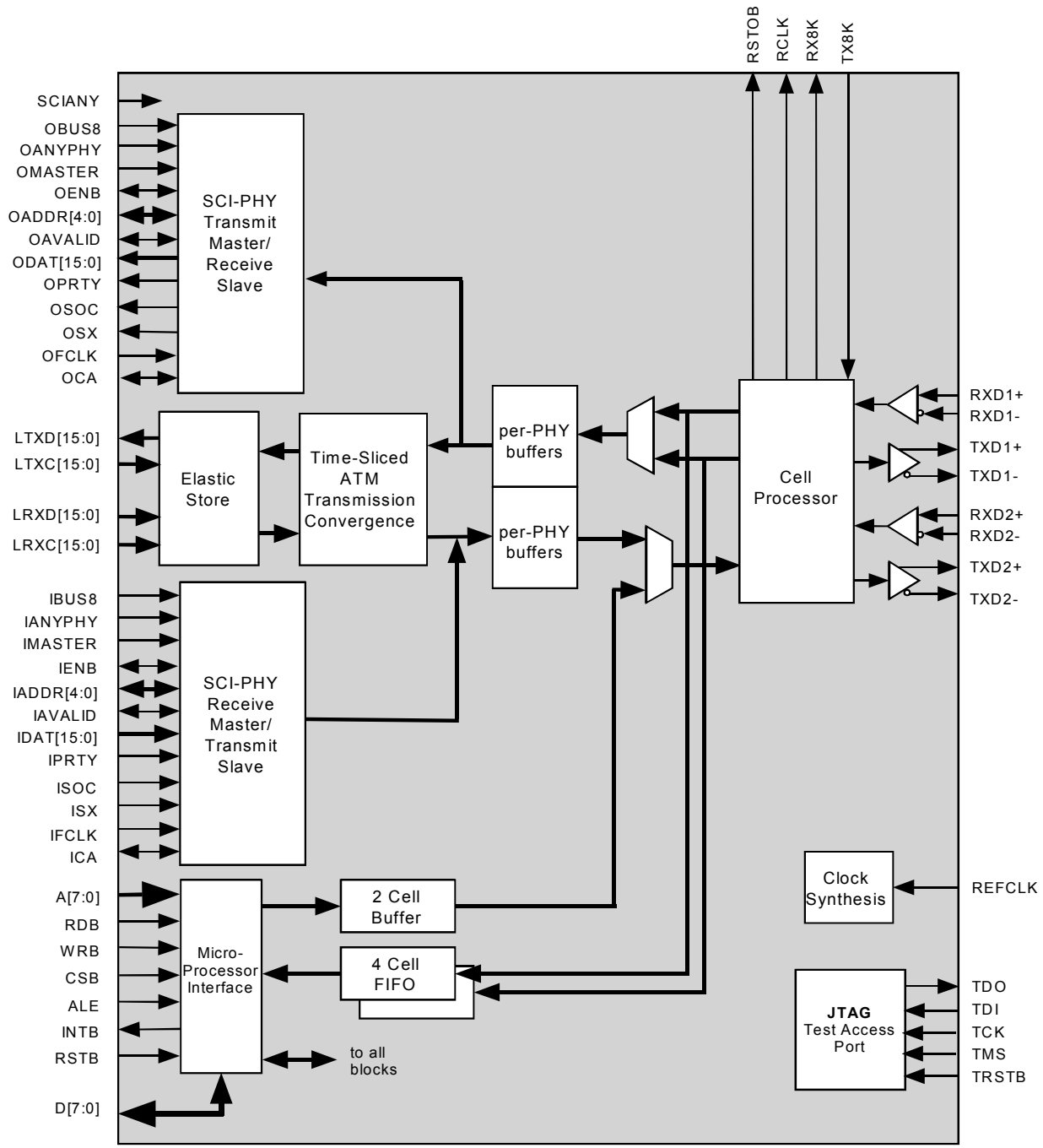
Fig. 5 S/UNI-DUPLEX to S/UNI-DUPLEX Protection Switching



Example of protection switching between cards

5 BLOCK DIAGRAM

Although separated to improve clarity, many signals in the following diagram share physical package pins. The use of the SCI-PHY/Any-PHY interfaces and the clocked serial data interfaces is mutually exclusive.



6 DESCRIPTION

The PM7350 S/UNI-DUPLEX is a monolithic integrated circuit typically used with its sister device, the S/UNI-VORTEX, to implement a point-to-point serial backplane interconnect architecture. The primary role of the S/UNI-DUPLEX is to interface to up to 32 devices (typically framers or PHYs) and transfer 52-56 byte data cells in serial format to/from a backplane. Devices interface to the S/UNI-DUPLEX via an 8 or 16-bit SCI-PHY/Utopia/Any-PHY bus, or optionally via a 16 port clock and data interface.

Each S/UNI-DUPLEX can connect to two 100 to 200 Mb/s Low Voltage Differential Signal (LVDS) serial links. A microprocessor port provides access to internal configuration and monitoring registers. The microprocessor port may also be used to insert and extract cells in support of an embedded microprocessor communication channel.

BUS INTERFACE:

One of four modes can be selected:

- 8 or 16 bit, Utopia L2 bus master operating at up to 33 MHz bus clock frequency. Also supports PMC-Sierra's SCI-PHY bus standard which is compatible with Utopia L2 but allows extended length cells and supports an additional bus address signal in order to support 32 PHY devices rather than Utopia's 31. See Table 1 for a comparison of these bus standards.
- 16 port, 4 pin clocked serial data interface (Tx, TxClk, Rx, RxClk), with integrated I.432 ATM cell delineation operating at up to 52 MHz serial clock frequency.
- 8 or 16 bit, SCI-PHY/Utopia bus slave operating at up to 52 MHz bus clock frequency. The slave input port presents itself as 32 addressable logical channels. The slave output port appears as a single addressable channel carrying the multiplexed traffic from up to 32 logical channels where each cell's channel number can optionally be embedded in the H5 header field (Utopia bus mode) or indicated in a cell prepend (SCI-PHY bus mode).
- 8 or 16 bit, Any-PHY bus slave (bus protocol compatible with the PM7351 S/UNI-VORTEX) operating at up to 52 MHz bus clock frequency. The slave input port presents itself as 32 addressable logical channels. The slave output port appears as a single addressable channel carrying the multiplexed traffic from up to 32 logical channels. In both directions each cell's logical channel number is indicated in a cell prepend.

LVDS INTERFACES (both directions):

- Dual 4-wire LVDS serial transceivers each operating at 100 to 200 Mbps across PCB or backplane traces, or across up to 10 meters of 4-wire twisted pair cabling for inter-shelf communications.
- Full integrated LVDS clock synthesis and recovery. No external analog components are required.
- Usable bandwidth (excludes system overhead) of 186 Mbps.

LVDS TRANSMIT DIRECTION

- Simple round robin multiplex of up to 32 PHYs (or 16 clock and data interfaces) plus the microprocessor port's cell transfer buffer.
- Multiplexed cell stream broadcast to both LVDS simultaneously.
- 6 bit port ID prepended to each cell for use by ATM layer to identify cell source (1 of 32 PHYs or processor).
- Back-pressure provided by far end (active link only) to prevent overflow of far end receiver.

LVDS RECEIVE DIRECTION

- Cells received from the active LVDS link are forwarded to the appropriate PHY, bit serial interface, or the microprocessor port as specified by a 6 bit port ID added to each cell at the far end device.
- The LVDS link marked as "spare" is monitored for errors, PHY cells are discarded, microprocessor port cells are accepted.
- Individual PHY and microprocessor FIFO back-pressure indications are sent to the far end to prevent FIFO overflows. Per stream back-pressure prevents head-of-line blocking.

MICROPROCESSOR INTERFACE

- 8 bit data bus, 8 bit address bus.
- Provides read/write access to all configuration and status registers.
- Provides CRC32 calculation and cell transfer registers to support an embedded microprocessor to microprocessor communication channel over the LVDS link.

7 PIN DIAGRAM

The S/UNI-DUPLEX is packaged in a 160-pin plastic ball grid array (PBGA) package having a body size of 15 mm by 15 mm and a ball pitch of 1.00 mm.

	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A		TRSTB	TDI	A[2]	RSTB	A[6]	RDB	BIAS	IMASTER LTXD[15]	IADDR[3] LRXC[15]	IADDR[1] LRXD[14]	ICA LRXC[13]	RSTOB	
B	TX8K	TCK	TMS	A[0]	A[4]	A[5]	ALE	INTB	IAVALID LTXC[15]	VSS	IENB LRXD[13]	VDD	IPRTY LTXD[13]	IDAT[15] LTXC[13]
C	D[7]	VDD	VSS	A[1]	VSS	A[7]	VSS	SCIANY	IBUS8 LTXD[14]	VDD	IADDR[0] LRXC[14]	VSS	IDAT[14] LTXD[12]	IDAT[13] LTXC[12]
D	D[4]	D[6]	D[5]	A[3]	VDD	WRB	CSB	VSS	IADDR[4] LRXD[15]	IADDR[2] LTXC[14]	VSS	IDAT[11] LRXC[12]	IDAT[12] LRXD[12]	IDAT[10] LTXD[11]
E	VDD	RX8K	VSS	RCLK							IDAT[7] LRXC[11]	IDAT[8] LRXD[11]	VDD	IDAT[9] LTXC[11]
F	D[0]	D[2]	D[1]	D[3]							IFCLK LTXC[9]	VDD	IDAT[6] LTXD[10]	IDAT[5] LTXC[10]
G	RXD1+	RXD1-	RES	TAVD			GND	GND			IDAT[3] LTXD[8]	IDAT[1] LTXD[7]	VSS	IDAT[4] LTXD[9]
H	TXD1+	TXD1-	TAVS	RESK			GND	GND			ISX LTXC[6]	IDAT[2] LTXC[8]	ISOC LTXD[6]	IDAT[0] LTXC[7]
J	RXD2+	RXD2-	RAVS	RAVD							ODAT[15] LRXC[10]	VSS	OPRTY LRXD[10]	IANYPHY LTXD[5]
K	TXD2+	TXD2-	TAVS	TAVD							VSS	ODAT[14] LRXD[9]	ODAT[13] LRXC[9]	VDD
L	ATP0	ATP1	CAVS	CAVD	OADDR[1] LRXD[0]	VDD	VSS	OSOC LRXD[3]	ODAT[2] LRXD[4]	ODAT[4] LRXC[6]	VDD	ODAT[12] LTXC[5]	ODAT[11] LRXD[8]	VDD
M	QAVS	QAVD	VDD	OMASTER LTXD[1]	OADDR[3] LTXC[1]	OAVALID LRXD[1]	VSS	VDD	VSS	OANYPHY LTXD[2]	ODAT[5] LRXD[6]	ODAT[9] LTXC[4]	VSS	ODAT[10] LRXC[8]
N	VSS	VDD	Unused LTXD[0]	VSS	OADDR[2] LTXC[0]	OADDR[4] LRXC[1]	OCA LRXC[2]	ODAT[1] LRXC[4]	ODAT[3] LRXD[5]	OFCLK LRXC[5]	ODAT[6] LRXC[7]	VDD	ODAT[8] LTXC[3]	Unused LTXD[3]
P		TDO	REFCLK	OADDR[0] LRXC[0]	VSS	OENB LRXD[2]	OSX LRXC[3]	ODAT[0] LTXC[2]	VDD	VSS	OBUS8 LTXD[4]	VSS	ODAT[7] LRXD[7]	

BOTTOM VIEW

8 PIN DESCRIPTION

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
RXD1+ RXD1- RXD2+ RXD2-	Diff. LVDS Input	G14 G13 J14 J13	The high-speed receive data (RXD1+/-, RXD2+/-) inputs present NRZ data from a serial backplane. Two pairs are provided for redundancy. The active link may be chosen by the local microprocessor or determined by a simple handshake. RXD1+/- and RXD2+/- are truly differential inputs offering superior common-mode noise rejection. They have sufficient sensitivity and common-mode range to support LVDS signals.
TXD1+ TXD1- TXD2+ TXD2-	Diff. LVDS Output	H14 H13 K14 K13	The transmit differential data (TXD1+/-, TXD2+/-) outputs present NRZ encoded data to a serial backplane. These outputs are open drain current sinks which interface directly with twisted-pair cabling or board interconnect. Edge rates are controlled to minimize radiated emissions. Both differential links carry identical traffic except the exact phase relationship is not guaranteed.
REFCLK	Input	P12	The reference clock input (REFCLK) must provide a jitter-free reference clock. It is used as the reference clock by both clock recovery and clock synthesis circuits. Any jitter below 1 MHz is transferred directly to the TXD1+/- and TXD2+/- outputs. The high-speed serial interface bit rate is eight times the REFCLK frequency.
RES RESK	Analog	G12 H11	A 4.75kΩ ±1% resistor must be connected between these two pins to achieve the correct LVDS output signal levels.
ATP0 ATP1	Analog	L14 L13	The Analog Test Points (ATP) are provided for production test purposes. In mission mode they are high impedance and should be connected to ground.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
TX8K	Input	B14	The transmit 8 kHz timing reference (TX8K) input allows a traceable signal to be transmitted to the far end of the high-speed serial links via TXD1+/- and TXD2+/-. A rising edge on TX8K is encoded in the next cell transmitted. Although TX8K is targeted at a typical need of transporting an 8 kHz signal, its frequency is not constrained to 8 kHz. Any frequency less than the cell rate is permissible.
RX8K	Output	E13	The receive 8 kHz timing reference (RX8K) output presents the timing extracted from one of the receive high-speed serial links, RXD1+/- or RXD2+/-. The rising edge of RX8K is accurate to the nearest byte boundary of the high-speed serial link; therefore, a small amount of jitter is present. At a link rate of 155.52 Mb/s, the jitter is 63ns peak-to-peak. Pulses on RX8K are always 16 high-speed serial link bit periods wide (two REFCLK periods).
RCLK	Output	E11	The Recovered Clock (RCLK) output presents the byte clock for the active receive high-speed serial link. The RCLK frequency shall be 0.125 of the RXD1+/- or RXD2+/- bit rate. Due to the digital clock recovery technique employed, jitter is introduced as 12.8 ns phase steps. If the active link is changed, RCLK can not be guaranteed to be glitch free. Because of these two factors, RCLK must be cleaned up by a PLL before it is suitable for use as a timing reference.
Clocked Data Serial Interface			

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
SCIANY	Input	C7	The SCI-PHY/Any-PHY Interface (SCIANY) input selects the type of PHY device interface. If SCIANY is a logic high, the S/UNI-DUPLEX will be configured to communicate to the PHY devices via a shared SCI-PHY Level 2, Utopia L2, or Any-PHY cell bus. If SCIANY is a logic low, each PHY device has a dedicated clocked bit serial interface. The two types of interfaces share common package pins. Failure to present the correct logic level on this signal for the application may result in damage to the S/UNI-DUPLEX or the PHY devices. When SCIANY is logic high, LTXD[3] and LTXD[0] become inputs and need to be tied to VDD or VSS through a pull up or a pull down.
LRXD[15] LRXD[14] LRXD[13] LRXD[12] LRXD[11] LRXD[10] LRXD[9] LRXD[8] LRXD[7] LRXD[6] LRXD[5] LRXD[4] LRXD[3] LRXD[2] LRXD[1] LRXD[0]	Input (SCIANY= 0)	D6 A4 B4 D2 E3 J2 K3 L2 P2 M4 N6 L6 L7 P9 M9 L10	The low-speed receive data (LRXD[15:0]) inputs provide data from individual modem channels. The data streams must carry contiguous ATM cells with valid HCS (Header Check Sequence) bytes. LRXD[n] can be clocked either by the rising or falling edge of the corresponding LRXC[n] input, depending on the value of the LRXCINV bit of the Master Configuration register. By default, the rising edge is used. These inputs are only active if the SCIANY input is a logic low.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
LRXC[15] LRXC[14] LRXC[13] LRXC[12] LRXC[11] LRXC[10] LRXC[9] LRXC[8] LRXC[7] LRXC[6] LRXC[5] LRXC[4] LRXC[3] LRXC[2] LRXC[1] LRXC[0]	Input (SCIANY = 0)	A5 C4 A3 D3 E4 J4 K2 M1 N4 L5 N5 N7 P8 N8 N9 P11	The low-speed receive clock (LRXC[15:0]) inputs provide timing for the receive links. Each LRXC signal is independent of the others. Each signal in LRXD[15:0] is sampled either on the rising or the falling edge of the corresponding LRXC[15:0] clock, depending the value of the LRXCINV bit of the Master Configuration register. By default, the rising edge is used. The active edge on each LRXC must only occur during those bit periods containing ATM cell data. It must be suppressed during bit periods containing transmission overhead. These inputs are only active if the SCIANY input is a logic low. Maximum clock rate is 50 MHz.
LTXD[15] LTXD[14] LTXD[13] LTXD[12] LTXD[11] LTXD[10] LTXD[9] LTXD[8] LTXD[7] LTXD[6] LTXD[5] LTXD[4] LTXD[3] LTXD[2] LTXD[1] LTXD[0]	Output	A6 C6 B2 C2 D1 F2 G1 G4 G3 H2 J1 P4 N1 M5 M11 N12	The low-speed transmit data signals (LTXD[15:0]) carry the outgoing link data in bit serial format. Each LTXD signal is independent of the other signals. The most significant bit of each data byte is transmitted first. Each signal in LTXD[15:0] can be updated either on the rising or falling edge of the corresponding LTXC[15:0] clock, depending the value of the LTXCINV bit of the Master Configuration register. By default, the rising edge is used. These outputs are only active if the SCIANY input is a logic low. When SCIANY is logic high, LTXD[3] and LTXD[0] become inputs and need to be tied to VDD or VSS through a pull up or a pull down.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
LTXC[15] LTXC[14] LTXC[13] LTXC[12] LTXC[11] LTXC[10] LTXC[9] LTXC[8] LTXC[7] LTXC[6] LTXC[5] LTXC[4] LTXC[3] LTXC[2] LTXC[1] LTXC[0]	Input (SCIANY = 0)	B6 D5 B1 C1 E1 F1 F4 H3 H1 H4 L3 M3 N2 P7 M10 N10	The low-speed transmit clock (LTXC[15:0]) inputs provide timing for the transmit links. Each LTXC signal is independent of the others. Each signal in LTXD[15:0] is updated either on the rising or the falling edge of the corresponding LTXC[15:0] clock, depending on the value of the LTXCINV bit of the Master Configuration register. By default, the rising edge is used. As an option, clock gaps can be recognized to force byte alignment to the transmission overhead. These outputs are only active if the SCIANY input is a logic low. Maximum clock rate is 50 MHz.
Input Parallel Bus – (SCIANY is logic high)			
IANYPHY	Input	J1	The Input Port Any-PHY configuration (IANYPHY) input determines the protocol of the SCI-PHY/Any-PHY input port interface. IANYPHY is only active if the SCIANY input is a logic high. If IANYPHY is logic low, the interface complies to the SCI-PHY/Utopia specification. If IANYPHY is logic high, the interface complies to the Any-PHY specification. The Any-PHY protocol is supported only when the input port cell interface is configured as a bus slave (IMASTER input must be set to logic 0 if IANYPHY is high). IANYPHY is an asynchronous input and is expected to be held static.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
IMASTER	Input	A6	The input port master select (IMASTER) pin determines the direction of the input port cell interface control signals. If IMASTER is low, the input port of the S/UNI-DUPLEX is a bus slave and complies with the SCI-PHY/Utopia or Any-PHY transmit protocol depending of the state of the IANYPHY input. The IADDR[4:0], IAVALID, IENB signals are inputs. The ICA signal is an output. If IMASTER is high, the input port of the S/UNI-DUPLEX is a bus master and complies with the SCI-PHY/Utopia receive protocol (IANYPHY must be set to low if IMASTER is high). The IADDR[4:0], IAVALID, IENB signals are outputs. The ICA signal is an input. This input is only active if the SCIANY input is a logic high.
IBUS8	Input	C6	The input port bus width select (IBUS8) selects the interface bus width. When IBUS8 is high, only IDAT[7:0] are expected to present valid data and IDAT[15:8] are ignored. When IBUS8 is low, all IDAT[15:0] inputs are used. This input is only active if the SCIANY input is a logic high.
IFCLK	Input	F4	The input FIFO clock (IFCLK) is used to read words into the S/UNI-DUPLEX upstream cell buffer. IFCLK must cycle at a 52 MHz or lower instantaneous rate. All SCI-PHY/Any-PHY input port timing is relative to the rising edge of IFCLK. This input is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
ISOC	Input	H2	This input is only active in SCI-PHY/Utopia bus slave or bus master modes (SCIANY = 1, ANYPHY= 0). The Input Start of Cell (ISOC) marks the start of the cell on the IDAT[15:0] bus. When ISOC is high, the first word of the cell structure is present on the IDAT[15:0] stream. It is not necessary for ISOC to be asserted for each cell, unless inband addressing is being used. An interrupt may be generated if ISOC is high during any word other than the first word of the cell structure. ISOC is sampled on the rising edge of IFCLK. If IMASTER is high, ISOC is considered valid only when the IENB signal was low in the previous cycle. If IMASTER is low, ISOC is considered valid coincident with IENB assertion.
ISX	Input	H4	The Transmit Start Of Cell (ISX) indication signal is only active in Any-PHY bus slave mode (when IANYPHY=1 and IMASTER=0). ISX marks the start of cell on the IDAT[15:0] data bus. When ISX is high, the first word of the cell structure is present on the IDAT[15:0] stream. ISX must be asserted for each cell. An interrupt may be generated if ISX is high during any word other than the expected first word of the cell structure. This input is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
IDAT[15] IDAT[14] IDAT[13] IDAT[12] IDAT[11] IDAT[10] IDAT[9] IDAT[8] IDAT[7] IDAT[6] IDAT[5] IDAT[4] IDAT[3] IDAT[2] IDAT[1] IDAT[0]	Input (SCIANY = 1)	B1 C2 C1 D2 D3 D1 E1 E3 E4 F2 F1 G1 G4 H3 G3 H1	The Input Data bus (IDAT[15:0]) carries the ATM cell words that are written to the upstream cell buffer. Only IDAT[7:0] are used if the IBUS8 input is high. IDAT[15:0] is sampled on the rising edge of IFCLK. As a SCI-PHY/Utopia bus master (IMASTER=1, IANYPHY=0) the IDAT[15:0] bus is considered valid only when the IENB signal was low in the previous cycle. As a bus slave (IMASTER = 0) the IDAT[15:0] bus is considered valid when the IENB signal is asserted low or the ISX signal is asserted high. As an Any-PHY bus slave (IMASTER = 0, IANYPHY=1) IDAT[15:0] bus is not considered valid when autonomous deselection occurs after the last word of a cell. These inputs are only active if the SCIANY input is a logic high.
IPRTY	Input	B2	The Input Parity (IPRTY) signal completes the parity (programmable for odd or even parity) of the IDAT[15:0] bus when IBUS8 is low and the IDAT[7:0] bus when IBUS8 is high. A maskable interrupt and a status bit are generated upon a parity error; no other actions are taken. The IPRTY signal is sampled on the rising edge of IFCLK. As a SCI-PHY/Utopia bus master (IMASTER=1, IANYPHY=0) IPRTY is considered valid only when the IENB signal was low in the previous cycle. As a bus slave (IMASTER=0) IPRTY is considered valid coincident with IENB being asserted low or ISX being asserted high. As an Any-PHY bus slave (IMASTER = 0, IANYPHY = 1) IPRTY is not considered valid when autonomous deselection occurs after the last word of a cell. This input is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
ICA	I/O	A3	The Input Cell Available (ICA) signal provides cell-level flow control. ICA's direction depends on the state of the IMASTER input. As a SCI-PHY/Utopia bus master (IMASTER = 1, IANYPHY = 0) the S/UNI-DUPLEX polls up to 32 PHYs using the PHY address signals IADDR[4:0]. A PHY device being addressed by IADDR[4:0] is expected to indicate whether or not it has a complete cell available for transfer by driving ICA during the clock cycle following that in which it is addressed. When a cell transfer is in progress, the S/UNI-DUPLEX will not poll the PHY device which is sending the cell so PHY devices need not support the cell availability indication during cell transfer. The selection of a particular PHY device from which to transfer a cell is indicated by the state of IADDR[4:0] during the last cycle IENB is high. As a bus slave (IMASTER = 0) the S/UNI-DUPLEX indicates the ability to accept additional cells via the ICA output. When IAVALID is sampled high in SCI-PHY or low in Any-PHY configuration, ICA is asserted if the cell FIFO for the logical channel addressed by IADDR[4:0] has at least one empty cell buffer. If the FIFO is full, ICA is deasserted. If a cell transfer is in progress that will fill a logical channel FIFO, ICA will also be deasserted. When IAVALID is sampled low in SCI-PHY or high in Any-PHY configuration, ICA becomes high impedance. ICA is delayed by an additional clock cycle in Any-PHY configuration. The buffer status for the particular logical channel involved is stale for a maximum of 16 cycles after the start of the cell transfer when using a 8 bit bus or 12 cycles when using a 16 bit bus. Therefore, the master should refrain from polling that logical channel in the interim.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
ICA (Cont'd)			As a bus slave (IMASTER = 0) the S/UNI-DUPLEX can also be configured to respond to a subset of the IADDRESS[4:0] address range. In this case, ICA will remain high-impedance when the logical channel addressed by IADDR[4:0] is outside the address range specified by ICAEN[31:0] of the Input Cell Available Enable registers. ICA is sampled or updated on the rising edge of IFCLK. This signal is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
IENB	I/O	B4	The active low input port enable (IENB) signal is used to initiate the reading of cells from a PHY device into the upstream cell buffer. As a SCI-PHY/Utopia bus master (IMASTER = 1, IANYPHY = 0) the S/UNI-DUPLEX asserts IENB to transfer a cell from one of up to 32 PHY devices. The source PHY is selected by the IADDR[4:0] signals. A valid word is expected on the IDAT[15:0] bus at the second rising edge of IFCLK after the enable is asserted. As a bus slave (IMASTER = 0) IENB is an input and a IDAT[15:0] word is accepted coincident with IENB being sampled low. As an Any-PHY bus slave (IMASTER = 0, IANYPHY = 1) IENB is ignored if ISX is high and may be held low upon the completion of a cell transfer, since a cell transfer is only initiated by assertion of ISX. IENB may be deasserted high at any time to pause a cell transfer.IENB is sampled or updated on the rising edge of IFCLK. The Any-PHY protocol supports autonomous deselection. As an Any-PHY slave the inputs become high impedance after the last word of a cell is transferred until the S/UNI-DUPLEX is reselected (via ISX) even if IENB is left asserted. As a SCI-PHY/Utopia slave ISX is not defined, so a subsequent cell is transferred (provided one is available) if IENB is held low beyond the end of a cell. This signal is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
IADDR[4] IADDR[3] IADDR[2] IADDR[1] IADDR[0]	I/O	D6 A5 D5 A4 C4	As a SCI-PHY/Utopia bus master (IMASTER = 1, IANYPHY = 0) the IADDR[4:0] signals are outputs used to address up to 32 PHY devices for the purposes of polling and selection for cell transfer. When conducting polling, in order to avoid bus contention, the S/UNI-DUPLEX inserts gap cycles during which IADDR[4:0] is set to 0x1F and IAVALID is logic 0. When this occurs, no PHY device should drive ICA during the following clock cycle. Polling is performed in incrementing sequential order. The PHY device selected for transfer is based on the IADDR[4:0] value present during the last cycle IENB was high. As a SCI-PHY/Utopia bus slave (IMASTER = 0, IANYPHY = 0) IADDR[4:0] are inputs. During polling when IAVALID is sampled high in SCI-PHY or low in Any-PHY configuration, the S/UNI-DUPLEX will drive ICA with the cell buffer availability status of the logical channel indexed by IADDR[4:0] on the next IFCLK cycle. The logical channel selected for a cell transfer is determined by the IADDR[4:0] value presented when IENB was last sampled high. Cell transfer is initiated with the ISOC input being asserted. As an Any-PHY bus slave (IMASTER = 0, IANYPHY = 1) IADDR[4:0] are inputs used only for polling. Cell transfer is initiated with inband addressing (prepend Word 0 contains the address) and the ISX input. Polling occurs when IAVALID is sampled low and the S/UNI-DUPLEX drives ICA with the cell buffer availability status of the logical channel indexed by IADDR[4:0]. There is a one IFCLK cycle gap between IAVALID sampled low and ICA.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
IADDR[4] IADDR[3] IADDR[2] IADDR[1] IADDR[0] (Cont'd)			As a bus slave device (either SCI-PHY or Any-PHY), the S/UNI-DUPLEX can be configured to be restricted to a subset of the logical channel address range. In this case, device polling or selection will occur when the logical channel addressed by IADDR[4:0] is inside the address range specified by ICAEN[31:0] of the Input Cell Available Enable registers. The IADDR[4:0] bus is updated or sampled on the rising edge of IFCLK. These signals are only active if the SCIANY input is a logic high.
IAVALID	I/O	B6	The Input Port Address Valid (IAVALID) pin indicates that the IADDR[4:0] bus is asserting a valid PHY address for polling purposes. As a SCI-PHY/Utopia bus master (IMASTER = 1, IANYPHY = 0) IAVALIV is an output. When IAVALID is deasserted, the IADDR[4:0] bus is set to 0x1F as defined by the Utopia L2 bus standard. therefore use of IAVALID is not necessary when less than 32 PHY devices are being polled. As a bus slave (IMASTER = 0) IAVALID is an input used to control the ICA output. IAVALID is active highin SCI-PHY/Utopia mode (IANYPHY = 0) and active low in Any-PHY mode (IANYPHY = 1). The ICA output is only driven when IAVALID is sampled active. If IAVALID is sampled inactive, ICA becomes high impedance. The S/UNI-DUPLEX supports polling in contiguous cycles if IAVALID is held active. ICA is delayed by an additional IFCLK cycle.IAVALID is sampled or updated on the rising edge of IFCLK. This signal is only active if the SCIANY input is a logic high.
Parallel Bus - Output			

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
OANYPHY	Input	M5	The Output Port Any-PHY configuration (OANYPHY) input determines the protocol of the SCI-PHY/Any-PHY output port interface. OANYPHY is only active if the SCIANY input is a logic high. If OANYPHY is logic low, the interface complies to the SCI-PHY/Utopia specification. If OANYPHY is logic high, the interface complies to the Any-PHY specification. The Any-PHY protocol is supported only when the output port cell interface is configured as a bus slave (IMASTER input must be set to logic low if OANYPHY is high). OANYPHY is an asynchronous input and is expected to be held static.
OMASTER	Input	M11	The Output Port Master select (OMASTER) pin determines the direction of the output port cell interface control signals. If OMASTER is high the OANYPHY must be low. The output port of the S/UNI-DUPLEX is a bus master that complies with the SCI-PHY/Utopia transmit protocol. The OADDR[4:0], OAVALID, OENB signals are outputs and the OCA signal is an input. If OMASTER is low, the output port of the S/UNI-DUPLEX is a bus slave and complies with the SCI-PHY/Utopia or the Any-PHY receive protocol depending on the state of the OANYPHY input. The OADDR[4:0], OAVALID, OENB signals are inputs. The OCA signal is an output. This input is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
OBUS8	Input	P4	The output port bus width select (OBUS8) selects the output port interface bus width. When OBUS8 is high, only ODAT[7:0] present valid data and ODAT[15:8] are held low. When OBUS8 is low, all ODAT[15:0] outputs are used. This input is only active if the SCIANY input is a logic high.
OFCLK	Input	N5	The output port FIFO clock (OFCLK) is used to transfer cells from the internal downstream cell buffer to the PHY devices. OFCLK must cycle at a 52 MHz or lower instantaneous rate, but a high enough rate to avoid a FIFO overflow. All SCI-PHY/Any-PHY output port timing is relative to the rising edge of OFCLK. This input is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
OSOC	Output	L7	In all bus modes, OSOC is updated on the rising edge of OFCLK. When not presenting valid data, OSOC is high impedance. In SCI-PHY/Utopia bus slave mode (OMASTER = 0, OANYPHY = 0) the output port start of cell (OSOC) indication signal marks the first word of the cell transfer on the ODAT[15:0] data bus. OSOC is driven immediately upon sampling OENB low if the previous polling cycle resulted in this device being selected (see the OCA description below). In Any-PHY bus slave mode (OMASTER = 0, OANYPHY = 1) the output port start of cell (OSOC) indication signal marks the second word of the cell transfer on the ODAT[15:0] data bus. OSOC is driven after one OFCLK cycle delay upon sampling OENB low if the previous polling cycle resulted in this device being selected (see the OCA description below). Autonomous deselection occurs after the last word of a cell resulting in setting OSOC high-impedance until reselection. In SCI-PHY/Utopia bus master mode (OMASTER = 1, OANYPHY = 0) the output port start of cell (OSOC) indication signal marks the first word of the cell transfer on the ODAT[15:0] data bus. OSOC is valid coincident with OENB assertion.. When OANYPHY is high, autonomous deselection occurs after the last word of a cell resulting in setting OSOC high-impedance until reselection. This output is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
OSX	Output	P8	The Output Start of Transfer (OSX) is only active in Any-PHY bus slave mode (OANYPHY = 1 OMASTER = 0). When OANYPHY is logic low, OSX is held low during cell transfer or high-impedance otherwise. OSX marks the start of the cell on the ODAT[15:0] bus. When OSX is high, the first word of the cell structure is present on the ODAT[15:0] stream. OSX is updated on the rising edge of OFCLK and considered valid only when the OENB signal was sampled low in the previous cycle and the S/UNI-VORTEX device was selected after the polling process. OSX becomes high impedance (with a cycle latency) upon sampling OENB high or if the S/UNI-VORTEX device is not selected for transfer. When OANYPHY is high, autonomous deselection occurs after the last word of a cell resulting in setting OSX high-impedance until reselection. This input is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
ODAT[15] ODAT[14] ODAT[13] ODAT[12] ODAT[11] ODAT[10] ODAT[9] ODAT[8] ODAT[7] ODAT[6] ODAT[5] ODAT[4] ODAT[3] ODAT[2] ODAT[1] ODAT[0]	Output (SCIANY = 1)	J4 K3 K2 L3 L2 M1 M3 N2 P2 N4 M4 L5 N6 L6 N7 P7	The output port cell data bus (ODAT[15:0]) carries the ATM cell octets that are transferred to the PHY devices. Only ODAT[7:0] are used if OBUS8 is high. The ODAT[15:0] bus is updated on the rising edge of OFCLK. As a SCI-PHY/Utopia bus master (OMASTER = 1, OANYPHY = 0), the ODAT[15:0] bus is considered valid coincident with OENB assertion. As a bus slave (OMASTER = 0), the ODAT[15:0] bus is considered valid only when the S/UNI-VORTEX device was selected after the polling process and the OENB signal is sampled low. As an SCI-PHY/Utopia bus slave (OMASTER = 0, OANYPHY = 0) ODAT[15:0] is driven immediately upon sampling OENB low it has an additional OFCLK cycle latency. When not presenting valid data, the ODAT[15:0] bus is high impedance. Autonomous deselection occurs after the last word of a cell resulting in setting ODAT[15:0] high-impedance until reselection. These outputs are only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
OPRTY	Output	J2	The output port parity (OPRTY) signal completes the parity (programmable for odd or even parity) of the ODAT[15:0] bus when OBUS8 is low and the ODAT[7:0] bus when OBUS8 is high. The OPRTY signal is updated on the rising edge of OFCLK. As a SCI-PHY/Utopia bus master (OMASTER = 1, OANYPHY = 0) OPRTY is considered valid coincident with OENB assertion. As a bus slave (OMASTER = 0) the OPRTY bus is considered valid only when the S/UNI-VORTEX device was selected after the polling process and the OENB signal is sampled low. As an SCI-PHY/Utopia bus slave (OMASTER = 0, OANYPHY = 0) OPRTY is driven immediately upon sampling OENB low, but as an Any-PHY bus slave (OMASTER = 0, OANYPHY = 1) it has an additional cycle latency when OANYPHY is logic high. When not presenting valid data, OPRTY is high impedance. As an Any-PHY bus slave autonomous deselection occurs after the last word of a cell resulting in setting OPRTY high-impedance until reselection. This output is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
OCA	I/O	N8	The Output Cell Available (OCA) signal provides cell-level flow control. OCA's direction depends on the state of the OMASTER input. As a SCI-PHY/Utopia bus master (OMASTER = 1, OANYPHY = 0) the S/UNI-DUPLEX polls up to 32 PHYs using the PHY address signals OADDR[4:0]. A PHY device being addressed by OADDR[4:0] is expected to indicate whether or not it can accept a cell by driving the OCA during the clock cycle following that in which it is addressed. When a cell transfer is in progress, the S/UNI-DUPLEX will not poll the PHY device which is receiving the cell so PHY devices need not support the cell availability indication during cell transfer. The selection of a particular PHY device to which a cell will be written is indicated by the state of OADDR[4:0] during the last cycle OENB was high. As a bus slave (OMASTER = 0) the S/UNI-DUPLEX indicates the existence of at least one complete cell within its buffers when polled. The S/UNI-DUPLEX round-robins between the logical channel cell FIFOs to autonomously select cells, so the interface appears as a single PHY slave. When OAVALID is sampled high in SCI-PHY or low in Any-PHY configuration and the sampled OADDR[4:0] matches the OAD[4:0] bits in the Output Address Match register, OCA is asserted if at least one cell is available for transfer. If all logical channel FIFOs are empty, OCA is deasserted. If a cell transfer is in progress that will read the last available cell, OCA will also be deasserted. When OAVALID is sampled low, OCA becomes high impedance. OCA is delayed by an additional clock cycle in Any-PHY configuration. OCA is sampled or updated on the rising edge of OFCLK. This signal is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
			High Speed LVDS Links
OENB	I/O	P9	The active low output port enable (OENB) signal is used to enact cell transfers from the output port. OENB's direction depends on the state of the OMASTER input. As a SCI-PHY/Utopia bus master (OMASTER = 1, OANYPHY = 0) OENB is an output and a valid word is output on the ODAT[15:0] bus coincidentally with the assertion of OENB. The state of OADDR[4:0] during the last cycle OENB was high selects the PHY to which the cell is destined. Once asserted low, OENB will remain low until the cell transfer is complete. As a bus slave (OMASTER = 0) OENB is an input. When OENB is sampled low and the S/UNI-DUPLEX has been selected, a word is output on bus ODAT[15:0]. Selection occurs when OENB is last sampled high if the OADDR[4:0] value equals the state of the OAD[4:0] bits in the Output Address Match register and OAVALID is sampled is its asserted state. OENB must be low for the duration of the cell transfer. As a SCI-PHY/Utopia slave valid data is driven immediately upon sampling OENB low. As a Any-PHY slave the OSX, OSOP, ODAT[15:0] and OPRTY outputs have an additional cycle of latency. It is permissible to pause a cell transfer by deasserting OENB high. As a SCI-PHY/Utopia slave the S/UNI-DUPLEX's must be reselected before the cell transfer can resume. As a Any-PHY slave the cell transfer resumes unconditionally when OENB is asserted low again. In either case, a cell transfer must be completed before another device on the bus is selected. The Any-PHY protocol supports autonomous deselection. As an Any-PHY slave the outputs become high impedance after the last word of a cell is transferred until the S/UNI-DUPLEX is reselected (via OSX) even if OENB is left asserted. As a SCI-PHY/Utopia slave OSX is not defined, so a subsequent cell is transferred (provided one is available) if OENB is held low beyond the end of a cell.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
OENB	I/O		(Continued) When OENB is sampled high or the S/UNI-DUPLEX is not selected, no read is performed and outputs ODAT[15:0], OPRTY, OSX and OSOC become high impedance. OENB is sampled or updated on the rising edge of OFCLK. This signal is only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
OADDR[4] OADDR[3] OADDR[2] OADDR[1] OADDR[0]	I/O	N9 M10 N10 L10 P11	As a SCI-PHY/Utopia bus master (OMASTER = 1, 0ANYPHY = 0) the OADDR[4:0] signals are used to address up to 32 PHY devices for the purposes of polling and selection for cell transfer. When conducting polling, in order to avoid bus contention, the S/UNI-DUPLEX inserts gap cycles during which the OADDR[4:0] bus is set to 0x1F and OAVALID is logic 0. When this occurs, no PHY device should drive OCA during the following clock cycle. The polling order is based on the existence of cells in the downstream cell buffer. The PHY device selected for transfer is based on the OADDR[4:0] value present during the last cycle OENB is high. As a bus slave the OADDR[4:0] signals are inputs. When OAVALID is sampled high in SCI-PHY/Utopia or low in Any-PHY configuration and the sampled OADDR[4:0] matches the OAD[4:0] bits in the Output Address Match register, OCA is asserted if at least one cell is available for transfer. OCA is delayed by an additional OFCLK cycle in Any-PHY configuration. If the OADDR[4:0] value equals the state of the OAD[4:0] bits in the Output Address Match register when the OENB is last sampled high, the S/UNI-DUPLEX will initiate a cell transfer. As a SCI-PHY/Utopia bus slave (OMASTER = 0, OANYPHY = 0) the device must be reselected to resume a cell transferred that has been halted by deasserting OENB high. The OADDR[4:0] bus is sampled or updated on the rising edge of OFCLK. These signals are only active if the SCIANY input is a logic high.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
OAVALID	I/O	M9	The Output Address Valid (OAVALID) pin indicates that the OADDR[4:0] bus is asserting a valid PHY address for polling purposes. As a SCI-PHY/Utopia bus master (OMASTER = 1, OANYPHY = 0) OAVALID is an output. When this signal is deasserted, the OADDR[4:0] bus is also set to 0x1Fas defined by the Utopia L2 bus standard. Therefore. Use of OAVALID is not necessary when less than 32 PHY devices are being polled. As a bus slave (OMASTER = 0) OAVALID is an input used to control the OCA output. The OCA output is only driven when OAVALID is asserted (sampled high in SCI-PHY/Utopia or sample low in Any-PHY configuration) and the sampled OADDR[4:0] value matches the OAD[4:0] bits in the Output Address Match register. If OAVALID is deasserted (sampled low in SCI-PHY/Utopia) or high in Any-PHY configuration) OCA becomes high impedance. The S/UNI-DUPLEX supports polling in contiguous cycles if OAVALID is held high. OCA is delayed by an additional OFCLK cycle in Any-PHY bus configuration. OAVALID is sampled or updated on the rising edge of OFCLK. This signal is only active if the SCIANY input is a logic high.
Microprocessor Bus			
CSB	Input	D8	The active-low chip select (CSB) signal is low during S/UNI-DUPLEX register accesses. Note that when not being used, CSB must be tied high. If CSB is not required (i.e., registers accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
RDB	Input	A8	The active-low read enable (RDB) signal is low during S/UNI-DUPLEX register read accesses. The S/UNI-DUPLEX drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	D9	The active-low write strobe (WRB) signal is low during S/UNI-DUPLEX register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	C14 D13 D12 D14 F11 F13 F12 F14	The bi-directional data bus D[7:0] is used during S/UNI-DUPLEX register read and write accesses.
A[7]/TRS A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	C9 A9 B9 B10 D11 A11 C11 B11	The address bus A[7:0] selects specific registers during S/UNI-DUPLEX register accesses. The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.
RSTB	Input	A10	The active-low reset (RSTB) signal provides an asynchronous S/UNI-DUPLEX reset. RSTB is a Schmitt triggered input with an integral pull-up resistor.
ALE	Input	B8	The address latch enable (ALE) is active-high and latches the address bus A[5:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-DUPLEX to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
INTB	OD Output	B7	The active-low interrupt (INTB) signal goes low when a S/UNI-DUPLEX interrupt source is active and that source is unmasked. The S/UNI-DUPLEX may be enabled to report many alarms or events via interrupts. INTB is tristated when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
RSTOB	OD Output	A2	The active low Reset Output pin may be used to reset other devices. RSTOB is asserted low when RSTB is low, the RESETO bit of the Master Configuration register is set or if a “remote reset activate” bit oriented code has been validated for the active link. The “remote reset deactivate” code sets RSTOB to high impedance unless the RESETO bit is set.
JTAG Boundary Scan Port			
TCK	Input	B13	The test clock (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	B12	The test mode select (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	A12	The test data input (TDI) signal carries test data into the S/UNI-DUPLEX via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tristate	P13	The test data output (TDO) signal carries test data out of the S/UNI-DUPLEX via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is inactive except when scanning of data is in progress.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
TRSTB	Input	A13	The active-low test reset (TRSTB) signal provides an asynchronous S/UNI-DUPLEX test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when not being used, TRSTB must be connected to the RSTB input.
Power and Ground			
BIAS	Power	A7	When tied to +5V, the BIAS input is used to bias the wells in the input and I/O pads so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When tied to +3.3V, the inputs and bi-directional inputs will only tolerate 3.3V level inputs.
VDD	Power	B3 C5 C13 D10 E2 E14 F3 K1 L1 L4 L9 M7 M12 N3 N13 P6	The digital power (VDD) pins should be connected to a well-decoupled +3.3 V DC supply.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
VSS	Ground	B5 C3 C8 C10 C12 D4 D7 E12 G2 J3 K4 L8 M2 M6 M8 N11 N14 P3 P5 P10	The digital ground (VSS) pins should be connected to GND.
QAVD	Analog Power	M13	Quiet Analog Power (QAVD). QAVD should be connected to analog +3.3 V. It should be electrically isolated (as much as possible) from the other power connections.
QAVS	Analog Ground	M14	Quiet Analog Ground (QAVS). QAVS should be connected to analog GND. It should be electrically isolated (as much as possible) from the other ground connections.
CAVD	Analog Power	L11	The power (CAVD) pin for the analog clock synthesis unit. This pin should be connected to analog +3.3V. It should be electrically isolated (as much as possible) from the other power connections.
CAVS	Analog Ground	L12	The ground (CAVS) pin for the analog clock synthesis unit. This pin should be connected to analog GND. It should be electrically isolated (as much as possible) from the other ground connections.

Ball Name	Type	Ball No.	Function
High Speed LVDS Links			
RAVD	Analog Power	J11	The power (RAVD) pin for the LVDS receivers. This pin should be connected to analog +3.3V. It should be electrically isolated (as much as possible) from the other power connections.
RAVS	Analog Ground	J12	The ground (RAVS) pin for the LVDS receivers. This pin should be connected to analog GND. It should be electrically isolated (as much as possible) from the other ground connections.
TAVD	Analog Power	G11 K11	The power (TAVD) pins for the LVDS transmitters. These pins should be connected to analog +3.3V. These should be electrically isolated (as much as possible) from the other power connections.
TAVS	Analog Ground	H12 K12	The ground (TAVS) pins for the LVDS transmitters. These pins should be connected to analog GND. These should be electrically isolated (as much as possible) from the other ground connections.
GND	Thermal Vias	G7 G8 H7 H8	The Thermal Vias (GND) are used to improve thermal conductance of the device package. They should be connected to the PCB ground plane. The GND pins are not electrically connected to the other ground pins of the package.

Notes on Pin Description:

1. All S/UNI-DUPLEX inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels, except RXD1+/- and RXD2+/-.

2. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.

3. The recommended power supply sequencing is as follows:

    1. 3.1 During power-up, the voltage on the BIAS pin must be kept equal to or greater than the voltage on the VDD pins, to avoid damage to the device.

    2. 3.2 The VDD power must be applied before input pins are driven or the input current per pin be limited to less than the maximum DC input current specification (20 mA).

3. 3.3 Analog power supplies (QAVD, CAVD, RAVD, TAVD) must be applied after VDD have been applied or they must be current limited to the maximum latch-up current specification (100 mA). In operation, the differential voltage measured between AVD supplies and VDD must be less than 0.5 V. The relative power sequencing of the multiple AVD power supplies is not important.

4. 3.4 Power down the device in the reverse sequence.

9 FUNCTIONAL DESCRIPTION

The S/UNI-DUPLEX supports two distinct methods of interconnection to modems, PHYs and other ATM devices: via a parallel bus interface or via 16 clocked serial data interface. In either case the primary function of the S/UNI-DUPLEX is to transfer cells between the external devices and the high speed LVDS serial links. At far end of the LVDS link another S/UNI-DUPLEX device or a S/UNI-VORTEX device must be connected. See the PMC-Sierra Data Sheet for the PM7351 S/UNI-VORTEX for details on that device.

In the LVDS transmit direction, cells are read from the external devices and multiplexed onto the LVDS link. Flow control, alarm, PHY identification, and other control information is added to each cell to ensure a managed link is maintained.

In the LVDS receive direction, system overhead is stripped off each cell before it is sent to the appropriate device on the parallel bus or over the clocked serial data interfaces. In bus slave mode, the PHY ID is left in the cell, typically for use by an ATM layer device such as PMC-Sierra's S/UNI-ATLAS so that the cell source can be determined. In bus master mode, or in clocked serial interface mode the PHY ID is stripped off and used to direct the cell to the appropriate Utopia slave device or to the appropriate clocked serial interface.

For a discussion of overall system architecture issues, the reader is referred to a companion document provided by PMC-Sierra titled *S/UNI-VORTEX & S/UNI-DUPLEX TECHNICAL OVERVIEW*. The document number is PMC-981025 and it can be obtained by one of the various means described on the last page of this document.

The remainder of this section focuses on the interfaces and functionality of a single S/UNI-DUPLEX device, although the reader should also view things in the context of the attached far-end device (either a S/UNI-DUPLEX or a S/UNI-VORTEX).

9.1 Parallel Bus Interface

The S/UNI-DUPLEX's parallel interface. is selected when the SCIANY input is tied high. This interface supports three types of bus: Utopia Level 2, SCI-PHY Level 2, and Any-PHY.

Table 1 provides the correspondence between the S/UNI-DUPLEX pin names and the Utopia Level 2, SCI-PHY Level 2 and Any-PHY signals. The Any-PHY bus format is enabled when the IANYPHY and OANYPHY inputs are tied high, SCI-PHY or Utopia is selected when the inputs are tied low. Input and output

bus formats need not be the same. When configured as a SCI-PHY or Utopia Level 2 interface the S/UNI-DUPLEX can be either a bus master or bus slave, as determined by the IMASTER and OMASTER inputs. When configured as an Any-PHY interface, the S/UNI-DUPLEX can only be a bus slave. 8 and 16 bit wide interfaces are supported in all configurations, and are determined by the IBUS8 and OBUS8 inputs.

Table 1 Signal Name Cross-Reference

S/UNI-DUPLEX PIN Name	UTOPIA Level 2 Bus Slave	UTOPIA Level 2 Bus Master	SCI-PHY Level 2 Bus Slave	SCI-PHY Level 2 Bus Master	Any-PHY Bus Slave
IFCLK	TxClk	RxClk	TFCLK	RFCLK	TCLK
IENB	TxEnb*	RxEnb*	TWRENB	RWRENB	TENB
IADDR[4:0]	TxAddr[4:0]	RxAddr[4:0]	TADDR[4:0]	RADDR[4:0]	TADR[4:0]
IAVALID	n/a	n/a	TAVALID	RAVALID	TADR[5]
IDAT[15:0]	TxData[15:0]	RxData[15:0]	TDAT[15:0]	RDAT[15:0]	TDAT[15:0]
IPRTY	TxPrty	RxPrty	TPRTY	RPRTY	TPRTY
ICA	TxClav	RxClav	TCA	RCA	TPA
ISOC	TxSOC	RxSOC	TSOC	RSOC	TSOP
ISX	n/a	n/a	n/a	n/a	TSX
OFCLK	RxClk	TxClk	RFCLK	TFCLK	RCLK
OENB	RxEnb*	TxEnb*	RWRENB	TWRENB	RENB
OADDR[4:0]	RxAddr[4:0]	TxAddr[4:0]	RADDR[4:0]	TADDR[4:0]	RADR[4:0]
OAVALID	n/a	n/a	RAVALID	TAVALID	RADR[5]
ODAT[15:0]	RxData[15:0]	TxData[15:0]	RDAT[15:0]	TDAT[15:0]	RDAT[15:0]
OPRTY	RxPrty	TxPrty	RPRTY	TPRTY	RPRTY
OCA	RxClav	TxClav	RCA	TCA	RPA
OSOC	RxSOC	TxSOC	RSOC	TSOC	RSOP
OSX	n/a	n/a	n/a	n/a	RSX

Utopia and SCI-PHY are electrically compatible, the only difference is that Utopia does not support the use of the optional OAVALID and IAVALID pins. Therefore, whether the input and output buses are Utopia or SCI-PHY is determined by the inclusion or exclusion of optional words in the cell format that is transferred across the bus. The cell formats supported are presented in Fig. 6 and Fig. 7. As programmed through register bits, bytes may be prepended to a basic ATM cell to support applications where user defined context information is carried inband. Also, inclusion of the H5 and H5/UDF fields (8 bit and 16 bit modes respectively) is optional under most configurations. For bus slave configurations, the PHY

identifier and an inband address can be included in an additional prepend word or in the H5/UDF fields, as discussed below. By default, none of the optional words are prepended, and the H5 or H5/UDF field is included.

Be aware that cells are transported transparently across the LVDS links. There are no constraints on the contents. Therefore, data streams other than ATM cells can be transferred across the parallel bus interface interface; only the bus timing and bus protocols need be respected.

It is also important to note that the treatment of the H5/UDF field, the address prepend (Word 0), and the optional User Prepend on the input and output buses are independent from how their corresponding fields on the LVDS link are configured. See Section 12.2 for further details.

9.1.1 SCI-PHY or Utopia Bus Master

The SCI-PHY/Utopia bus master format is enabled when the IANYPHY and OANYPHY inputs are tied low and the IMASTER and OMASTER inputs are tied high. The SCI-PHY/Utopia bus master interface supports up to 32 PHY entities provided the IAVALID and OAVALID signals are used; otherwise, 31 are supported. The interface is fully Utopia Level 2 compliant when IAVALID and OAVALID are not used. It is assumed the PHY devices perform all Transmission Convergence (TC) functions including cell delineation, cell rate decoupling, payload scrambling, HCS insertion and cell filtering upon header errors.

In the ingress direction (cells are transferred from the input bus to the LVDS link), the S/UNI-DUPLEX uses round robin polling to provide equal access to all PHY devices. As directed by flow control information on the LVDS link (and optionally through S/UNI-DUPLEX configuration), any PHY device may temporarily be removed from the polling sequence. Data transfers are cell based, that is, an entire cell is transferred from one PHY device before another is selected. Polling occurs concurrently with cell transfers to ensure maximum throughput.

The SCI-PHY/Any-PHY Input Configuration 1 register (0x0C) determines the cell format of the input bus. Unlike the Any-PHY bus mode, a SCI-PHY/Utopia bus master does not require and hence does not support embedded PHY ID. The cell length options for the 8 bit bus (shown in Fig. 6) are described in Table 2. 16 bit bus options (shown in Fig. 7) are described in Table 3.

Table 2 Eight Bit SCI-PHY/Utopia Bus Master, Input Configuration

# bytes	Byte 0	1	2	7	Register 0x0C H5UDF	PRELEN	Notes
52	N	N	N	N	0	00	Short cell, no H5 byte
53	**N**	**N**	**N**	**Y**	**1**	**00**	**Default, Utopia compatible**
53	N	Y	N	N	0	01	1 user byte then H1-H4
54	N	Y	N	Y	1	01	1 user byte then H1-H5
54	N	Y	Y	N	0	10	2 user bytes then H1-H4.
55	N	Y	Y	Y	1	10	2 user bytes then H1-H5.

Table 3 Sixteen Bit SCI-PHY/Utopia Bus Master, Input Configuration

# bytes	Word 0	1	4	Register 0x0C H5UDF	PRELEN	Notes
52	N	N	N	0	00	Short cell, no H5/UDF field
54	**N**	**N**	**Y**	**1**	**00**	**Default, Utopia compatible**
54	N	Y	N	0	01	1 user word then H1-H4
56	N	Y	Y	1	01	1 user word, H1-H4, then H5/UDF

In the egress direction (cells are transferred from the LVDS link to the output bus.), only those PHY devices are polled for which there is a cell in the internal cell buffer. The cell buffer is organized as 32 FIFOs, each associated with a single PHY device. This arrangement prevents head-of-line blocking. As per the ingress interface, transfers are cell based and polling is concurrent with cell transfers.

The SCI-PHY/Any-PHY Output Configuration register (0x14) determines the cell format of the output bus. A SCI-PHY/Utopia bus master neither requires nor supports embedded PHY ID. The cell length options for the 8 bit bus (shown in Fig. 6) are described in Table 4. 16 bit bus options (shown in Fig. 7) are described in Table 5.

Table 4 Eight Bit SCI-PHY/Utopia Bus Master, Output Configuration

# bytes	Byte 0	1	2	7	Register 0x14 INADD UDF	H5 UDF	PRE LEN	Notes
52	N	N	N	N	X	0	00	Short cell, no PHY ID is generated
53	**N**	**N**	**N**	**Y**	**X**	**1**	**00**	**Default setting. Utopia compatible, standard 53 byte cell, no PHY ID**
53	N	Y	N	N	X	0	01	1 user byte, H1-H4, no PHY ID
54	N	Y	N	Y	X	1	01	1 user byte, H1-H5, no PHY ID
54	N	Y	Y	N	X	0	10	2 user bytes, H1-H4, no PHY ID
55	N	Y	Y	Y	X	1	10	2 user bytes, H1-H5, no PHY ID

Table 5 Sixteen Bit SCI-PHY/Utopia Bus Master, Output Configuration

# bytes	Word 0	1	4	Register 0x14 INADD UDF	H5 UDF	PRE LEN	Notes
52	N	N	N	X	0	00	Short cell, no PHY ID
54	**N**	**N**	**Y**	**X**	**1**	**00**	**Default, Utopia compatible, no PHY ID**
54	N	Y	N	X	0	01	2 user bytes, H1-H4, no PHY ID
56	N	Y	Y	X	1	01	2 user bytes, H1-H4, H5/UDF, no PHY ID

9.1.2 SCI-PHY or Utopia Bus Slave

The SCI-PHY/Utopia bus slave format is enabled when the IANYPHY, OANYPHY, IMASTER, and OMASTER inputs are all tied low.

In the ingress direction (cells are transferred from the parallel bus input port to the LVDS links), the port presents itself as 32 PHY entities but is fully Utopia Level 2 compatible when 31 or fewer PHYs are active and IAVALID is tied high. Cells read from the bus are queued in a dedicated FIFO for each virtual PHY (hereafter referred to as a logical channel). The ability of the FIFOs to accept additional cells is discovered through polling using the IADDR[4:0] and IAVALID inputs. Upon IAVALID being sampled high the ICA output is asserted if the cell FIFO for the logical channel addressed by IADDR[4:0] has at least one empty cell buffer. If the FIFO is full, ICA is deasserted. If a cell transfer is in progress that will fill a logical channel FIFO, ICA will also be deasserted. If IAVALID is sampled low (in SCI-PHY mode) ICA becomes high impedance.

When operating as a SCI-PHY/Utopia interface, a cell transfer is effected by the assertion low of IENB. The logical channel FIFO to which the cell is written is selected by the IADDR[4:0] value sampled when IENB was last sampled high.

The SCI-PHY/Any-PHY Input Configuration 1 register (0x0C) determines the cell format of the input bus. A SCI-PHY/Utopia input bus slave neither requires nor supports embedded PHY ID. The cell length options for the 8 bit bus (shown in Fig. 6) are described in Table 6. 16 bit bus options (shown in Fig. 7) are described in Table 7. Note that these options are identical to the SCI-PHY/Utopia input bus master configuration.

Table 6 Eight Bit SCI-PHY/Utopia Bus Slave, Input Configuration

	Byte				Register 0x0C		
# bytes	**0**	**1**	**2**	**7**	**H5UDF**	**PRELEN**	**Notes**
52	N	N	N	N	0	00	H1-H4, no H5 byte
53	**N**	**N**	**N**	**Y**	**1**	**00**	**Default, Utopia compatible**
53	N	Y	N	N	0	01	1 user byte then H1-H4
54	N	Y	N	Y	1	01	1 user byte then H1-H5
54	N	Y	Y	N	0	10	2 user bytes then H1-H4
55	N	Y	Y	Y	1	10	2 user bytes then H1-H5

Table 7 Sixteen Bit SCI-PHY/Utopia Bus Slave, Input Configuration

	Word			Register 0x0C		
# bytes	**0**	**1**	**4**	**H5UDF**	**PRELEN**	**Notes**
52	N	N	N	0	00	H1-H4, no H5/UDF field
54	**N**	**N**	**Y**	**1**	**00**	**Default, Utopia compatible**
54	N	Y	N	0	01	1 user word then H1-H4
56	N	Y	Y	1	01	1 user word, H1-H4, then H5/UDF

In the egress direction (cells are transferred from the LVDS to the output port), the port appears as a single addressable SCI-PHY/Utopia Level 2 slave. The cells received on the high-speed serial link are queued in FIFOs dedicated to each logical channel. The corresponding PHY ID of each cell is encoded in system prepend bytes sent over the LVDS link. The S/UNI-DUPLEX autonomously multiplexes the traffic from up to 32 logical channels and presents it as a single cell stream on the output bus. If at least one cell is present in any of the FIFOs, OCA will drive high when the device is polled.

Polling occurs when OAVALID is sampled high and the sampled OADDR[4:0] matches the OAD[4:0] bits in the Output Address Match register. Utopia L2 compatibility is achieved if OAVALID is tied high and OAD[4:0] is not all ones.

A cell transfer will be enacted if the OADDR[4:0] value equals the state of the OAD[4:0] bits in the Output Address Match register when the OENB is last sampled high.

In SCI-PHY bus mode a word is prepended to the transferred ATM cell to identify the cell's source (i.e. a logical channel number). To retain Utopia Level 2 compatibility, the word identifying the logical channel can be placed in the H5/UDF field. The three most significant bits of the channel number in the 8-bit format and the 11 most significant bits of the prepend in the 16-bit format are derived from the contents of the Extended Address Match registers, which default to all zeros.

The SCI-PHY/Any-PHY Output Configuration register (0x14) determines the cell format on the output bus. The cell length options for the 8 bit bus (shown in Fig. 6) are described in Table 8. 16 bit bus options (shown in Fig. 7) are described in Table 9.

Table 8 Eight Bit SCI-PHY/Utopia Bus Slave, Output Configuration

	Byte				Register 0x14			
# bytes	**0**	**1**	**2**	**7**	**INADD UDF**	**H5 UDF**	**PRE LEN**	**Notes**
52	N	N	N	N	0	0	00	H1-H4 only, no PHY ID is generated
53	**N**	**N**	**N**	**Y**	**0**	**1**	**00**	**Default setting. Utopia compatible, standard 53 byte cell, no PHY ID**
53	N	Y	N	N	0	0	01	1 user byte, H1-H4, no PHY ID
54	N	Y	N	Y	0	1	01	1 user byte, H1-H5, no PHY ID
54	N	Y	Y	N	0	0	10	2 user bytes, H1-H4, no PHY ID
55	N	Y	Y	Y	0	1	10	2 user bytes, H1-H5, no PHY ID
53	**N**	**N**	**N**	**Y**	**1**	**X**	**00**	**Most common setting when Utopia compatibility is desired. Standard 53 byte cell, PHY ID embedded in H5.**
54	N	Y	N	Y	1	X	01	1 user byte, H1-H4, PHY ID in H5
55	N	Y	Y	Y	1	X	10	2 user bytes, H1-H4, PHY ID in H5

Table 9 Sixteen Bit SCI-PHY/Utopia Bus Slave, Output Configuration

# bytes	Word 0	Word 1	Word 4	Register 0x14 INADD UDF	Register 0x14 H5 UDF	Register 0x14 PRE LEN	Notes
52	N	N	N	0	0	00	H1-H4 only, no PHY ID
54	**N**	**N**	**Y**	**0**	**1**	**00**	**Default, Utopia compatible, no PHY ID**
54	N	Y	N	0	0	01	2 user bytes, H1-H4, no PHY ID
56	N	Y	Y	0	1	01	2 user bytes, H1-H4, H5/UDF, no PHY ID
54	**N**	**N**	**Y**	**1**	**X**	**00**	**Most common setting when Utopia compatibility is desired. Standard 54 byte cell, PHY ID embedded in H5/UDF.**
56	N	Y	Y	1	X	01	2 user bytes, H1-H4, PHY ID in H5/UDF

9.1.3 Any-PHY Slave

The Any-PHY bus slave format is enabled when the IANYPHY and OANYPHY inputs are high, and IMASTER, and OMASTER inputs are all tied low.

In the ingress direction (cells are transferred from the parallel bus input port to the LVDS links), the port presents itself as 32 PHY entities. Cells read from the bus are queued in a dedicated FIFO for each logical channel. As in the SCI-PHY bus mode, the ability of the FIFOs to accept additional cells is discovered through polling using the IADDR[4:0] and IAVALID inputs. Upon IAVALID being sampled low (note this is opposite to SCI-PHY mode) the ICA output is asserted if the cell FIFO for the logical channel addressed by IADDR[4:0] has at least one empty cell buffer. If the FIFO is full, ICA is deasserted. If a cell transfer is in progress that will fill a logical channel FIFO, ICA will also be deasserted. If IAVALID is sampled high ICA becomes high impedance. ICA is delayed by one bus cycle (i.e. one IFCLK cycle) in the Any-PHY bus configuration.

In Any-PHY mode cell transfer is initiated using inband selection. The first word of the cell, coincident with the assertion of the ISX signal, is used for logical channel selection. Cells are accepted by the S/UNI-DUPLEX if the value in the Extended Address field of Word 0 agrees with the Extended Address Match registers over the range of bits specified by the Extended Address Mask registers.

Table 10 summarizes the distinctions between the SCI-PHY/Utopia and Any-PHY protocols in the ingress direction.

Table 10 SCI-PHY/Utopia and Any-PHY Comparison, Ingress Direction

Attribute	SCI-PHY	Any-PHY
Latency	ICA is driven high or low immediately upon sampling IAVALID high and becomes high impedance immediately upon sampling IAVALID low.	ICA is driven or becomes high impedance on the IFCLK rising edge following the one that samples a IAVALID low or high respectively.
Logical Channel Selection	Logical channel is selected by IADDR[4:0] when IENB was last sampled high.	An extra word (Word 0) is prepended to the cell coincident with the assertion of the ISX signal. Word 0 is used for logical channel selection
ISX	Unused.	High coincident with the first word of the cell data structure.
ISOC	High coincident with the first word of the cell data structure.	Unused in the S/UNI-DUPLEX.
Autonomous deselection	Not supported. A subsequent cell is input (provided space is available) if IENB is held low beyond the end of a cell.	Supported. Subsequent writes are ignored if IENB is held low until ISX input is asserted.

The SCI-PHY/Any-PHY Input Configuration 1 register (0x0C) determines the cell format of the input bus. An Any-PHY input bus slave requires the embedded PHY ID to be present in Byte 0 or Word 0. The cell format options for the 8 bit bus (shown in Fig. 6) are described in Table 11. 16 bit bus options (shown in Fig. 7) are described in Table 12.

Table 11 Eight Bit Any-PHY Bus Slave, Input Configuration

	Byte				Register 0x0C		
# bytes	**0**	**1**	**2**	**7**	**H5UDF**	**PRELEN**	**Notes**
53	Y	N	N	N	0	00	PHY ID byte, then H1-H4, no H5 byte
54	**Y**	**N**	**N**	**Y**	**1**	**00**	**Default setting. PHY ID, then H1-H5**
54	Y	Y	N	N	0	01	PHY ID, 1 user byte then H1-H4
55	Y	Y	N	Y	1	01	PHY ID, 1 user byte then H1-H5
55	Y	Y	Y	N	0	10	PHY ID, 2 user bytes then H1-H4
55	Y	Y	Y	Y	1	10	PHY ID, 2 user bytes then H1-H5

Table 12 Sixteen Bit Any-PHY Bus Slave, Input Configuration

# bytes	Word 0	Word 1	Word 4	Register 0x0C H5UDF	Register 0x0C PRELEN	Notes
54	Y	N	N	0	00	PHY ID word, then H1-H4, no H5/UDF field
56	**Y**	**N**	**Y**	**1**	**00**	**Default, PHY ID, H1-H4, then H5/UDF**
56	Y	Y	N	0	01	PHY ID, user word, then H1-H4, no H5/UDF
58	Y	Y	Y	1	01	PHY ID, user word, H1-H4, then H5/UDF

In the egress direction (cells are transferred from the LVDS to the output port), the port appears as a single addressable Any-PHY slave. The S/UNI-DUPLEX autonomously multiplexes the traffic from up to 32 logical channels and presents it as a single cell stream on the output bus. If at least one cell is present in any of the FIFOs, OCA will drive high when the device is polled. OCA is delayed by an additional clock cycle (one OFCLK) in the Any-PHY configuration.

Polling occurs when OAVALID is sampled low and the sampled OADDR[4:0] matches the OAD[4:0] bits in the Output Address Match register.

A cell transfer will be enacted if the OADDR[4:0] value equals the state of the OAD[4:0] bits in the Output Address Match register when the OENB is last sampled high. A word prepended to the transferred ATM cell identifies the logical channel. The three most significant bits of the prepend in the 8-bit format and the 11 most significant bits of the prepend in the 16-bit format are derived from the contents of the Extended Address Match registers, which default to all zeros.

Table 13 summarizes the distinctions between the two protocols in the egress direction.

Table 13 SCI-PHY/Utopia and Any-PHY Comparison, Egress Direction

Attribute	SCI-PHY/Utopia	Any-PHY
Latency	ODAT[15:0], OPRTY and OSOC are driven or become high impedance immediately upon sampling OENB low or high, respectively. OCA is driven immediately upon sampling a OADDR[4:0] value that matches the contents of the Output Address Match register.	0DAT[15:0], 0PRTY, 0SOC and OSX are driven or become high impedance on the OFCLK rising edge following the one that samples OENB low or high, respectively. OCA is driven on the OFCLK rising edge following the one that samples a OADDR[4:0] value that matches the content of the Output Address Match register.
OSX	Undefined. It is low when not high impedance.	High coincident with the first word of the cell data structure.

OSOC	High coincident with the first word of the cell data structure.	High coincident with the second word of the cell data structure.
Paused transfers	Permitted by deasserting OENB high, but the S/UNI-DUPLEX the address presented on OADDR[4:0] must match the content of the Output Address Match register the last cycle OENB is high to reselect the device.	Permitted by deasserting OENB high. The cell transfer resumes unconditionally when OENB is asserted low again.
Autonomous deselection	Not supported. A subsequent cell is output (provided one is available) if OENB is held low beyond the end of a cell.	The outputs become high impedance after the last word of a cell is transferred until the S/UNI-DUPLEX is reselected.

The SCI-PHY/Any-PHY Output Configuration register (0x14) determines the cell format on the output bus. Byte 0 or Word 0 will always contain the channel ID. The cell length options for the 8 bit bus (shown in Fig. 6) are described in Table 14. 16 bit bus options (shown in Fig. 1) are described in Table 15.

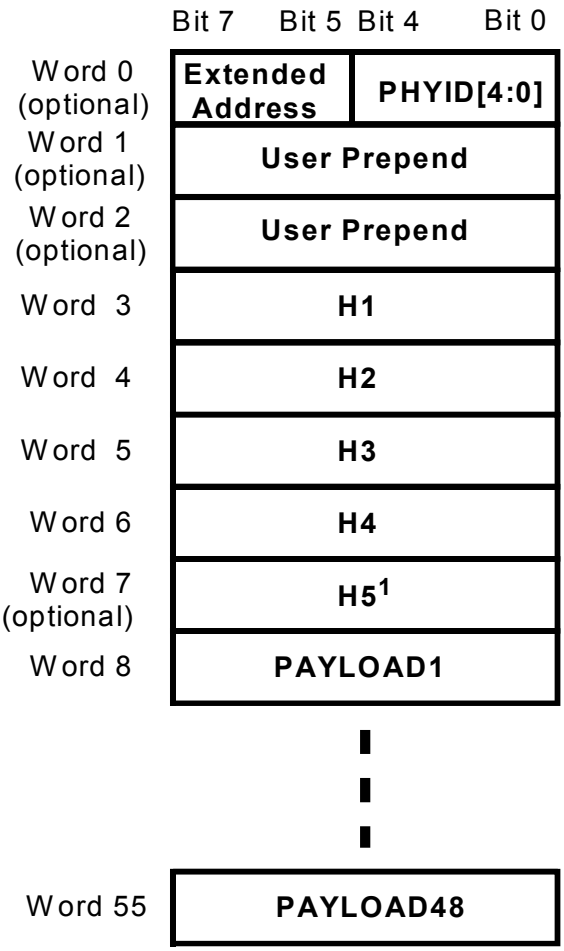
Table 14 Eight Bit Any-PHY Bus Slave, Output Configuration

	Byte				Register 0x14			
# bytes	0	1	2	7	INADD UDF	H5 UDF	PRE LEN	Notes
53	N	N	N	N	X	0	00	PHY ID in byte 0, then H1-H4
54	**N**	**N**	**N**	**Y**	**X**	**1**	**00**	**Default setting. PHY ID , then H1-H5**
54	N	Y	N	N	X	0	01	PHY ID, 1 user byte, then H1-H4
55	N	Y	N	Y	X	1	01	PHY ID, 1 user byte, then H1-H5
55	N	Y	Y	N	X	0	10	PHY ID, 2 user bytes, then H1-H4
56	N	Y	Y	Y	X	1	10	PHY ID, 2 user bytes, then H1-H5

Table 15 Sixteen Bit SCI-PHY/Utopia Bus Slave, Output Configuration

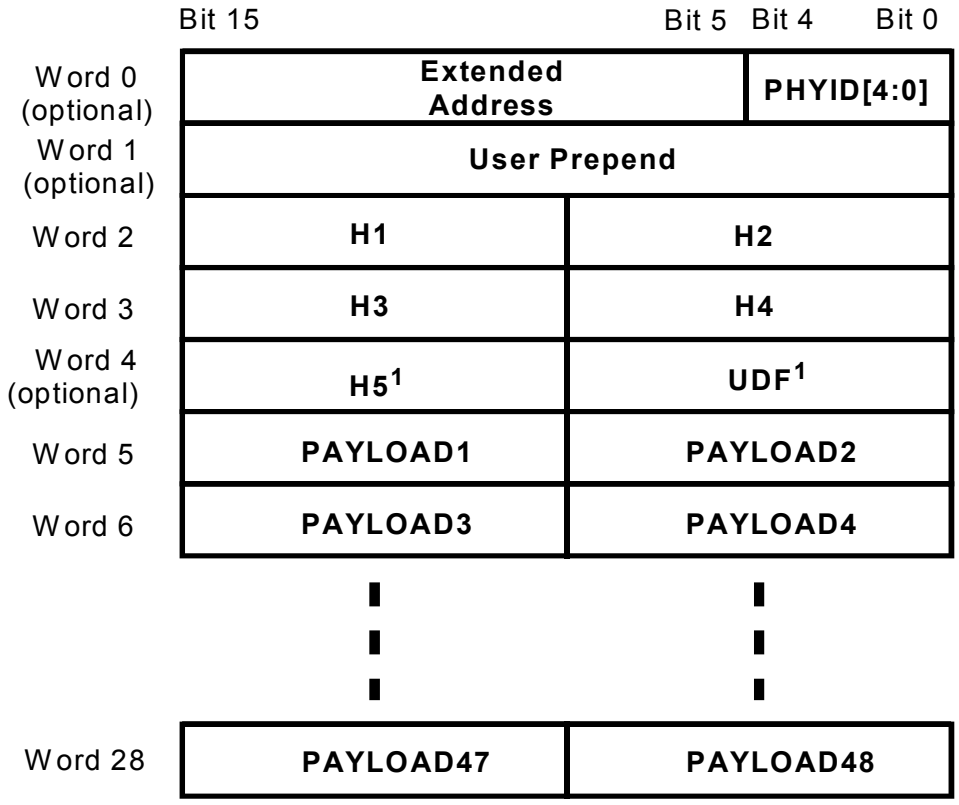
	Word			Register 0x14			
# bytes	0	1	4	INADD UDF	H5 UDF	PRE LEN	Notes
54	N	N	N	X	0	00	PHY ID in word 0, then H1-H4
56	**N**	**N**	**Y**	**X**	**1**	**00**	**Default setting. PHY ID , H1-H4, then H5/UDF**
56	N	Y	N	X	0	01	PHY ID , 2 user bytes, H1-H4
58	N	Y	Y	X	1	01	PHY ID , 2 user bytes, H1-H4, H5/UDF

Fig. 6 Eight Bit SCI-PHY/Utopia/Any-PHY Cell Format



Note 1: Optionally, the H5 field can be overwritten by the Extended Address and PHYID[4:0].

Fig. 7 Sixteen Bit SCI-PHY/Utopia/Utopia Cell Format



Note 1: Optionally, the H5/UDF fields can be overwritten by the Extended Address and PHYID[4:0].

9.2 Clocked Serial Data Interface

In some systems the PHY devices to which the S/UNI-DUPLEX is to interface may not contain an integrated Transmission Convergence function even though the low level protocol being transported over that interface is I.432 compliant ATM cells. For these types of devices (typically framers or modems) the S/UNI-DUPLEX provides up to 16 bi-directional clocked serial data interfaces with fully integrated, I.432 compliant, Transmission Convergence (TC) functions to allow cell structured bit streams to be exchanged with the modems. The modems perform all Physical Media Dependent (PMD) functions so that the bit streams contain only contiguous ATM cells. The S/UNI-DUPLEX requires that the clock is gapped during PMD overhead bit locations.

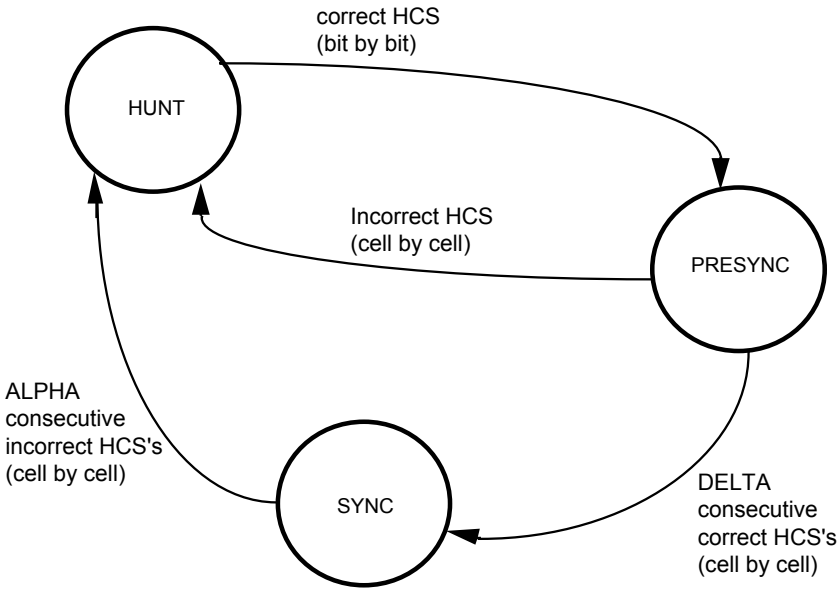
9.2.1 Upstream Functions

In the upstream direction (input from the modems), the S/UNI-DUPLEX provides 2 inputs (clock and data) per channel and implements HCS cell delineation, payload descrambling, idle cell filtering and header error detection to recover valid ATM cells. These functions are performed in accordance with ITU-T Recommendation I.432.1.

When configuring the S/UNI-DUPLEX in clocked serial data mode the user must modify the Transmit Logical Channel FIFO Depth register (0x5E) accordingly. See the register descriptions for details.

Cell delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the ATM cell header. The HCS is a CRC-8 ($x^8 + x^2 + x + 1$) calculation over the first 4 octets of the ATM cell header. In accordance with ITU-T Recommendation I.432.1, the coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. The cell delineation circuitry performs a sequential bit-by-bit hunt for a correct HCS sequence. This state is referred to as the HUNT state. When a correct HCS is found, a particular cell boundary is assumed and the PRESYNC state is entered. This state verifies that the previously detected HCS pattern was not a false indication. If the HCS pattern was a false indication then an incorrect HCS should be received within the next DELTA cells and the delineation state machine falls back to the HUNT state. If an incorrect HCS is not found in this PRESYNC period then a transition to the SYNC state is made, cell delineation is declared and all non-idle cells with a correct HCS are passed on. In the SYNC state synchronization is not relinquished until ALPHA consecutive incorrect HCS patterns are found. In such an event a transition is made back to the HUNT state. The state diagram of the cell delineation process is shown in Fig. 8.

Fig. 8 Cell delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6.

The loss of cell delineation (LCD) alarm is declared after a programmable threshold of incorrect cells occurs while in the HUNT state. The threshold is set by the Receive Serial LCD Count Threshold register. The threshold has a default value of 104 which translates to 73 ms at 600 kbs.All idle cells are filtered out and not passed to the high-speed interface. They are identified as cells containing all zeros VPI, and VCI fields and a one in the CLP bit. Optionally, unassigned cells (like idle cells except CLP is a zero) may also be filtered.

All cells with an incorrect HCS octet are filtered out. Header correction is not implemented.

As an option configured in Receive Serial Indirect Channel Configuration register (0x69), the ATM Transmission Convergence functions can be disabled to provide a clear channel capability. In this case, the serial data is segmented into 53 byte packets independent of the contents, and then transported across the high-speed LVDS links.

9.2.2 Downstream Functions

In the downstream direction (toward the modems), the S/UNI-DUPLEX uses one clock input and one data output per channel to produce valid ATM cell streams with correct HCS octets and inserted idle cells to adapt to the clock generated by the modem.

Each modem provides its own clock, which may be asynchronous to all others. The S/UNI-DUPLEX responds to the active edge of each transmit clock by generating a single bit. Idle cells are automatically generated and interleaved with the cells available from the high-speed serial interface to match the channel's bit rate as driven by the clock input.

When it needs to insert transmission overhead (such as framing bits) into the data stream provided by the S/UNI-DUPLEX, the modem is expected to gap the downstream clock provided to the S/UNI-DUPLEX so that no data bits are output during the overhead bit period(s).

Optionally, the S/UNI-DUPLEX can be programmed (using register 0x74) to optionally force octet alignment of the data to overhead by monitoring the clock gaps. To support dynamically adaptable modem rate without external intervention, the system automatically adapts to frequency changes on LTXC[15:0]. When byte alignment is enabled, the clock gap period is monitored on each LTXC[15:0] input. If the gap period is greater than the minimum detectable period, the most significant bit of the data octet is output during the gap period, allowing the receiving modem to receive it on the first clock active edge after the gap.

The S/UNI-DUPLEX can detect clock gaps of eight clock periods over the permitted LTXC[15:0] clock line frequency range. The frequency range over which one bit framing gap can be detected changes linearly with the speed of the high-speed links. When operating the LVDS interface at 200 Mb/s (REFCLK frequency set to 25 MHz), the S/UNI-DUPLEX will detect one bit clock gap for a line frequency range of 200 kHz to 8 MHz. At the minimum frequency of 100 Mb/s (REFCLK frequency of 12.5 MHz) the line frequency range at which one bit framing gap can be detected is 100 kHz to 4 MHz.

As an option (see Transmit Serial Indirect Channel Data register 0x71) the transmitted data stream can be provided clear channel by disabling HCS generation and payload scrambling. It is the responsibility of the traffic generation entity at the other end of the LVDS link to send traffic at a sufficient rate to keep the internal FIFOs from emptying, else the clear channel data will be interrupted by an automatically generated ATM idle cell pattern.

9.3 High-Speed Serial Interface

The S/UNI-DUPLEX provides backplane interconnection via 100 to 200 Mb/s serial links. All data destined to and coming from the core cell processing card are concentrated on these high-speed links. The transceivers support UTP-5 cable lengths up to 10m. To avoid clock skew issues, no clock is transmitted and the receivers recover a local clock from the incoming data.

Two bi-directional LVDS links are provided for redundancy; each link is intended to be routed to different core cards. Both LVDS transmitters carry identical traffic except for internally generated overhead. Both links are frequency locked to the single input reference clock although their phase is not guaranteed to match. At the LVDS receivers clock recovery and cell delineation are always active for both receivers to allow a quick switch to the redundant core card with minimal cell loss.

The serial links carry ATM cells with prepended bytes. The cell format is illustrated in Fig. 9 and discussed in Section 12.2). The S/UNI-DUPLEX appends the first four bytes and the Header Check Sequence (HCS) byte in the upstream direction and strips them off and parses them in the downstream direction. The remainder of the bytes in the data structure are transferred transparently. The bytes are serialized most significant bit first. The bit stream is a simple concatenation of the extended cells. Cell rate decoupling is accomplished through introduction of stuff cells.

The transmitter inserts a correct CRC-8 that protects both the ATM cell header and prepended bytes in the HCS byte. Cells with an errored HCS are counted and then discarded. The receiver also uses the HCS byte for determining cell delineation. Failure to establish cell alignment results in a loss of cell delineation (LCD) alarm. The entire bit stream is scrambled with a $x^{43} + 1$ self-synchronous scrambler.Table 16 summarizes the contents of the system prepended bytes.

Fig. 9 High-Speed Serial Link Data Structure

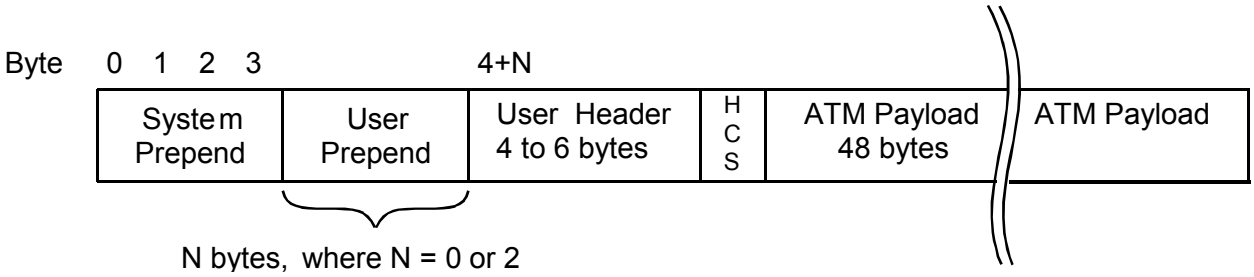


Table 16 Prepended Fields

Byte	Bits	Mnemonic	Description
0 1	7:0 7:0	CA[15:8] CA[7:0]	The CA[15:0] bits carry per-PHY flow control information in the upstream direction. To support 32 PHYs, the status for each PHY is sent every other cell; the CASEL indicates which half is represented. If CASEL is logic 0, CA[15:0] corresponds to those PHYs with addresses 0 through 15. If CASEL is logic 1, CA[15:0] corresponds to those PHYs with addresses 16 through 31. In the downstream direction, CA[15:0] communicates congestion of the upstream entity. The encoding is identical to the upstream direction. A logic 0 indicates the far end can accept no more cells for a specific logical channel. A logic 1 indicates the S/UNI-DUPLEX is free to send queued traffic for that logical channel immediately. In the event of an errored header (as detected by an incorrect HCS), the CA bits will be assumed to be all zero. This ensures cells are not transmitted for which there is no buffer space.
2	7	CASEL	The state of the CA select bit determines which half of the PHY devices the CA[15:0] bits correspond to. CASEL toggles with each cell transmitted.

Byte	Bits	Mnemonic	Description
2	6	UPCA	The UPCA bit carries flow control information for the microprocessor control channel. If this bit is one, control channel cells may be transferred. In the event of an errored header, the UPCA bit will be assumed to be zero. This ensures cells are not transmitted for which there is no buffer space.
2	5:0	PHYID	The PHY identifier determines to which PHY a cell is destined in the downstream direction and from which PHY it came in the upstream direction. It also indicates whether the cell is a stuff or control channel cell. The field is encoded as follows: "111111" – Stuff cell provided for cell rate decoupling. The payload carries no useful data and the cell shall be discarded. "111110" – Control channel cell. On the transmit serial link, PHYID shall equal this value for all cells inserted via the Microprocessor Cell Buffer. All cells received on the serial link with this encoding will be routed to the local microprocessor. "100000" to "111101" – Reserved "000000" to "011111" – Logical channel index for the PHY devices.
3	7	BOC	The Bit Oriented Code (BOC) bit position carries a repeating 16 pattern that encodes one of 63 possible code words used for remote control and status reporting. Five codes are predefined to represent a remote defect, a loopback activate request, a loopback deactivate request, a reset activate request and a reset deactivate request. The remaining codes are either reserved or user defined. The receiver ensures the pattern is the same for 10 (default) or 5 repetitions before

Byte	Bits	Mnemonic	Description
			validating a new code word. Refer to the 9.3.1 section for more details.
3	6	ACTIVE	The link active bit indicates which of the redundant links is currently chosen. The S/UNI-DUPLEX will switch to the link which contains a one in this location for at least 3 consecutive cells. The local microprocessor can override this selection. If both links present a one in this location, the selection remains unchanged. To confirm which link is active, the transmitted ACTIVE bit will be a one if the associated receive link is selected. In the event of an errored header, the previous ACTIVE value is retained.
3	5:0	TREF[5:0]	The timing reference encodes an 8 kHz signal inband that is independent of the serial bit rate. The TREF[5:0] binary value represents the number of high-speed link bytes after this one at which the timing reference is inferred. An all ones value indicates no timing mark is associated with this cell.

The transmitter outputs are internally terminated current mode drivers. Correct termination is at the receiver required to provide appropriated signal levels.

The internal transmit clock is synthesized from a 12.5 MHz to 25 MHz clock. The resulting data bit rate is eight times the frequency of the REFCLK input. All jitter below 1 MHz on REFCLK is passed unattenuated to the TXD1+/- and TXD2+/- outputs. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free reference input and a low noise board layout, the intrinsic jitter is typically less than 0.01 UI RMS and 0.10 UI peak-to-peak when measured using a band pass filter with 12 kHz and 1.3 MHz cutoff frequencies.

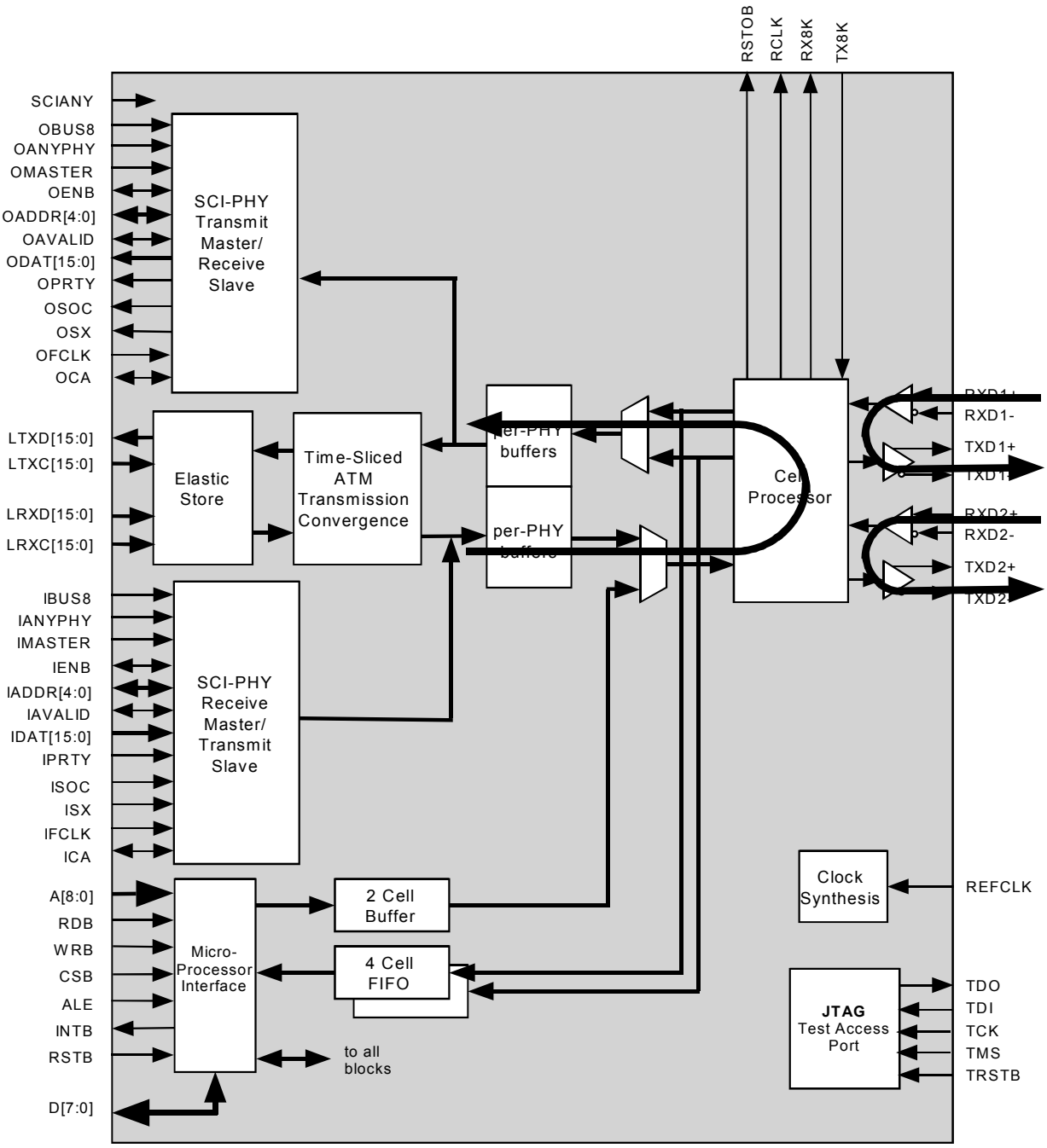
The two truly differential receivers are capable of handling signal swings down to 100mV. A wide common mode range makes them compatible with LVDS signals. External termination resisters must be provided to match the cable impedance.

The receivers monitor for loss of signal (LOS) on the links. LOS is declared upon 2048 bit periods (13.2 μs at 155.52 Mb/s) without a signal transition in the scrambled data. As a consequence, a status bit is set, a maskable interrupt is asserted and the RDI (Remote Defect Indication) codeword is sent repetitively in the BOC bit in the corresponding downstream link. The LOS indication is cleared when a signal transition has occurred in each of 16 consecutive intervals of 16 bit periods each.

Clock recovery is performed by a digital phase locked loop (DPLL). The implementation is robust against operating condition variations and power supply noise. The receive link is constrained to be within 100 ppm of eight times the REFCLK frequency.

As shown in Fig. 10, two datapath loopbacks are provided on each LVDS link to aid in fault isolation and continuity verification. The metallic loopback routes high-speed serial receive data to the transmitter. The diagnostic loopback replaces the downstream data with the upstream data. The loopbacks can be enabled individually or simultaneously, and each link can be looped back independently of the other.

Fig. 10 Datapath Loopback



A diagnostic loopback is effected if the DLB bit of the Serial Links Maintenance register (0x05) corresponding to the active high-speed serial link is set to logic 1 (DLB1 or DLB2 depending if data is being received from the RXD1+/- or RXD2+/- inputs). The upstream data and clock are inserted into the downstream datapath

after clock recovery. Setting the DLB bit corresponding to the inactive link has no effect.

The metallic loopback is set independently on each high-speed serial link. It can be effected in one of three ways: after the receipt of the loopback activate code on the corresponding RXD1+/- or RXD2+/- inputs (as described in Section 9.3.2) when the corresponding MLB1 or MLB2 bit of the Serial Link Maintenance register is set to logic 1 or when the reset (RSTB) input is asserted low. The loopback occurs at the LVDS transceiver after the conversion to digital but before clock recovery. The looped back data may be slightly distorted by the data slicing (differential to single-ended) and re-buffering that occurs.

Metallic loopback is terminated if a loopback deactivate bit oriented code is received and validated, provided the corresponding MLB1 or MLB2 bit of the Serial Links Maintenance register to logic 0.

9.3.1 Link Integrity Monitoring

Although the serial link bit error rate can be inferred from the accumulated Header Check Sequence (HCS) errors, the option exists to perform error monitoring over the entire bit stream.

When the feature is enabled the second User Prepend byte transmitted shall be overwritten by the CRC-8 syndrome for the preceding cell. The encoding is valid for all cells, including stuff cells. The CRC-8 polynomial is $x^8 + x^2 + x + 1$. The receiver shall raise a maskable interrupt and optionally increment the HCS error count. Simultaneous HCS and cell CRC-8 errors result in a single increment.

9.3.2 Bit Oriented Codes

Bit Oriented Codes (BOCs) are carried in the BOC bit position in the System Prepend. The 63 possible codes can be used to carry predefined or user defined signaling.

Bit oriented codes are transmitted as a repeating 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0). The code to be transmitted is set independently on the two LVDS links, and is programmed by writing the TXD1 Bit Oriented Code and TXD2 Bit Oriented Code registers. The autonomously generated Remote Defect Indication (RDI) code, which is generated upon a loss-of-signal or loss-of-cell-delineation, takes precedence over the programmed code. RDI insertion can be disabled via the RDIDIS bit of the Serial Links Maintenance register. RDI can be inserted manually on a high-speed serial link by setting the corresponding TXD1 Bit Oriented Code or TXD2 Bit Oriented Code register to all zeros.

The receiver can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the Bit Oriented Code Receiver Enable register. Unless fast declaration is necessary, it is recommended that the AVC bit be set to logic 0 to improve bit error tolerance. Valid BOC are indicated through the RXD1 Bit Oriented Code Status and RXD2 Bit Oriented Code Status registers. The BOC bits are set to all ones (111111) if no valid code has been detected. A maskable interrupt is generated to signal when a detected code has been validated, or optionally, when a valid code goes away (i.e. the BOC bits go to all ones).

When the receiver is out of cell delineation (OCD), the BOC detection is disabled and the corresponding RXD1 or RXD2 Bit Oriented Code Status register will produce all ones (111111). .

The valid codes are provided in Table 17. The Reserved codes anticipate future enhanced feature set devices and should not be used. The User Defined codes may be used without restriction. Regardless of definition, all 63 codes may be validated and read by a microprocessor. Only four codes result in autonomous action: loopback activate, loopback deactivate, reset output activate and reset output deactivate.

Note that processing of the metallic loopback activate code is handled as a special case. The RXD1+/-, RXD2+/- data is looped back onto TXD1+/-, TXD2+/- respectively at the end of the reception of the loopback activate code on the corresponding high-speed serial link rather than when the code is first validated. For the loopback to be enabled the loopback code must be first validated (received 8 out of 10 times at least once) and then invalidated, typically by reception of another code. The loopback is not enable upon initial validation of the loopback activate code because the looped back signal, which still contains the original loopback activate command, would cause the far-end receiver to go into metallic loopback, thereby forming an undesirable closed loop condition! The loopback is cleared immediately upon the validation of the loopback deactivate code, assuming the corresponding MLB register bit of the Serial Links Maintenance register is logic 0.

To produce a loopback at the far end, program the desired TXD1 Bit Oriented Code or TXD2 Bit Oriented Code register with the loopback activate code for at least 1 ms and then revert to another (typically idle) code. Upon termination of the loopback activate code, the data transmitted on TXD1+/- or TXD2+/- is expected to be received verbatim on the RXD1+/- or RXD2+/- inputs. When transmitting a loopback activate code on a high-speed serial link, it is recommended the corresponding RDIDIS1 or RDIDIS2 register bit be set to logic 1, or else a loss-of-signal or loss-of-cell-delineation event would cause a premature loopback due to a pre-emptive Remote Defect Indication (RDI) code being sent.

The remote reset activate and remote reset deactivate code words are used to control the RSTOB output. If the remote reset activate code is validated, the RSTOB output is asserted low. If the remote reset deactivate code is validated the RSTOB output becomes high impedance. RSTOB can also be controlled through the RESETO bit in the Master Configuration register.

The Remote Defect Indication (RDI) is sent whenever Loss of Signal (LOS) or Loss of Cell Delineation (LCD) is declared. This code word takes precedence over all others.

Table 17 Assigned Bit Oriented Codes

Function	Codeword (left bit transmitted first)
Remote Defect Indication (RDI)	11111111 00000000
Loopback activate	11111111 01000000
Loopback deactivate	11111111 00100000
Remote reset activate	11111111 01100000
Remote reset deactivate	11111111 00010000
Reserved	11111111 01010000
. . .	. . .
Reserved	11111111 00000100
User Defined	11111111 01000100
. . .	. . .
User Defined	11111111 00111110
Idle Code	11111111 01111110

9.3.3 Cell Delineation Process

The S/UNI-DUPLEX performs HCS cell delineation, payload descrambling, idle cell filtering and header error detection to recover valid cells from the receive high-speed links. These functions are performed with a similar algorithm as for the upstream Clocked Serial Data interface described in Section 9.2.1 but support 9 to 13 byte cell headers.

The loss of cell delineation (LCD) alarm is declared after 1318 consecutive cell periods (4.0 ms at 155.52Mb/s) in the HUNT or PRESYNC states. The LCD alarm is cleared after 1318 consecutive cells in the SYNC state.

9.3.4 Protection Switching Protocol

The S/UNI-DUPLEX and its sister device, the S/UNI-VORTEX inherently support system architectures requiring fault tolerance and 1:1 redundancy of the system's common equipment. In point-to-point backplane architectures such as these, the 1:1 protection also includes the associated LVDS links connecting the common equipment to the line cards. The S/UNI-VORTEX and S/UNI-DUPLEX perform clock recovery, cell delineation, and header error monitoring for all receive high-speed serial links simultaneously. The maintained error counts and alarm status indications may be used by the control system to determine the state and viability of each LVDS link. See the S/UNI-VORTEX data sheet for additional details.

In these architectures, each S/UNI-DUPLEX will be connected to two S/UNI-VORTEXs (see Fig. 1) or to two S/UNI-DUPLEXs (see Fig. 5). Upon a failure of the active card, the spare card becomes the conduit for traffic. The S/UNI-VORTEX and S/UNI-DUPLEX facilitate link selection upon start-up as well as switching between links upon failure conditions.

Typically a centralized resource or cooperating distributed microprocessor subsystems will determine which common card is to be considered active for each downstream S/UNI-DUPLEX and sets the active indication accordingly. The current state of the link's active bit is sent downstream once per transmitted cell. The active status is debounced and acted upon by the far-end S/UNI-DUPLEX.

The S/UNI-DUPLEX will only accept data traffic from one of its two LVDS links, and normally it is the link marked active that is considered the working link (although this can be overridden locally as discussed below). Thus, although the far-end S/UNI-VORTEX or S/UNI-DUPLEX may indicate the desired active and spare links, it is actually the local S/UNI-DUPLEX that must enforce the protection switching. The link switching mechanism preserves cell integrity on the high-speed serial link that becomes active. In other words, switching occurs between cells.

At reset Link 1 is marked as the active link. It is also important to note that a Loss of Signal (LOS) on the active LVDS link does not automatically affect the value of the ACTIVE bit. The ACTIVE bit value prior to the LOS condition is maintained unless the other link's active indication is asserted (after debouncing) or until a local override (described below) or device reset is invoked. The value of the extracted ACTIVE bit is forced to logic 0 when the corresponding link is in Loss of Cell Delineation (LCD) state.

If the S/UNI-DUPLEX is auto-selecting its active link status (Master Configuration register 0x01, RXAUTOSEL = 1) the active bit transmitted on the two LVDS links

will indicate which link is currently chosen as active. This reflected ACTIVE bit may not have a direct affect on the far end S/UNI-VORTEX or S/UNI-DUPLEX, but its status is typically debounced (must remain the same for 3 received cells) and then stored by the far end device. The reflected status is normally monitored by the control system to determine when protection switching has been completed. The S/UNI-DUPLEX stores its LVDS active indication in the ACTIVE bit in Master Configuration register (0x01).

The S/UNI-DUPLEX can override active link selection in the receive direction or force link selection in the transmit direction (this applies to the S/UNI-DUPLEX to S/UNI-DUPLEX type configuration) using the Master Configuration register (0x01). If the S/UNI-DUPLEX is forcing its ACTIVE link status (Master Configuration register 0x01, RXAUTOSEL = 0) the active receive link and the transmitted ACTIVE bit on the two LVDS links will reflect the status of the Master Configuration register ACTIVE bit. If ACTIVE is 0 then LVDS link 1 receiver will be active and link 1 transmitter will indicate it is active, while LVDS link 2 transmitter will indicate it is inactive. If the ACTIVE bit is 0 the opposite indications will occur.

9.4 Cell Buffering and Flow Control

The possibility of congestion is inherent in an access multiplexer. In the downstream direction, the WAN link can generate a burst of cells for a particular PHY device at a rate far exceeding the modem's bandwidth capacity. Therefore, feedback to the core card is required to cause it to buffer and smooth cell bursts to prevent downstream buffer overflow. In the upstream direction, the subscribed aggregate bandwidth can exceed that accommodated by the WAN uplink. Flow control is required to ensure fair access to the uplink, to minimize cell loss and to minimize the impact of greedy users on others.

9.4.1 LVDS Receive Traffic Flow Control

In the LVDS receive direction the primary task of the S/UNI-DUPLEX is to accept cells from the active high speed link, inspect the PHYID field to determine the destination of the cell, and then route the cell to the appropriate parallel bus PHY, clocked serial data interface, or to the microprocessor port. Because the LVDS link typically supports a much higher transfer bandwidth than the external devices, rate decoupling and flow control are implemented. Flow control signaling is implemented using in-band system overhead appended to each cell sent over the LVDS link (see Table 16).

On the currently active link user cells (those destined to the parallel bus or clocked serial data interfaces) and inter-processor communication channel cells (those destined to the microprocessor port) are processed. On the inactive link only inter-processor communication cells (hereafter called control cells) are

processed – user cells are discarded. Both links discard stuff cells after extracting the system overhead. The active link uses all fields of the system overhead on each cell. The inactive link monitors the PHYID (only to identify control channel cells), the ACTIVE, BOC, and TREF fields. Both links monitor for loss of signal and loss of cell delineation conditions. Cells received with an incorrect Header Check Sequence (HCS) (due to bit errors during transmission) are counted and discarded. The system overhead fields of errored cells are ignored.

User and control channel cells received from the high-speed serial link are temporarily stored in a shallow buffer partitioned into a separate FIFO for each logical channel. As discussed below, cells are read out of this buffer under the control of the parallel bus, the clocked serial data, or the microprocessor interface. The buffer is logically partitioned into a FIFO for each logical channel. Each FIFO has an associated flow control bit (CA for user cells, UPCA for the control channels) embedded within the prepended bytes in the upstream high-speed serial link.

The 34 (32 PHYs + 2 control channels) channel FIFOs are four cells deep. When a FIFO contains less than two cells, the corresponding flow control bit is set to allow cell transmission. Upon the beginning of the write of a cell which will place the second cell in the FIFO, the flow control bit becomes a zero until only one cell remains in the FIFO. The far end device (either another S/UNI-DUPLEX or a S/UNI-VORTEX) will only resume sending cells to that PHY or control channel when its flow control bit has been set to a one. Since the flow control bit is encoded into the next upstream cell (either a user data cell or a filler cell) there will be some latency between the setting and clearing of the flow control bit and the corresponding action by the far-end device. However, since the far-end buffer is four cells deep no overflow condition will occur.

The process of reading cells out of the per channel FIFOs and placing them on the parallel bus is flow controlled by the bus polling protocol, as discussed in Section 9.1. When operating with the clocked serial data interface, cells are read from the FIFO at a rate determined by the transmit clock provided to the S/UNI-DUPLEX by the modem. If the FIFO contains less than one complete cell when the previous cell has been serialized then an idle cell will be emitted. Idle cell generation has no impact of the channel's FIFO.

See Section 9.7.1 for a description of how the two control channel interfaces are presented to the microprocessor port.

9.4.2 LVDS Transmit Traffic Flow Control

In the LVDS transmit direction, the primary task of the S/UNI-DUPLEX is accept cells from the parallel bus, clocked serial interfaces, or microprocessor port

control channel, add system overhead to the cell (including the PHY ID), and then transmit the cell over both high speed links simultaneously. Per PHY rate decoupling and flow control are implemented to ensure head-of-line blocking and far-end buffer overflow never occur. Flow control signaling is implemented using in-band system overhead appended to each cell sent over the LVDS link (see Table 16).

The transmitted cell is identical on both links except for the ACTIVE field, the BOC bit and UPCA status field. Stuff cells are automatically generated and sent over the high speed link if there is no user data cell or control channel cell to send or if the far-end is indicating that it has no room in any of its per channel buffers.

It is important to note that the S/UNI-DUPLEX only acts on the CA and UPCA status fields of the active LVDS receive link. The inactive link's flow control information is ignored. This should be taken into account when designing 1:1 protected systems, especially with respect to the behavior of the standby common card data path and the embedded control channel.

Rate decoupling between the external PHYs and the LVDS link occurs via the per channel buffers. Specifically, independent internal processes determine how the buffers are filled and how they are scheduled onto the LVDS link.

When the S/UNI-DUPLEX is configured as a parallel bus master the 32 PHY devices are polled in a round robin fashion. When a polled external PHY indicates that it has a cell available the cell is transferred into a shallow FIFO. Each PHY has its own FIFO. If the per-channel flow control asserted by the far-end prevents cells from being transferred from a buffer to the LVDS transmit link, the buffer may fill to capacity, at which time the S/UNI-DUPLEX will remove that external PHY from the polling sequence until buffer space becomes available. Under congestion the S/UNI-DUPLEX does not discard cells, although the external PHY device may have to.

When the S/UNI-DUPLEX is configured as a parallel bus slave the PHY devices are polled by the bus master and the S/UNI-DUPLEX provides the appropriate FIFO status indication, as described in Section 9.1.2 and Section 9.1.3. If the per-channel flow control asserted by the far-end prevents cells from being transferred from a buffer to the LVDS transmit link, the buffer may fill to capacity, at which time the S/UNI-DUPLEX will deassert the buffer available status for that PHY when it is polled. Under congestion the S/UNI-DUPLEX does not discard cells, although the external bus master may have to.

When the S/UNI-DUPLEX is configured for clocked serial data interfaces, cells from the maximum 16 PHYs are buffered in 16 dedicated logical channel FIFOs. They should be programmed in the Transmit Logical Channel FIFO Depth

register (0x5E) to be four cells deep as per the I.432 specification. If flow control asserted by the far-end device prevents cells from a particular serial data interface from being read, the corresponding FIFO will begin to fill. In general, proper system engineering should ensure that the far-end is able to keep up, but should flow control continue to be asserted by the far-end an overflow condition could occur. Overflow results in an optional interrupt being raised, an error status register being set, and subsequently received cells being discarded until FIFO space is available.

Regardless of whether configured a bus master, bus slave, or clocked serial data device, the S/UNI-DUPLEX monitors the per-channel FIFOs and performs round robin scheduling of cells onto the transmit LVDS links. The control channel FIFO is given equal priority to the PHYs.

The device attached to the far-end of the LVDS link is typically a S/UNI-VORTEX (see Fig. 1) or a S/UNI-DUPLEX (see Fig. 4 and Fig. 5). Although the S/UNI-DUPLEX only implements one form of transmit flow control, to help understand the end-to-end flow control we will discuss the two situations separately.

Case #1: the far-end device is a S/UNI-VORTEX

The S/UNI-VORTEX is a parallel bus slave with a single receive buffer for each of its eight LVDS links. It uses a weighted round robin polling of these buffers and schedules the received cells onto the parallel bus under the control of the bus master. The S/UNI-VORTEX's eight LVDS links running at 200 Mb/s can provide aggregate traffic bursts that exceed the capacity of a 800 Mb/s parallel bus. Also, link polling weights may be set such that one or more links receive relatively less of the aggregate bus bandwidth. Therefore, it is quite likely that congestion will sometimes occur at the S/UNI-VORTEX's LVDS receive buffers.

Since all traffic received on the eight LVDS links is heading to the S/UNI-VORTEX's parallel bus there was no need to partition this FIFO into individual channels. Therefore the S/UNI-VORTEX implements flow control on each of its LVDS links in a binary fashion – all 32 logical channels are enabled or all channels are disabled. The S/UNI-VORTEX may or may not treat the microprocessor control channel independently from the user channels depending on how it is configured. If it is programmed to route control channel cells out over the parallel bus then the control channel flow control is identical to the 32 user channels. If the control channel is being routed to the microprocessor port then the control channel flow control is independent from the user channels.

When the S/UNI-VORTEX's LVDS receiver cell buffer becomes congested the S/UNI-VORTEX will immediately clear the CA bits and possibly the UPCA fields in Table 16 in the cells sent on the downstream LVDS link. When the S/UNI-

DUPLEX sees that all far-end channels are congested it will immediately start sending stuff cells on the upstream serial link (unless it has control channel cells to send and that channel is not marked as congested). With the worst case alignment between upstream and downstream links, the S/UNI-DUPLEX may transmit up to two cells after the cell available deassertion was first registered by the far-end S/UNI-VORTEX. The FIFO threshold on the S/UNI-VORTEX accounts for this latency, buffer overflow cannot occur.

Once the far-end S/UNI-VORTEX has a chance to clear cells from its receiver buffer it will reassert the cell available bit on all channels. Refer to the S/UNI-VORTEX Data Sheet for further information.

Case #2: the far-end device is a S/UNI-DUPLEX

Unlike the S/UNI-VORTEX, the far-end's S/UNI-DUPLEX's LVDS receive buffer is divided into 32 FIFOS, so it always individually indicates the status of the 32 user channels. This also applies to the control channel – its status in independent of the status of the user channels.

When the near-end S/UNI-DUPLEX sees that a PHY or control channel is congested it will take that channel out of the round robin scheduling used to transfer cells from the buffers to the transmit LVDS link. If none of the remaining channels have cells to send, or if all channels are experiencing congestion, then the S/UNI-DUPLEX will automatically broadcast a stuff cell on the two upstream serial links.

With worst case alignment between upstream and downstream links, the S/UNI-DUPLEX may transmit up to two cells to a channel after the cell available deassertion for that channel was first registered by the far-end S/UNI-DUPLEX. Since the FIFO threshold on the S/UNI-DUPLEX accounts for this latency, buffer overflow cannot occur on the active link.

Once the far-end S/UNI-DUPLEX has a chance to clear cells from the congested receive buffer it will reassert the cell available bit on the affected channel.

9.5 Timing Reference Insertion and Recovery

The high-speed serial links are capable of transporting a timing reference independent of the bit rate. The timing signal received on the active RXD1+/- or RXD2+/- inputs is presented on RX8K. Rising edges of TX8K input are encoded in the TXD1+/- and TXD2+/- cells.

Although the timing reference is targeted at a typical need of transporting an 8 kHz signal, its frequency is not constrained to 8 kHz. Any frequency less than the cell rate is permissible.

The rising edge of TX8K initializes an internal counter to the number of bytes in the high-speed serial cell minus one. The counter decrements with each byte transmitted. Upon the fourth byte of the next extended cell, the state of the counter is encoded in the TREF[5:0] field. If no rising edge on TX8K has occurred, TREF[5:0] is set to all ones.

In the receive direction, two independent counters are initialized to the value of TREF[5:0] extracted from RXD1+/- or RXD2+/-. The counters decrement with each byte received on its respective high-speed serial link. When the count becomes zero, a rising edge is generated on an internal reference signal associated to this counter. If the value of TREF[5:0] is all ones, the signal remains low. The internal reference signal of the high-speed serial link that is declared active is output on RX8K.

If the same functionality is implemented at the far end of the serial link, it can be seen that the recovered timing event is generated one cell period later than the inserted timing with a resolution of one byte. Because of the limited edge encoding resolution, some jitter is present. At a link rate of 155.52 Mb/s, 63ns of peak-to-peak jitter will occur on RX8K. A local high-Q phase locked loop (PLL) can be used to remove the jitter.

In systems where 1:1 protection is used the timing reference output on TX8K will change sources if the link marked active changes. Even though the S/UNI-DUPLEX maintains the edges being sent on both links, and even if the far end sources are synchronized, there is no guarantee that an arbitrary phase hit will not occur during protection switching.

In general the LVDS links will run error free, but if errors do occur the S/UNI-DUPLEX discards a cell that arrive with an HCS error. Hence it is possible that a transmission error could corrupt the cell carrying a clock edge indication in TREF[5:0]. This would result in that edge being lost (i.e. there would be no corresponding output on TX8K).

9.6 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-DUPLEX identification code is 173500CD hexadecimal.

9.7 Microprocessor Interface

The microprocessor interface is provided for device configuration and status monitoring by an external microprocessor. Normal mode registers and test mode

registers can be accessed through this port. Test mode registers are used to enhance the testability of the S/UNI-DUPLEX.

The interface has a 8-bit wide data bus. Multiplexed address and data operation is supported.

9.7.1 Inband Communication

A cell insertion and extraction capability provides a simple unacknowledged cell relay capability. For a fully robust control channel implementation, it is assumed the local microprocessor and the remote entity are running a reliable communications protocol.

In the upstream direction, identical copies of each control channel cell are broadcast on both the active and spare high-speed serial links. If the user wishes to implement two independent control channels (active/inactive or link 1/link 2) then the contents of the cell will have to indicate the cell's destination link. In the downstream direction, each high-speed serial link has a dedicated receive queue for the control channel cells.

The control channel is treated as a virtual PHY device. In the upstream direction, it is scheduled with the same priority as the other logical channels. Flow control with the receiving device (either a S/UNI-VORTEX or a S/UNI-DUPLEX) is based on the cell available bit (UPCA, see Table 16) of the high-speed serial link marked as active. In the downstream direction, control channel cells are queued in a four cell FIFO for each high-speed serial link. If either FIFO contains two or more cells, the cell available bit returned upstream on the corresponding high-speed link is deasserted to prevent cell loss when the microprocessor cell reads fail to keep pace with the incoming control channel cells.

9.7.2 Writing Cells

The S/UNI-DUPLEX contains a two cell buffer for the insertion of a cell by the microprocessor into the high-speed serial interface. Optional CRC-32 calculation over the last 48 bytes of the cell relieves the microprocessor of this task. The CRC-32 generator polynomial is consistent with AAL5:

5. $G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

All cells written by the microprocessor will have binary 111110 encoded in the PHYID[5:0] field within the cell prepend bytes. This distinction between user cells and control cells provides a clear channel for both types of cells.

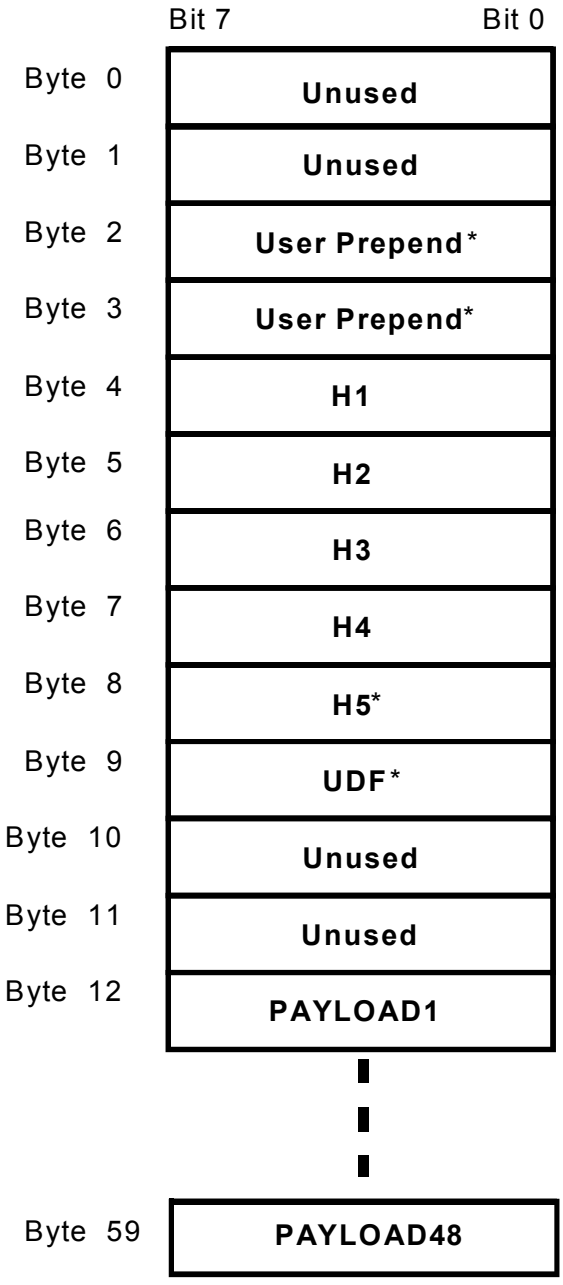
The microprocessor cell format is illustrated in Fig. 11. The 8-bit cell data structure is fixed at 60 bytes long regardless of how the SCI-PHY/Utopia/Any-PHY bus (or the Clocked Serial Data interface) and LVDS link are configured. The microprocessor must transfer all bytes of the cell, including the unused ones. The unused bytes are included in the received cell when it is made available to the far-end microprocessor, but the value of the bytes is undefined. This 60 bytes cell format is used to retain interface compatibility with the PM7326 S/UNI-APEX device, and to align the header and data fields on 32 bit boundaries.

Bytes marked with an asterisk in Fig. 11 must be included in cells written into the cell transfer register, but they will only be sent across the LVDS if the corresponding Transmit High-Speed Serial Configuration register (0x60) and the far-end's corresponding Receive High-Speed Serial Configuration register have been programmed to include them. See Section 12.2 for details.

Other than what has already been mentioned, there are no constraints on the contents of cells written by the microprocessor. They are transported across the LVDS link transparently. Specifically, although the standard ATM header bytes H1-H5 are shown in Fig. 11 there is no restriction on the values they can contain.

See Section 12.1.1 for details on the cell write protocol.

Fig. 11 Microprocessor Cell Format



*Depending on the serial link programming, these fields may be undefined or not transmitted.

9.7.3 Reading Cells

The microprocessor cell buffer has a capacity of four cells. The UPCA bit returned on the upstream high-speed serial link will be set to logic 0 when the buffer contains more than two cells. This shall prevent overflow of the local buffer if the indication is responded to within two cell slots.

Maskable interrupt status bits are generated upon the receipt of the first cell, upon detection of a CRC-32 error and upon a buffer overflow. If a buffer overflow occurs (this would indicate an operation failure due to the far-end device not respecting the UPCA bit status), entire cells are lost (the new incoming cells would be lost).

The format of received cell when it is read from the Microprocessor Cell Buffer Data register is shown in Fig. 11. Unused bytes have undefined value. The value of the bytes marked with an asterisk depends on the configuration of the corresponding LVDS link and the source of the cell. This is discussed further in the Operations section.

See Section 12.1.2 for details on the cell read protocol.

9.8 Internal Registers

The microprocessor interface provides access to normal and test mode registers. The normal mode registers are required for mission mode operation, and test mode registers are used to enhance the testability of the S/UNI-DUPLEX. The register set is accessed as follows:

9.9 Register Memory Map

Address	Register
0x00	Master Reset and Identity / Load Performance Meters
0x01	Master Configuration
0x02	Master Interrupt Status
0x03	Miscellaneous Interrupt Statuses
0x04	Clock Monitor
0x05	Serial Links Maintenance
0x06	Extended Address Match (LSB)
0x07	Extended Address Match (MSB)
0x08	Extended Address Mask (LSB)
0x09	Extended Address Mask (MSB)
0x0A	Output Address Match
0x0B	Configuration Pins Status

0x0C	SCI-PHY/Any-PHY Input Configuration 1
0x0D	SCI-PHY/Any-PHY Input Configuration 2
0x0E	SCI-PHY/Any-PHY Input Interrupt Enables
0x0F	SCI-PHY/Any-PHY Input Interrupt Status
0x10	Input Cell Available Enable (LSB)
0x11	Input Cell Available Enable (2nd)
0x12	Input Cell Available Enable (3rd)
0x13	Input Cell Available Enable (MSB)
0x14	SCI-PHY/Any-PHY Output Configuration
0x15	SCI-PHY/Any-PHY Output Polling Range
0X16 – 0x17	Reserved
0x18	RXD1 Bit Oriented Code Enable
0x19	RXD1 Bit Oriented Code Status
0x1A	RXD2 Bit Oriented Code Enable
0x1B	RXD2 Bit Oriented Code Status
0x1C	Reserved
0x1D	TXD1 Bit Oriented Code
0x1E	Reserved
0x1F	TXD2 Bit Oriented Code
0x20	Microprocessor Cell Buffer Interrupt
0x21	Microprocessor Insert FIFO Control
0x22	Microprocessor Extract FIFO Control
0x23	Microprocessor Insert FIFO Ready
0x24	Microprocessor Extract FIFO Ready
0x25	Insert CRC-32 Accumulator (LSB)
0x26	Insert CRC-32 Accumulator (2nd byte)
0x27	Insert CRC-32 Accumulator (3rd byte)
0x28	Insert CRC-32 Accumulator (MSB)
0x29	Extract CRC-32 Accumulator (LSB)
0x2A	Extract CRC-32 Accumulator (2nd byte)
0x2B	Extract CRC-32 Accumulator (3rd byte)
0x2C	Extract CRC-32 Accumulator (MSB)
0x2D	Microprocessor Cell Buffer Data
0x2E – 0x2F	Reserved
0x30	RXD1 Extract FIFO Control
0x31	RXD1 Extract FIFO Interrupt Status
0x32 – 0x33	Reserved
0x34	RXD2 Extract FIFO Control
0x35	RXD2 Extract FIFO Interrupt Status

0x36 – 0x3B	Reserved
0x3C	Receive Logical Channel FIFO Control
0x3D	Receive Logical Channel FIFO Interrupt Status
0x3E – 0x3F	Reserved
0x40	RXD1 High-Speed Serial Configuration
0x41	RXD1 High-Speed Serial Cell Filtering Configuration/Status
0x42	RXD1 High-Speed Serial Interrupt Enables
0x43	RXD1 High-Speed Serial Interrupt Status
0x44	RXD1 High-Speed Serial HCS Error Count
0x45	RXD1 High-Speed Serial Cell Counter (LSB)
0x46	RXD1 High-Speed Serial Cell Counter
0x47	RXD1 High-Speed Serial Cell Counter (MSB)
0x48 - 0x4F	Reserved
0x50	RXD2 High-Speed Serial Configuration
0x51	RXD2 High-Speed Serial Cell Filtering Configuration/Status
0x52	RXD2 High-Speed Serial Interrupt Enables
0x53	RXD2 High-Speed Serial Interrupt Status
0x54	RXD2 High-Speed Serial HCS Error Count
0x55	RXD2 High-Speed Serial Cell Counter (LSB)
0x56	RXD2 High-Speed Serial Cell Counter
0x57	RXD2 High-Speed Serial Cell Counter (MSB)
0x58 – 0x5B	Reserved
0x5C	Transmit Logical Channel FIFO Control
0x5D	Transmit Logical Channel FIFO Interrupt Status
0x5E	Transmit Logical Channel FIFO Depth
0x5F	Reserved
0x60	Transmit High-Speed Serial Configuration
0x61	Transmit High-Speed Serial Cell Count Status
0x62	Transmit High-Speed Serial Cell Counter (LSB)
0x63	Transmit High-Speed Serial Cell Counter
0x64	Transmit High-Speed Serial Cell Counter (MSB)
0x65 – 0x67	Reserved
0x68	Receive Serial Indirect Channel Select
0x69	Receive Serial Indirect Channel Configuration
0x6A	Receive Serial Indirect Channel Interrupt Enables
0x6B	Receive Serial Indirect Channel Interrupt and Status
0x6C	Receive Serial Indirect Channel HCS Error Count
0x6D	Receive Serial LCD Count Threshold

0x6E – 0x6F	Reserved
0x70	Transmit Serial Indirect Channel Select
0x71	Transmit Serial Indirect Channel Data
0x72 – 0x73	Reserved
0x74	Transmit Serial Alignment Control
0x75 – 0x7F	Reserved
0x80 – 0xFF	Reserved for test registers

For all register accesses, CSB must be low.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-DUPLEX. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[8]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-DUPLEX to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-DUPLEX operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-DUPLEX operates as intended, reserved register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

Register 0x00: Master Reset and Identity / Load Performance Meters

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	0
Bit 4	R	TYPE[0]	1
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

This register allows the revision number of the S/UNI-DUPLEX to be read by software permitting graceful migration to newer, feature-enhanced versions of the S/UNI-DUPLEX.

In addition, writing to this register simultaneously loads all the performance meter registers in the S/UNI-DUPLEX.

ID[3:0]:

The ID bits can be read to provide a binary S/UNI-DUPLEX revision number.

TYPE[2:0]:

The TYPE bits can be read to distinguish the S/UNI-DUPLEX from the other members of the S/UNI family of devices.

RESET:

The RESET bit allows the S/UNI-DUPLEX to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-DUPLEX is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-DUPLEX out of reset. Holding the S/UNI-DUPLEX in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Register 0x01: Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LTXCINV	0
Bit 4	R/W	LRXCINV	0
Bit 3	R/W	RESETO	0
Bit 2	R/W	MINTE	0
Bit 1	R/W	RXAUTOSEL	1
Bit 0	R/W	ACTIVE	0

ACTIVE:

The ACTIVE bit reports and allows the selection of the active high-speed serial link. If ACTIVE is logic 0, the cell data and RX8K timing reference are extracted from the RXD1+/- serial link. If ACTIVE is logic 1, the cell data and RX8K timing reference are extracted from the RXD2+/- serial link.

The value read reflects the link actually selected. It is either the value written if RXAUTOSEL is logic 0, or the selection based on the system prepend otherwise.

The active high-speed serial link can be determined automatically depending on the value of the RXAUTOSEL bit. If RXAUTOSEL is set to logic 0, the microprocessor selects the active high-speed link by writing to the ACTIVE bit. Writing to the ACTIVE bit has no effect if the RXAUTOSEL is logic 1.

RXAUTOSEL:

The RXAUTOSEL bit controls the automatic selection of the active high-speed serial link. If RXAUTOSEL is logic 1, the DUPLEX switches the active link based on the status information extracted from both links.
.

MINTE:

The Master Interrupt Enable allows internal interrupt statuses to be propagated to the interrupt output. If MINTE is logic 1, INTB will be asserted low upon the assertion of an interrupt status bit whose individual enable is set. If MINTE is logic 0, INTB is unconditionally high-impedance.

RESETO:

The RESETO bit controls the state of the RSTOB output. Setting RESETO to logic 1 causes the active low RSTOB output to be asserted. Setting RESETO to logic 0 causes the RSTOB output to go back to high impedance. RSTOB can also be controlled through bit oriented code received on the active high-speed link.

LRXCINV:

The LRXCINV bit determines the edge of the clock used to sample the LRXD[15:0] bus. When the LRXCINV bit is set to logic 1, each line of the LRXD[15:0] bus is sampled on the falling edge of the clock signal input on the corresponding LRXC[15:0] line. When the LRXCINV bit is set to logic 0, each line of the LRXD[15:0] bus is sampled on the rising edge of the clock signal input on the corresponding LRXC[15:0] line.

LTXCINV:

The LTXCINV bit determines the edge of the clock used to output the LTXD[15:0] bus. When the LTXCINV bit is set to logic 1, each line of the LTXD[15:0] bus is output on the falling edge of the clock signal input on the corresponding LTXC[15:0] line. When the LTXCINV bit is set to logic 0, each line of the LTXD[15:0] bus is output on the rising edge of the clock signal input on the corresponding LTXC[15:0] line.

Reserved:

These bits must be logic 0 for correct operation.

Register 0x02: Master Interrupt Status

Bit	Type	Function	Default
Bit 7	R	UPCIFI	X
Bit 6	R	OCIF	X
Bit 5	R	ICIF	X
Bit 4	R	TFI	X
Bit 3	R	RFI	X
Bit 2	R	TXI	X
Bit 1	R	RX2I	X
Bit 0	R	RX1I	X

RX1I, RX2I:

This register indicates whether there is a pending interrupt for a particular high-speed serial link receiver. RX1I is associated with RXD1+/-. and RX2I is associated with RXD2+/-. If RX1I or RX2I is logic 1, at least one interrupt status bit within the RXD1 or RXD2 High-Speed Serial Interrupt Status register that has its corresponding enable set is a logic 1.
These bits are not self-clearing; they are only cleared to logic 0 by reading the RXD1 or RXD2 High-Speed Serial Interrupt Status register.

TXI:

This register indicates whether there is a pending interrupt for the high-speed serial link transmitter. If TXI is logic 1, the interrupt status bit in the Transmit High-Speed Serial Cell Count Status register has its corresponding enable set and is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the Transmit High-Speed Serial Cell Count Status register.

RFI:

This register indicates whether there is a pending interrupt for the Receive Logical Channel FIFO. IF RFI is logic 1, the interrupt status bit in the Receive Logical Channel FIFO Interrupt Status register has its corresponding enable set and is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the Receive Logical Channel FIFO Interrupt register.

TFI:

This register indicates whether there is a pending interrupt for the Transmit Logical Channel FIFO. If TFI is logic 1, the interrupt status bit in the Transmit Logical Channel FIFO Interrupt Status register has its corresponding enable set and is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the Transmit Logical Channel FIFO Interrupt Status register.

ICIFI

This register indicates whether there is a pending interrupt for the SCI-PHY/Any-PHY interface input port. If ICIFI is logic 1, at least one interrupt status bit within the SCI-PHY/Any-PHY Input Interrupt Status register that has its corresponding enable set is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the SCI-PHY/Any-PHY Input Interrupt Status register.

OCIFI

This register indicates whether there is a pending interrupt for the SCI-PHY/Any-PHY Interface output port. If OCIFI is logic 1, at least one interrupt status bit within the SCI-PHY/Any-PHY Output Configuration and Interrupt Status register that has its corresponding enable set is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the SCI-PHY/Any-PHY Output Configuration and Interrupt Status register

UPCIFI:

This bit indicates whether there is a pending interrupt for the Microprocessor Cell Interface. If UPCIFI is logic 1, at least one interrupt status bit within the Microprocessor Cell Buffer Interrupt register that has its corresponding enable set is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the Microprocessor Cell Buffer Interrupt register.

Register 0x03: Miscellaneous Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	UPFI	X
Bit 2	R	RCSDI	X
Bit 1	R	RBOCI	X
Bit 0	R	ROOLI	X

ROOLI:

The Reference Out of Lock interrupt (ROOLI) status is a logic 1 if the ROOLV bit of the Clock Monitor register has changed state since the last time this register was read. The ROOLI bit is reset when this register is read.

RBOCI

This bit indicates whether there is a pending interrupt for the RXD1, RXD2 Bit Oriented Code Status registers. If RBOCI is logic 1, at least one interrupt status bit within the RXD1 Receive Bit Oriented Code Status register or the RXD2 Bit Oriented Code Status register that has its corresponding enable set is a logic 1.

RCSDI:

This register indicates whether there is a pending interrupt for the receive Clocked Serial Data Interface. If RCSDI is logic 1, at least one interrupt status bit within one of the Receive Serial Indirect Channel Interrupt and Status register that has its corresponding enable set is a logic 1.

This bit is cleared upon a read of this register.

UPFI:

This bit indicates whether there is a pending interrupt for one of the Microprocessor Extract FIFOs. If UPFI is logic 1, at least one interrupt status bit within the Microprocessor RXD1 FIFO Interrupt Status register or Microprocessor RXD2 FIFO Interrupt Status register that has its corresponding enable set is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the RXD1 Extract FIFO Interrupt Status register or the Microprocessor RXD2 Extract FIFO Interrupt Status register.

Register 0x04: Clock Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ROOLE	0
Bit 3	R	ROOLV	X
Bit 2	R	REFCLKA	X
Bit 1	R	OFCLKA	X
Bit 0	R	IFCLKA	X

This register provides activity monitoring of the S/UNI-DUPLEX clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

The register also reports the state of the clock synthesis unit that generates the internal clocks.

IFCLKA:

The IFCLK active (IFCLKA) bit monitors for low to high transitions on the IFCLK SCI-PHY/Any-PHY interface clock input. IFCLKA is set high on a rising edge of IFCLK, and is set low when this register is read. When the Clocked Serial Data interface is used (SCIANY input tied to logic 0), the IFCLKA bit monitors the internally generated CSDCLK. This clock is generated by dividing the high-speed serial link clock by 6.

OFCLKA:

The OFCLK active (OFCLKA) bit monitors for low to high transitions on the OFCLK SCI-PHY/Any-PHY interface clock input. OFCLKA is set high on a rising edge of OFCLK, and is set low when this register is read. When the Clocked Serial Data interface is used (SCIANY input tied to logic 0), the IFCLKA bit monitors the internally generated CSDCLK. This clock is generated by dividing the high-speed serial link clock by 6.

REFCLKA:

The REFCLK active (REFCLKA) bit monitors for low to high transitions on the REFCLK reference clock input. REFCLKA is set high on a rising edge of REFCLK, and is set low when this register is read.

ROOLV:

The reference out of lock status indicates the clock synthesis phase locked loop is unable to lock to the reference on REFCLK. ROOLV is a logic one if the synthesized clock frequency is not within 488 ppm of eight times the REFCLK frequency.

ROOLE:

The ROOLE bit is an interrupt enable for the transmit reference out of lock status. When ROOLE and the Master Interrupt Enable bit of the Master Configuration register are set to logic one, the INTB output is asserted low when the ROOLV bit changes state.

Register 0x05: Serial Links Maintenance

Bit	Type	Function	Default
Bit 7	R/W	RDIDIS2	0
Bit 6	R/W	RDIDIS1	0
Bit 5	R/W	TXDIS2	0
Bit 4	R/W	TXDIS1	0
Bit 3	R/W	MLB2	0
Bit 2	R/W	MLB1	0
Bit 1	R/W	DLB2	0
Bit 0	R/W	DLB1	0

DLB1:

The Diagnostic Loopback 1 enable bit allows TXD1+/- data to replace RXD1+/- data. When DLB1 is logic 1, the receive circuitry for the serial link is timed off the internal transmit clock and the TXD1+/- data is multiplexed into RXD1+/- just after the clock recovery. Upstream data is effectively routed to the downstream datapath if the corresponding high-speed serial link is active.

DLB2:

The Diagnostic Loopback 2 enable bit allows TXD2+/- data to replace RXD2+/- data. When DLB2 is logic 1, the receive circuitry for the serial link is timed off the internal transmit clock and the TXD2+/- data is multiplexed into RXD2+/- just after the clock recovery. Upstream data is effectively routed to the downstream datapath if the corresponding high-speed serial link is active.

MLB1:

The Metallic Loopback 1 enable bit allows RXD1+/- data to be presented on TXD1+/-. When LLB is logic one, the sliced receive data replaces the transmit data at the high-speed transmitter.

Note that the loopback can also be activated remotely through inband bit oriented codes.

MLB2:

The Metallic Loopback 2 enable bit allows RXD1+/- data to be presented on TXD1+/-. When LLB is logic one, the sliced receive data replaces the transmit data at the high-speed transmitter.

Note that the loopback can also be activated remotely through inband bit oriented codes.

TXDIS1:

The Transmit Disable 1 bit disables the high-speed outputs. If TXDIS1 is logic one, the TXD1+/- outputs do not drive valid logic levels, but instead float. TXDIS does not affect the differential output impedance; it is always within the range specified in the D.C. Characteristics section..

TXDIS2:

The Transmit Disable 2 bit disables the high-speed outputs. If TXDIS2 is logic one, the TXD2+/- outputs do not drive valid logic levels, but instead float. TXDIS does not affect the differential output impedance; it is always within the range specified in the D.C. Characteristics section.

RDIDIS1:

The RDI Disable 1 bit disables the automatic transmission of a RDI codeword on TXD1+/-. If RDIDIS1 is logic zero, the declaration of LOS or LCD results in the RDI codeword being transmitted in the BOC bit position .

Note that RDI can be sent manually by writing all zeros to the TXD1 Transmit Bit Oriented Code register.

RDIDIS2:

The RDI Disable 2 bit disables the automatic transmission of a RDI codeword on TXD2+/-. If RDIDIS2 is logic zero, the declaration of LOS or LCD results in the RDI codeword being transmitted in the BOC bit position .

Note that RDI can be sent manually by writing all zeros to the TXD2 Transmit Bit Oriented Code register.

Register 0x06: Extended Address Match (LSB)

Bit	Type	Function	Default
Bit 7	R/W	XAD[7]	0
Bit 6	R/W	XAD[6]	0
Bit 5	R/W	XAD[5]	0
Bit 4	R/W	XAD[4]	0
Bit 3	R/W	XAD[3]	0
Bit 2	R/W	XAD[2]	0
Bit 1	R/W	XAD[1]	0
Bit 0	R/W	XAD[0]	0

XAD[7:0]

This register in conjunction with the XAD[10:8]bits of the Extended Address Match (MSB) register is used in the selection of the SCI-PHY/Any-PHY input port for cell transfer when operating in Any-PHY bus slave mode (ANYPHY input set to logic 1, IMASTER input set to logic 0). Cells are accepted if the value in the Extended Address field of the prepend is equal with the XAD[10:0] bits over the range of bits specified by the Extended Address Mask registers.

When operating the SCI-PHY/Any-PHY output port in bus slave (OMASTER input set to logic 0), the XAD[2:0] bits are inserted in the three most significant bits of the Extended Address field of the prepend in the eight bit format and the XAD[11:0] bits are inserted in the 11 most significant bits of the Extended Address field of the prepend in 16 bit format.

Register 0x07: Extended Address Match (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	XAD[10]	0
Bit 1	R/W	XAD[9]	0
Bit 0	R/W	XAD[8]	0

XAD[10:8]]

These are the three most significant bits of the Extended Address Match.

Register 0x08: Extended Address Mask (LSB)

Bit	Type	Function	Default
Bit 7	R/W	XAM[7]	0
Bit 6	R/W	XAM[6]	0
Bit 5	R/W	XAM[5]	0
Bit 4	R/W	XAM[4]	0
Bit 3	R/W	XAM[3]	0
Bit 2	R/W	XAM[2]	0
Bit 1	R/W	XAM[1]	0
Bit 0	R/W	XAM[0]	0

XAM[7:0]

The XAM[7:0] bits are used in conjunction with the XAM[10:8] bits of the Extended Address Mask (MSB) register to mask bits of the Extended Address Match registers when comparing it with the Extended Address field of the prepend. When a bit of XAM[10:0] is set to logic 0, the corresponding bit of the Extended Address Match registers is masked in the comparison process. i.e. a match occurs independently of the Extended Address Match bit value.

Register 0x09: Extended Address Mask (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	XAM[10]	0
Bit 1	R/W	XAM[9]	0
Bit 0	R/W	XAM[8]	0

XAM[10:8]]

These are the three most significant bits of the Extended Address Match.

Register 0x0A: Output Address Match

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	OCAEN	0
Bit 4	R/W	OAD[4]	0
Bit 3	R/W	OAD[3]	0
Bit 2	R/W	OAD[2]	0
Bit 1	R/W	OAD[1]	0
Bit 0	R/W	OAD[0]	0

OAD[4:0]

The OAD[4:0] bits are used in the selection of the output port of the SCI-PHY/Any-PHY interface for polling and cell transfer. Polling occurs when the OAVALID input is sampled high and the sampled OADDR[4:0] inputs match the OAD[4:0] bits. A transfer is enacted if the value of the OADDR[4:0] inputs equals the OAD[4:0] bits when OENB is last sampled high.

OCAEN:

The OCAEN bit controls whether the OCA output is driven in response to polling when the SCI-PHY/Any-PHY interface output port is operated in bus slave mode (OMASTER set to logic 0). If OCAEN is set to logic 0, the OCA output pin stays unconditionally high impedance. If OCAEN is set to logic 1, OCA drives upon sampling a logic 1 on OAVALID while OADDR[4:0] value is equal to OAD[4:0] bits of this register. OCAEN should only be set to logic 1 after the aforementioned register bits have been initialized.

Register 0x0B: Configuration Pins Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	SCIANYV	X
Bit 5	R	OBUS8V	X
Bit 4	R	OANYPHYV	X
Bit 3	R	OMASTERV	X
Bit 2	R	IBUS8V	X
Bit 1	R	IANYPHYV	X
Bit 0	R	IMASTERV	X

The Configuration Pins Status Register reflects the value of the S/UNI-DUPLEX input pins used to configure the Clocked Serial Data and the SCI-PHY/Any-PHY interfaces. The IMASTERV, IANYPHYV, IBUS8V, OMASTERV, OANYPHYV, OBUS8V values are only meaningful when the SCIANY pin is high.

IMASTERV:

When IMASTERV is high, the SCI-PHY/Any-PHY interface input port is configured as a bus master. When IMASTERV is low the, input port is configured as a bus slave.

IANYPHYV:

When IANYPHYV is high, the SCI-PHY/Any-PHY interface input port complies with the Any-PHY protocol. When IANYPHYV is low the, input port complies with the SCI-PHY/Utopia protocol.

IBUS8V:

When IBUS8V is high, the SCI-PHY/Any-PHY interface input port is eight bit wide. When IBUS8V is low, the SCI-PHY/Any-PHY interface input port is sixteen bit wide.

OMASTERV:

When OMASTERV is high, the SCI-PHY/Any-PHY interface output port is configured as a bus master. When OMASTERV is low the, input port is configured as a bus slave.

OANYPHYV:

When OANYPHYV is high, the SCI-PHY/Any-PHY interface output port complies to the Any-PHY protocol. When OANYPHYV is low the, output port complies to the SCI-PHY/Utopia protocol.

OBUS8V:

When OBUS8V is high, the SCI-PHY/Any-PHY interface output port is eight bit wide. When OBUS8V is low, the SCI-PHY/Any-PHY interface output port is sixteen bit wide.

SCIANYV:

When SCIANYV is high, the SCI-PHY/Any-PHY interface is used to exchange cells with the DUPLEX. When SCIANYV is low, the Clocked Serial Data interface is used to exchange cells with the DUPLEX.

Register 0x0C: SCI-PHY/Any-PHY Input Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	H5UDF	1
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	PRELEN[1]	0
Bit 2	R/W	PRELEN[0]	0
Bit 1		Unused	X
Bit 0	R/W	PTYP	0

PTYP:

The Parity Type (PTYP) bit selects even or odd parity for the IPRTY input of the SCI-PHY/Any-PHY input port. When set to logic 1, IPRTY is the even parity bit for IDAT[15:0] if IBUS8 input is low or for IDAT[7:0] if IBUS8 input is high. When set to logic 0, IPRTY is the odd parity bit for IDAT[15:0] if IBUS8 input is low or for IDAT[7:0] if IBUS8 input is high.

PRELEN[1:0]:

The Prepend Length (PRELEN[1:0]) bits determine the number of words prepended to each cell received on the SCI-PHY/Any-PHY input port.

When IBUS8 is a logic 1, the binary PRELEN[1:0] value indicates whether the optional “Word 1” and “Word 2” illustrated in Fig. 6 are included in the data structure expected on IDAT[7:0]. The possible values are:

PRELEN[1:0]	Description
00	no prepended word
01	“Word 1” only is included
10	“Word 1:” and “Word 2” are included

When IBUS8 is a logic 0, only PRELEN[0] is used. When PRELEN[0] is logic 1, the optional “Word 1” illustrated in Fig. 7 is included in the data structure expected on IDAT[15:0].

Reserved:

This bit must be logic 0 for correct operation.

H5UDF:

The H5UDF bit determines whether or not the H5/UDF octets are included in cells transferred over the SCI-PHY/Any-PHY input port. When H5UDF is set to logic 1 (default), the H5 and UDF octets are included, i.e. the optional "Word 4" illustrated in Fig. 6 and Fig. 7 is included in the 8-bit or 16-bit data structure expected on IDAT[15:0].

Register 0x0D: SCI-PHY/Any-PHY Input Configuration 2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	ENFLTR	0
Bit 5	R/W	NNI	1
Bit 4	R/W	PHYDEV[4]	0
Bit 3	R/W	PHYDEV[3]	0
Bit 2	R/W	PHYDEV[2]	0
Bit 1	R/W	PHYDEV[1]	0
Bit 0	R/W	PHYDEV[0]	0

PHYDEV[4:0]:

The PHYDEV[4:0] bits are used to define the polling range of the SCI-PHY/Any-PHY input port when configured as a bus master (IMASTER is set to logic 1) The number of PHY devices to be polled is configured as follows:

PHYDEV[4:0]	Description
00000	Poll all 32 devices
00001	Poll PHY#1 thru PHY#2
00010	Poll PHY#1 thru PHY#3
00011	Poll PHY#1 thru PHY#4
:	:
11110	Poll PHY#1 thru PHY#31
11111	Poll all 32 PHY devices

Setting PHYDEV[4:0] to poll more PHY devices than actually connected to the SCI-PHY/Any-PHY input port may result in loss of cell throughput due to longer than necessary polling cycles.

NNI:

The NNI bit selects whether the UNI or NNI cell header format is used when determining whether a cell is unassigned or reserved for the Physical Layer. When set to logic 1 (default), the NNI format is used. When set to logic 0, the UNI format is used, i.e. the 4 most significant bits of Byte 1 of the cell header are ignored.

ENFLTR:

The ENFLTR bit controls the transfer of Physical Layer and unassigned cells over the SCI-PHY/Any-PHY input port. If ENFLTR is set logic 1, Physical Layer and unassigned cells are removed from the cells transferred over the SCI-PHY/Any-PHY input port. If ENFLTR is set logic 0, all cells, including Physical Layer and unassigned cells are transferred over the SCI-PHY/Any-PHY input port.

Register 0x0E: SCI-PHY/Any-PHY Input Interrupt Enables

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	PHYCELLE	0
Bit 1	R/W	CELLXFERRE	0
Bit 0	R/W	PARERRE	0

The Master Interrupt Enable bit of the Master Configuration register must also be logic 1 for these enables to take effect.

PHYCELLE:

The PHYCELLE bit enables the generation of an interrupt when a physical layer cell is transferred over the SCI-PHY/Any-PHY input port. When PHYCELLE is set to logic 1, the interrupt is enabled. Physical layer cells are defined in the I.361 standard as IDLE, unassigned and reserved cells (i.e. cells with a VPI = 0 and VCI = 0). These cells should be filtered out by the PHY device and would not normally be sent to the S/UNI-DUPLEX.

CELLXFERRE:

The CELLXFERRE bit enables the generation of an interrupt upon an invalid start of cell sequence. When CELLXFERRE is set to logic 1, the interrupt is enabled.

PARERRE:

The PARRERRE bit enables the generation of an interrupt on an input cell parity error. When PARRERE is set to logic 1, the interrupt is enabled.

Register 0x0F: SCI-PHY/Any-PHY Input Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	PHYCELLI	0
Bit 1	R	CELLXFERRI	0
Bit 0	R	PARERRI	0

PHYCELLI:

The PHYCELLI bit is set to logic 1 when a physical cell is transferred over the SCI-PHY/Any-PHY input port. This bit is reset immediately after a read to this register.

CELLXFERRI:

The CELLXFERRI bit is set to logic 1 when an invalid start of cell sequence is detected, i.e. ISOC or ISX is asserted when not expected at the SCI-PHY/Any-PHY input port. This bit is reset immediately after a read to this register.

The same event that asserts this bit may also result in a corrupted cell being transmitted on a high-speed serial link.

PARERRI:

The PARERRI bit is set to logic 1 when a parity error occurs while receiving a cell at the SCI-PHY/Any-PHY input port. This bit is reset immediately after a read to this register.

Register 0x10: Input Cell Available Enable (LSB)

Bit	Type	Function	Default
Bit 7	R/W	ICAEN[7]	1
Bit 6	R/W	ICAEN[6]	1
Bit 5	R/W	ICAEN[5]	1
Bit 4	R/W	ICAEN[4]	1
Bit 3	R/W	ICAEN[3]	1
Bit 2	R/W	ICAEN[2]	1
Bit 1	R/W	ICAEN[1]	1
Bit 0	R/W	ICAEN[0]	1

Register 0x11: Input Cell Available Enable (2nd)

Bit	Type	Function	Default
Bit 7	R/W	ICAEN[15]	1
Bit 6	R/W	ICAEN[14]	1
Bit 5	R/W	ICAEN[13]	1
Bit 4	R/W	ICAEN[12]	1
Bit 3	R/W	ICAEN[11]	1
Bit 2	R/W	ICAEN[10]	1
Bit 1	R/W	ICAEN[9]	1
Bit 0	R/W	ICAEN[8]	1

Register 0x12: Input Cell Available Enable (3rd)

Bit	Type	Function	Default
Bit 7	R/W	ICAEN[23]	1
Bit 6	R/W	ICAEN[22]	1
Bit 5	R/W	ICAEN[21]	1
Bit 4	R/W	ICAEN[20]	1
Bit 3	R/W	ICAEN[19]	1
Bit 2	R/W	ICAEN[18]	1
Bit 1	R/W	ICAEN[17]	1
Bit 0	R/W	ICAEN[16]	1

Register 0x13: Input Cell Available Enable (MSB)

Bit	Type	Function	Default
Bit 7	R/W	ICAEN[31]	1
Bit 6	R/W	ICAEN[30]	1
Bit 5	R/W	ICAEN[29]	1
Bit 4	R/W	ICAEN[28]	1
Bit 3	R/W	ICAEN[27]	1
Bit 2	R/W	ICAEN[26]	1
Bit 1	R/W	ICAEN[25]	1
Bit 0	R/W	ICAEN[24]	1

ICAEN[31:0]:

The four registers of ICAEN[31:0] control the polling of devices attached to the SCI-PHY/Any-PHY input port.
When operating in master mode (IMASTER input set to logic 1), the ICAEN[31:0] bits can be used to selectively remove a PHY device from the polling sequence. Setting a bit of ICAEN[31:0] to logic 0 prevents the S/UNI-DUPLEX to poll the corresponding device.

When operating in slave mode, the ICAEN[31:0] bits can be used to disable logical channels. Logical channels are disabled in group of four consecutive addresses, i.e. setting to logic 0 one or more bits of a four bit nibble of ICA[31:0] disables all four corresponding logical channels. If a disabled PHY

address is polled, ICA remains high impedance. Similarly, PHY selection is ignored and no cells are transferred to the S/UNI-DUPLEX when a disabled PHY is addressed. This is typically used to allow more than one slave device to share the cell input bus. Disabling all traffic to the SCIPHY/Any-PHY input port is achieved by setting all ICAEN[31:0] bits to logic 0.

Setting the Input Cell Available registers to other values than the default value may cause the device to behave erratically when the S/UNI-DUPLEX is configured for Clocked Serial Data interface (SCIANY input is low).

Register 0x14: SCI-PHY/Any-PHY Output Configuration

Bit	Type	Function	Default
Bit 7	R	CELLXFERRI	X
Bit 6	R/W	CELLXFERRE	0
Bit 5		Unused	X
Bit 4	R/W	INADDUDF	0
Bit 3	R/W	H5UDF	1
Bit 2	R/W	PRELEN[1]	0
Bit 1	R/W	PRELEN[0]	0
Bit 0	R/W	PTYP	0

PTYP:

The Parity Type (PTYP) bit selects even or odd parity for the OPRTY output of the SCI-PHY output port. When set to logic 1, OPRTY completes even parity bit for ODAT[15:0] if OBUS8 input is low or for ODAT[7:0] if OBUS8 input is high. When set to logic 0, OPRTY completes odd parity bits for ODAT[15:0] if OBUS8 input is low or for ODAT[7:0] if OBUS8 input is high.

PRELEN[1:0]:

The Prepend Length (PRELEN[1:0]) bits determine the number of prepended words to each cell

When OBUS8 is a logic 1, the binary PRELEN[1:0] value indicates whether the optional “Word 1” and “Word 2” illustrated in Fig. 6 are included in the data structure presented on ODAT[7:0]. The possible values are:

PRELEN[1:0]	Description
00	no prepended word
01	“Word 1” only is included
10	“Word 1:” and “Word2” are included

When OBUS8 is a logic 0, only PRELEN[0] is used. When PRELEN[0] is logic 1, the optional “Word 1” illustrated in Fig. 7 is included in the data structure presented on ODAT[15:0].

H5UDF:

The H5UDF bit determines whether or not the H5/UDF octets are included in cells transferred over the SCI-PHY/Any-PHY output port. When H5UDF is set

to logic 1 (default) and the eight bit SCI-PHY/Any-PHY cell format is used (OBUS8 input set to logic 1), the H5 byte is included, i.e. the optional “Word 7” illustrated in Fig. 6, in the data structure expected on ODAT[7:0]. When H5UDF is set to logic 1 (default) and the 16 bit SCI-PHY/Utopia/Any-PHY cell format is used (OBUS8 input set to logic 0), the H5 and UDF octets are included, i.e. the optional “Word 4” illustrated in Fig. 7, in the data structure expected on ODAT[15:0].

INADDUDF:

The INADDUDF bit relocates the word identifying the logical channel in the H5/UDF field when the output port is configured as a SCI-PHY/Utopia bus slave. When this bit is set to logic 1 and eight bit cell format is used (OBUS8 input set to logic 1), the logical channel is identified in the five lower bits of the H5 byte. The three upper bits of the H5 register are set to the value of the three least significant bits of the Extended Address Match register, which default to all zeros. When this bit is set to logic 1 and 16 bit cell format is used (OBUS8 input set to logic 0), the logical channel is identified in the five lower bits of the H5/UDF word. The eleven remainder bits of the H5/UDF word are set to the value of the Extended Address Match register, which default to all zeros. In both cases, “Word 0” is excluded from the cell data (refer to Fig. 6 and Fig. 7).

For proper operation to occur when INADDUDF is set to 1 the H5UDF bit must also be set to one (its default value). This bit has no effect when the SCI-PHY/Any-PHY Output port is not configured as a SCI-PHY/Utopia bus slave.

CELLXFERRE:

The Cell Transfer Error Interrupt Enable (CELLXFERRE) bit allows the generation of an interrupt on an invalid selection by an external master device. This occurs when a cell transfer is attempted, but the S/UNI-DUPLEX has indicated no cell is available by returning OCA low when polled. When CELLXFERRE is set to logic 1, the INTB output is asserted low when the CELLXFERRI bit is logic 1.

CELLXFERRI:

The CELLXFERRI bit provides a status of the Cell Transfer Error Interrupt. The CELLXFERRI is only valid when the SCI-PHY/Any-PHY Interface output port is configured as a bus slave (OMASTER=low). This interrupt status is asserted upon the selection by the external bus master of the SCI-PHY/Any-PHY Interface output port for a transfer without a cell being available, i.e. the S/UNI-DUPLEX has indicated no cell is available by returning OCA low when polled. The CELLXFERRI bit will not be asserted when the OENB is maintained low beyong the end of a cell transfer even if no new cell is

available. This bit is reset immediately after a read to this register.

Register 0x15: SCI-PHY/Any-PHY Output Polling Range

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PHYDEV[4]	0
Bit 3	R/W	PHYDEV[3]	0
Bit 2	R/W	PHYDEV[2]	0
Bit 1	R/W	PHYDEV[1]	0
Bit 0	R/W	PHYDEV[0]	0

PHYDEV[4:0]:

The PHYDEV[4:0] bits are used to define the polling range of the SCI-PHY/Any-PHY output port when configured as a bus master (OMASTER is set to logic 1). The number of PHY devices to be polled is configured as follows:

PHYDEV[4:0]	Description
00000	Poll all 32 devices
00001	Poll PHY#1 thru PHY#2
00010	Poll PHY#1 thru PHY#3
00011	Poll PHY#1 thru PHY#4
:	:
11110	Poll PHY#1 thru PHY#31
11111	Poll all 32 PHY devices

Setting PHYDEV[4:0] to poll more PHY devices than actually connected to the SCI-PHY/Any-PHY output port may result in loss of cell throughput due to longer than necessary polling cycles

Registers 0x18, 0x1A:
RXD1, RXD2 Bit Oriented Code Receiver Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	BOCE	0

These registers select the validation criteria to be used in determining a valid bit oriented code (BOC) and enables generation of an interrupt on a change in code status of the BOC received on RXD1+/- and RXD2+/-.

IDLE:

The IDLE bit enables the assertion of the INTB output when there is a transition from a validated BOC to idle code. When IDLE and the Master Interrupt Enable bit of the Master Configuration register are set to logic 1, the interrupt is enabled.

AVC:

The AVC bit position selects the validation criteria used in determining a valid BOC. A logic 1 in the AVC bit position selects an alternate validation criterion of 4 out of 5 matching BOCs; a logic 0 selects the 8 out of 10 matching BOC criterion. Unless fast declaration is necessary, it is recommended that AVC be set to logic 0 to improve bit error tolerance.

BOCE:

The BOCE bit enables the assertion of the INTB output when a valid BOC is detected. When BOCE and the Master Interrupt Enable bit of the Master Configuration register are set to logic 1, the interrupt is enabled.

Register 0x19, 0x1B:
RXD1, RXD2 Receive Bit Oriented Code Status

Bit	Type	Function	Default
Bit 7	R	IDLEI	X
Bit 6	R	BOCI	X
Bit 5	R	BOC[5]	X
Bit 4	R	BOC[4]	X
Bit 3	R	BOC[3]	X
Bit 2	R	BOC[2]	X
Bit 1	R	BOC[1]	X
Bit 0	R	BOC[0]	X

BOC[5:0]:

The BOC[5:0] bits indicate the current state value of the received bit-oriented code. The value is updated when the BOC has been a valid code 8 out of 10 or 4 out of 5 times, as selected by the AVC bit of the Bit Oriented Code Receiver Enable register. These bits are set to all ones (111111) if no valid code has been detected. An update is accompanied by a logic 1 in the BOCI bit.

IDLEI:

The IDLEI bit position indicates the detection of a transition from a valid BOC to idle or invalidated state code value of 111111. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle or invalid code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI will also set when no code is currently validated. Note that failure to meet the 8 of 10 (or 4 of 5) persistency criteria, either due to bit errors or a change to a new code, does result in IDLEI being set. IDLEI is cleared to logic 0 when the register is read.

BOCI:

The BOCI bit position indicates the detection of a valid BOC. BOCI becomes logic 1 when BOC[5:0] changes from the transition or IDLE code value of 111111. BOCI is cleared to logic 0 when the register is read.

BOCI will not be set at the transition to a validated IDLE code.

Registers 0x1D, 0x1F: TXD1, TXD2 Transmit Bit Oriented Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BC[5]	1
Bit 4	R/W	BC[4]	1
Bit 3	R/W	BC[3]	1
Bit 2	R/W	BC[2]	1
Bit 1	R/W	BC[1]	1
Bit 0	R/W	BC[0]	1

This register enables the generation of a bit oriented code and selects the 6-bit code to be transmitted in the BOC bit position of the corresponding TXD1+/-.or TXd2+/- high-speed serial link.

The contents of the register will be transmitted repeatedly in the BOC bit position of the corresponding TXD1+/- or TXD2+/- high-speed serial link with the format 111111110[BC0][BC1][BC2][BC3][BC4][BC5]0, provided a Remote Defect Indication (RDI) is not currently being transmitted. The default value represents an idle code.

Register 0x20: Microprocessor Cell Buffer Interrupt

Bit	Type	Function	Default
Bit 7	R	EXTCRCERRI	X
Bit 6	R	EXTRDYI	X
Bit 5	R	INSOVRI	X
Bit 4	R	INSRDYI	X
Bit 3	R/W	EXTCRCERRE	0
Bit 2	R/W	EXTRDYE	0
Bit 1	R/W	INSOVRE	0
Bit 0	R/W	INSRDYE	0

The Master Interrupt Enable bit of the Master Configuration register must also be logic 1 for the interrupt enables to take effect.

INSRDYE:

The INSRDYE bit allows the generation of an interrupt signal when the Insert FIFO becomes available. When INSRDYE is set to logic 1, the INTB output is asserted low when the INSRDYI bit is logic 1.

INSOVRE:

The INSOVRE bit controls the generation an interrupt signal when a write access is done to a full Insert FIFO. When INSOVRE is set to logic 1, the INTB output is asserted low when the INSOVRI bit is logic 1.

EXTRDYE:

The EXTRDYE bit allows the generation of an interrupt signal when an Extract FIFO becomes ready. When EXTRDYE is set to logic 1, the INTB output is asserted low when the EXTRDYI bit is logic 1.

EXTCRCERRE:

The EXTCRCERRE bit controls the generation an interrupt signal upon detection of a CRC-32 error at the end of a cell read access. When EXCRCERRE is set to logic 1, the INTB output is asserted low when the EXTCRCERRI bit is logic 1.

INSRDYI:

The INSRDYI bit provides the status of the Insert FIFO Ready Interrupt. This bit is set to logic 1 when the Insert FIFO becomes ready to accept a cell (i.e. a cell is transferred from a full FIFO) or upon the completion of a cell write if at least one more cell can be written. Ready status of a specific FIFO is indicated by a logic 1 at the corresponding bit of the Microprocessor Insert FIFO Ready register. The INSRDYI bit is reset immediately after a read to this register.

INSOVRI:

The INSOVRI bit indicates the status of the write access to the Insert FIFO. This bit is set to high when a write access has being done to a full Insert FIFO and that the data has been discarded. This bit is reset immediately after a read to this register.

EXTRDYI:

The EXTRDYI bit provides the status of the Extract FIFOs Ready Interrupt. This bit is set to logic 1 when one of the Extract FIFO becomes ready for a cell read (i.e. upon reception of the only cell in the FIFO) or upon the completion of a cell read if there is at least one more cell to be read from the FIFO. Ready status of a specific FIFO is indicated by a logic 1 at the corresponding bit of the Microprocessor Insert FIFO Ready register. This bit is reset immediately after a read to this register.

EXTCRCERRI:

The EXTCRCERRI bit indicates the CRC-32 status of a cell read from an Extract FIFO. When the EXTCRCCHK bit is set to logic 1, the EXTCRCERRI bit is updated when the last byte of a cell is read by the microprocessor. It is set to logic 1 if the value of the Extract CRC Accumulator register differs from the expected CRC-32 remainder polynomial. Otherwise, it is set to logic 0.

This bit is also reset immediately after a read to this register.

Register 0x21: Microprocessor Insert FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	INSCRCEND	0
Bit 4	R/W	INSCRCPR	1
Bit 3	W	INSRST	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

INSRST:

The INSRST bit allows the microprocessor to abort a cell write to the Insert FIFO. If INSRST is set to a logic 1 when previously logic 0, the extract pointer is reset without completing the transaction. Setting INSRST after the last write (i.e. at the beginning of the next cell) has no effect. To abort a cell, the microprocessor must have written at least the first byte of the cell but less than 56 bytes.

INSRST is not readable.

This bit is cleared on every write to Microprocessor Cell Data register.

INSCRCPR:

The INSCRCPR bit is used to force the value of the Insert CRC-32 accumulation register to its preset value. If INSCRCPR is set to logic 1, the Insert CRC-32 accumulation register is kept to its preset value. If INSCRCPR is set to logic 0, CRC-32 calculations are performed on inserted cells. CRC-32 calculations are performed on the cell payload bytes being written to the Microprocessor Cell Data register.

INSCRCEND:

The INSCRCEND bit is used to indicate that the following inserted cell is the last one of the CPCS-PDU. Setting this bit to logic 1 will cause the last four bytes of the cell transferred from the microprocessor to be replaced by the value of the ones complement of the Insert CRC-32 Accumulation register.

Register 0x22: Microprocessor Extract FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	EXTCRCCHK	0
Bit 4	R/W	EXTCRCPR	1
Bit 3	W	EXTABRT	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	EXTFSEL	0

EXTFSEL:

The EXTFSEL bit is used to select the one of Microprocessor Extract FIFOs for a cell read operation. A logic 0 in EXTFSEL selects the Extract FIFO associated with RXD1+/-. A logic 1 in EXTFSEL selects the Extract FIFO associated with RXD2+/-. The Extract FIFO has to be selected prior to starting the cell transfer. Due to synchronization delays, a read of the Microprocessor Cell Buffer Data register should not be initiated until two REFCLK periods after completion of the write of these bits.

EXTABRT:

The EXTABRT bit allows the microprocessor to discard a cell without reading the remaining contents. If EXTABRT is set to a logic 1 when previously logic 0, the extract pointer is reset, effectively discarding the remaining content of the cell. Setting EXTABRT after the last read (i.e. at the beginning of the next cell) has no effect. To abort a cell, the microprocessor must have read at least the first word of the cell but no more than 56 bytes.

Due to synchronization delays, no cell extraction operation should be initiated until two REFCLK periods after completion of the write of this bit.

EXTABRT is not readable.

It is cleared on every read from normal mode Microprocessor Cell Data register.

EXTCRCPR:

The EXTCRCPR bit is used to force the value of the Extract CRC-32 accumulation register to its preset value. If EXTCRCPR is set to logic 1, the Insert CRC-32 accumulation register is kept to its preset value. If EXTCRCPR is set to logic 0, CRC-32 verification is performed on extracted cells. The CRC-32 calculations are performed on the bytes being read from the location of the Microprocessor Cell Data register corresponding to the payload of extract cells.

Due to synchronization delays, a read of the Microprocessor Cell Buffer Data register should not be initiated until two REFCLK periods after completion of the write of this bit.

EXTCRCCHK:

The EXTCRCCHK bit is used to enable the CRC-32 field check. Setting this bit to logic 1 will cause the S/UNI-DUPLEX to verify if the value of the Extract CRC-32 Accumulation register is equal to the expected CRC-32 remainder polynomial at the end of a cell read access by the microprocessor. If EXTCRCCHK is logic 1, the EXTCRCERRI bit will be set to logic 1 if the CRC-32 value is incorrect.

Register 0x23: Microprocessor Insert FIFO Ready

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	INSRDY	X

INSRDY

The INSRDY bit provides the ready status of the Microprocessor Insert FIFO. A logic 1 in the INSRDY bit indicates that the Microprocessor Insert FIFO is ready to accept a cell.

Note that the INSRDY bit will always return a logic 0 if the FIFO is currently being written to.

Register 0x24: Microprocessor Extract FIFO Ready

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	EXTRDY[1]	X
Bit 0	R	EXTRDY[0]	X

EXTRDY[1:0]:

The EXTRDY[1:0] bits provide the ready status of the Extract FIFOs. A logic 1 in a EXTRDY[0] bit indicates that the Extract FIFO associated with RXD1+/- as at least one cell available for reading. A logic 1 in a EXTRDY[1] bit indicates that the Extract FIFO associated with RXD2+/- as at least one cell available for reading.

Note that the EXTRDY bit for the FIFO currently being read will always return a logic 0.

Register 0x25: Insert CRC-32 Accumulator (LSB)

Bit	Type	Function	Default
Bit 7	R/W	INSCRCACC[7]	1
Bit 6	R/W	INSCRCACC[6]	1
Bit 5	R/W	INSCRCACC[5]	1
Bit 4	R/W	INSCRCACC[4]	1
Bit 3	R/W	INSCRCACC[3]	1
Bit 2	R/W	INSCRCACC[2]	1
Bit 1	R/W	INSCRCACC[1]	1
Bit 0	R/W	INSCRCACC[0]	1

Register 0x26: Insert CRC-32 Accumulator (2nd)

Bit	Type	Function	Default
Bit 7	R/W	INSCRCACC[15]	1
Bit 6	R/W	INSCRCACC[14]	1
Bit 5	R/W	INSCRCACC[13]	1
Bit 4	R/W	INSCRCACC[12]	1
Bit 3	R/W	INSCRCACC[11]	1
Bit 2	R/W	INSCRCACC[10]	1
Bit 1	R/W	INSCRCACC[9]	1
Bit 0	R/W	INSCRCACC[8]	1

Register 0x27: Insert CRC-32 Accumulator (3rd)

Bit	Type	Function	Default
Bit 7	R/W	INSCRCACC[23]	1

Bit	Type	Function	Default
Bit 6	R/W	INSCRCACC[22]	1
Bit 5	R/W	INSCRCACC[21]	1
Bit 4	R/W	INSCRCACC[20]	1
Bit 3	R/W	INSCRCACC[19]	1
Bit 2	R/W	INSCRCACC[18]	1
Bit 1	R/W	INSCRCACC[17]	1
Bit 0	R/W	INSCRCACC[16]	1

Register 0x28: Insert CRC-32 Accumulator (MSB)

Bit	Type	Function	Default
Bit 7	R/W	INSCRCACC[31]	1
Bit 6	R/W	INSCRCACC[30]	1
Bit 5	R/W	INSCRCACC[29]	1
Bit 4	R/W	INSCRCACC[28]	1
Bit 3	R/W	INSCRCACC[27]	1
Bit 2	R/W	INSCRCACC[26]	1
Bit 1	R/W	INSCRCACC[25]	1
Bit 0	R/W	INSCRCACC[24]	1

INSCRCACC[31:0]:

The four registers of INSCRCACC[31:0] allow the microprocessor to read or write the contents of the Insert CRC Accumulator register. This register accumulates the CRC-32 value over the data being written to the Insert FIFO.

The rising edge of WRB for two successive write accesses to these registers must separated by at least three REFCLK periods.

Register 0x29: Extract CRC-32 Accumulator (LSB)

Bit	Type	Function	Default
Bit 7	R/W	EXTCRCACC[7]	1
Bit 6	R/W	EXTCRCACC[6]	1
Bit 5	R/W	EXTCRCACC[5]	1
Bit 4	R/W	EXTCRCACC[4]	1
Bit 3	R/W	EXTCRCACC[3]	1
Bit 2	R/W	EXTCRCACC[2]	1
Bit 1	R/W	EXTCRCACC[1]	1
Bit 0	R/W	EXTCRCACC[0]	1

Register 0x2A: Extract CRC-32 Accumulator (2nd)

Bit	Type	Function	Default
Bit 7	R/W	EXTCRCACC[15]	1
Bit 6	R/W	EXTCRCACC[14]	1
Bit 5	R/W	EXTCRCACC[13]	1
Bit 4	R/W	EXTCRCACC[12]	1
Bit 3	R/W	EXTCRCACC[11]	1
Bit 2	R/W	EXTCRCACC[10]	1
Bit 1	R/W	EXTCRCACC[9]	1
Bit 0	R/W	EXTCRCACC[8]	1

Register 0x2B: Extract CRC-32 Accumulator (3rd)

Bit	Type	Function	Default
Bit 7	R/W	EXTCRCACC[23]	1
Bit 6	R/W	EXTCRCACC[22]	1
Bit 5	R/W	EXTCRCACC[21]	1
Bit 4	R/W	EXTCRCACC[20]	1
Bit 3	R/W	EXTCRCACC[19]	1

Bit	Type	Function	Default
Bit 2	R/W	EXTCRCACC[18]	1
Bit 1	R/W	EXTCRCACC[17]	1
Bit 0	R/W	EXTCRCACC[16]	1

Register 0x2C: Extract CRC-32 Accumulator (MSB)

Bit	Type	Function	Default
Bit 7	R/W	EXTCRCACC[31]	1
Bit 6	R/W	EXTCRCACC[30]	1
Bit 5	R/W	EXTCRCACC[29]	1
Bit 4	R/W	EXTCRCACC[28]	1
Bit 3	R/W	EXTCRCACC[27]	1
Bit 2	R/W	EXTCRCACC[26]	1
Bit 1	R/W	EXTCRCACC[25]	1
Bit 0	R/W	EXTCRCACC[24]	1

EXTCRCACC[31:0]:

The four registers of EXTCRCACC[31:0] allows the microprocessor to read or write the content of the Extract CRC Accumulator register. The Extract CRC-32 Accumulator register accumulates the CRC-32 value of the data being from an Extract FIFO.

The rising edge of WRB for two successive write accesses to these registers must separated by at least three REFCLK periods.

Register 0x2D: Microprocessor Cell Data

Bit	Type	Function	Default
Bit 7	R/W	MCDAT[7]	X
Bit 6	R/W	MCDAT[6]	X
Bit 5	R/W	MCDAT[5]	X
Bit 4	R/W	MCDAT[4]	X
Bit 3	R/W	MCDAT[3]	X
Bit 2	R/W	MCDAT[2]	X
Bit 1	R/W	MCDAT[1]	X
Bit 0	R/W	MCDAT[0]	X

MCDAT[7:0]:

The MCDAT[7:0] is used to write to the Insert FIFO or read from the selected Extract FIFO by the microprocessor.

When inserting cells, the Insert FIFO Ready register may be polled to determine whether the FIFO is ready to receive a cell. Alternately, an interrupt may be generated by setting the Insert FIFO Interrupt Enable register bit accordingly. A cell is transferred to the Insert FIFO by performing successive write accesses to the Microprocessor Cell Data register. The rising edge of WRB for two successive write accesses to this register must separated by at least three REFCLK periods.

When extracting cells, the Extract FIFO Ready register may be polled to determine which FIFO has a cell available to be read. Alternately, an interrupt may be generated by setting the Extract FIFO Interrupt Enable register bit accordingly. Selection of the Extract FIFO is done by writing the EXTFSEL bit of the Extract FIFO Control register. A cell is transferred from an Extract FIFO by performing successive read accesses to the Microprocessor Cell Data register. The falling edge of RDB for two successive read accesses to this register must separated by at least three REFCLK periods.

Register 0x30: RXD1 Extract FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	UPF1OVRE	0
Bit 0	R/W	UPF1RST	0

UPF1RST:

The UPF1RST bit is used to reset the Microprocessor Cell Extract FIFO associated with RXD1+/-. When UPF1RST is set to logic 0, the FIFO operates normally. When UPF1RST is set to logic 1, all the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until logic 0 is written to UPF1RST.

UPF1OVRE:

The UPF1OVRE bit enables the assertion of the INTB output due to an overflow error condition of the Microprocessor Cell Extract FIFO associated with RXD1+/-. When UPF1OVRE is set to logic 1, the interrupt is enabled.

Register 0x31: RXD1 Extract FIFO Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	UPF1OVRI	0

UPF1OVRI:

The UPF1OVRI bit indicates an interrupt due to overflow error condition of the Microprocessor Cell Extract FIFO associated with RXD1+/-. Generally, the UPF1OVRI status bit should never be asserted; its assertion would indicate that the flow control protocol is being ignored. The UPF1OVRI bit is reset immediately after a read to this register.

Register 0x34: RXD2 Extract FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	UPF2OVRE	0
Bit 0	R/W	UPF2RST	0

UPF2RST:

The UPF2RST bit is used to reset the Microprocessor Cell Extract FIFO associated with RXD2+/-. When UPF2RST is set to logic 0, the FIFO operates normally. When UPF2RST is set to logic 1, all the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until logic 0 is written to UPF2RST.

UPF2OVRE:

The UPF2OVRE bit enables the assertion of the INTB output due to an overflow error condition of the Microprocessor Cell Extract FIFO associated with RXD2+/-. When UPF2OVRE is set to logic 1, the interrupt is enabled.

Register 0x35: RXD2 Extract FIFO Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	UPF2OVRI	0

UPF2OVRI:

The UPF2OVRI bit indicates an interrupt due to overflow error condition of the Microprocessor Extract FIFO associated with RXD1+/-. Generally, the UPF2OVRI status bit should never be asserted; its assertion would indicate that the flow control protocol is being ignored. The UPF2OVRI bit is reset immediately after a read to this register.

Register 0x3C: Receive Logical Channel FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	FOVRE	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset all logical channel FIFOs for the receive link. When FIFORST is set to logic 0, the FIFO channels operate normally. When FIFORST is set to logic 1, all the FIFOs are immediately emptied and ignore writes from the active LVDS link. While the FIFO is reset the flow control information sent to the far end (via the LVDS link) indicates “buffer full or unavailable” for all channels. The FIFOs remain empty and continue to ignore writes until logic 0 is written to FIFORST.

To prevent unstable behavior during cell format configuration, FIFORST should be left asserted while changing the cell format or length.

If a cell is being transferred from the SCIPHY/Any-PHY output port or from the Clocked Serial Data interface when a reset of the FIFO occurs the cell will be corrupted.

When using the SCI-PHY/Any-PHY output port as a bus slave, the bus master need not have started the cell transfer (in response to the asserted OCA from the S/UNI-DUPLEX) for cell corruption to occur. The S/UNI-DUPLEX uses a partial look ahead buffer that cannot be reset by the Receive Logical Channel FIFO reset. Even if the bus master suspends cell transfers during the time when the Receive Logical Channel FIFO is reset, the next cell read from the S/UNI-DUPLEX will be corrupted if there was a cell wainting for transfer when the FIFO reset occurred. The simplest approach is to allow the bus master to continue normal operation during a FIFO reset. If required, the bus master can discard any cells received from that link after it is reset.

FOVRE:

The FOVRE bit enables the assertion of the INTB output due to a FIFO overrun error condition. When FOVRE is set to logic 1, the interrupt is enabled.

Register 0x3D:Receive Logical Channel FIFO Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	FOVRI	X

FOVRI:

The FOVRI bit indicates an interrupt due to a logical channel FIFO over flow error condition. Generally, the FOVRI status bit should never be asserted; its assertion would indicate that the flow control protocol is being ignored. The FOVRI bit is reset immediately after a read to this register.

Registers 0x40, 0x50:
RXD1, RXD2 High-Speed Serial Configuration

Bit	Type	Function	Default
Bit 7	R/W	DDSCR	0
Bit 6	R/W	HDSCR	1
Bit 5		Unused	X
Bit 4	R/W	CNTCELLERR	0
Bit 3	R/W	CELLCRC	0
Bit 2	R/W	PREPEND	0
Bit 1	R/W	USRHDR[1]	1
Bit 0	R/W	USRHDR[0]	0

These registers configure, on a per-link basis, the format of the cells expected on RXD1 and RXD2 serial links.

USRHDR[1:0]:

The USRHDR[1:0] bits determine the length of the expected User Header field of the received cells, as illustrated in Fig. 9.

USRHDR[1:0]	Bytes in User Header
00	4
01	5
10	6
11	Reserved

PREPEND:

The PREPEND bit determines if the User Prepend field is expected to exist in the received cells. If PREPEND is logic 1, a two byte User Prepend is expected to follow the System Prepend field.

CELLCRC:

The CELLCRC bit determines whether the entire high-speed serial data structure is expected to be protected by a CRC-8 code word. The PREPEND

bit must be logic 1 for this bit to have effect. If CELLCRC and PREPEND are logic 1, the second User Prepend byte is expected to contain the CRC-8 syndrome for the preceding cell. A non-zero remainder shall result in a maskable interrupt and, if enabled by the CNTCELLERR bit, a cell error count increment. If CELLCRC is logic 0, the contents of the second User Prepend byte are not examined.

CNTCELLERR:

The CNTCELLERR bit allows the redefinition of the Receive High-Speed Serial HCS Error Count register to include the number of cell CRC-8 errors. If CNTCELLERR, CELLCRC and PREPEND are logic 1, each non-zero remainder for the CRC-8 protecting the entire cell or non-zero remainder HCS results in an increment. (Simultaneous cell CRC-8 and HCS errors result in a single increment.) If CNTCELLERR, CELLCRC, and PREPEND are logic 0, the count represents the number of HCS errors.

DDSCR and HDSCR:

The Disable Descramble (DDSCR) and Header Descramble enable (HDSCR) bits control the descrambling of the cell by the $x^{43} + 1$ self-synchronous descrambler. When DDSCR is a logic one, cell header and payload descrambling is disabled. When DDSCR is a logic zero, payload descrambling is enabled and cell header descrambling is determined by HDSCR. HDSCR enables descrambling of the System Prepend, User Prepend, User Header, and HCS byte collectively. The operation of the DDSCR and HDSCR bits is summarized below:

DDSCR	HDSCR	Operation
1	X	Cell payload and header descrambling is disabled. THIS CONFIGURATION SHOULD ONLY BE USED FOR DIAGNOSTIC PURPOSES.
0	0	Cell payload is descrambled. Cell header is left unscrambled. THIS CONFIGURATION SHOULD ONLY BE USED FOR DIAGNOSTIC PURPOSES.
0	1	Cell payload and header are both descrambled.

Registers 0x41, 0x51:
RXD1, RXD2 High-Speed Serial Cell Filtering Configuration/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	HCSPASS	0
Bit 5	R/W	Reserved	0
Bit 4	R	OCDV	X
Bit 3		Unused	X
Bit 2	R	ACTV	X
Bit 1	R	LCDV	X
Bit 0	R	LOSV	X

These registers provide the status of each individual RXD1+/- and RXD2+/- serial link.

LOSV:

The LOSV gives the Loss of Signal state. LOSV becomes logic 1 upon 2048 bit periods (13.2 μs at 155.52 Mb/s) without a signal transition in the received data (i.e. before descrambling, if enabled). LOSV becomes logic 0 when a signal transition has occurred in each of 16 consecutive non-overlapping intervals of 16 bit periods each.

LCDV:

The LCDV bit gives the Loss of Cell Delineation state. When LCDV is logic 1, an out of cell delineation (OCD) defect has persisted for 1318 cells. LCDV becomes logic 0 when cell delineation has been maintained for 1318 cells. LCDV is logic 1 out of reset.

ACTV:

The ACTV bit provides the debounced state of the ACTIVE bit in the cell prepend. ACTV reflects the state of the ACTIVE bit when it has been the same for three consecutive valid cells.

OCDV:

The OCDV bit indicates the cell delineation state. When OCDV is logic 1, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries. When OCDV is logic 0, the cell delineation

state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Reserved:

This bit must be logic 0 for correct operation.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of a HCS error. When HCSPASS is logic 0, cells containing a HCS error are dropped. When HCSPASS is logic 1, non-stuff cells are passed to the FIFO interface regardless of errors detected in the HCS. Stuff cells continue to be dropped and HCS errors continue to be counted by the performance monitor registers. Additionally, the HCS verification finite state machine never exits the ‘SYNC’ state, and hence will never lose cell delineation. This bit is provided for diagnostic purposes only.

Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states.

Registers 0x42, 0x52:
RXD1, RXD2 High-Speed Serial Interrupt Enables

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	HCSE	0
Bit 5	R/W	XFERE	0
Bit 4	R/W	OCDE	0
Bit 3	R/W	CELLERRE	0
Bit 2	R/W	ACTE	0
Bit 1	R/W	LCDE	0
Bit 0	R/W	LOSE	0

These registers allow changes in the corresponding RXD1 High-Speed Serial Cell Filtering Configuration/Status and RXD2 High-Speed Serial Cell Filtering Configuration/Status register bits, HCS errors and counter transfers to cause assertion low the INTB output.

The Master Interrupt Enable bit of the Master Configuration register must also be logic 1 for the interrupt enables to take effect.

LOSE:

The LOSE bit enables the generation of an interrupt upon a change in the Loss of Signal state. When LOSE is set to logic 1, the INTB output is asserted low when the LOSI bit is logic 1.

LCDE:

The LCDE bit enables the generation of an interrupt due to a change in the LCD (Loss of Cell Delineation) state. When LCDE is set to logic 1, the INTB output is asserted low when the LCDI bit is logic 1.

ACTE:

The ACTE bit enables the generation of an interrupt due to a change in the ACTV register bit. When ACTE is set to logic 1, the INTB output is asserted low when the ACTI bit is logic 1.

CELLERRE:

The CELLERRE bit enables the generation of an interrupt due to a non-zero remainder of the CRC-8 protecting the entire cell while in the SYNC cell

delineation state. When CELLERRE , CELLCRC, and PREPEND are set to logic 1, the interrupt is enabled.

OCDE:

The OCDE bit enables the generation of an interrupt due to a change in cell delineation state. When OCDE is set to logic 1, the INTB output is asserted low when the OCDI bit is logic 1.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a HCS error while in the SYNC cell delineation state. When HCSE is set to logic 1, the INTB output is asserted low when the HCSI bit is logic 1.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive cell counter and HCS error counter holding registers. When XFERE is set to logic 1, the INTB output is asserted low when the XFERI bit is logic 1.

Registers 0x43,0x53:
RXD1, RXD2 High-Speed Serial Interrupt Status

Bit	Type	Function	Default
Bit 7	R	OVR	X
Bit 6	R	XFERI	X
Bit 5	R	HCSI	X
Bit 4	R	OCDI	X
Bit 3	R	CELLERRI	X
Bit 2	R	ACTI	X
Bit 1	R	LCDI	X
Bit 0	R	LOSI	X

These registers provide an indication of events that have occurred since the last time they were read. These bits are not affected by the programming of the RXD1 and RXD2 High-Speed Serial Interrupt Enables registers, which only determines whether the status of the bits in these registers is propagated to the INTB output.

LOSI:

The LOSI bit is set to logic 1 whenever the associated LOSV register bit changes state. This bit is reset immediately after a read to this register.

LCDI:

The LCDI bit is set to logic 1 whenever the associated LCDV register bit changes state. This bit is reset immediately after a read to this register.

ACTI:

The ACTI bit is set to logic 1 whenever the associated ACTV register bit changes state. This bit is reset immediately after a read to this register.

CELLERRI:

The CELLERRI bit is set high when a non-zero remainder occurs for the CRC-8 protecting the entire cell. This bit is reset immediately after a read to this register.

HCSI:

The HCSI bit is set high when a HCS error is detected. This bit is reset immediately after a read to this register.

XFERI:

The XFERI bit indicates that a transfer of accumulated counter data has occurred. A logic 1 in this bit position indicates that the receive cell counter and error counter holding registers have been updated. This update is initiated by writing to the associated (i.e. this link only) Receive High-Speed Serial HCS Error Count register, one of the associated Receive High-Speed Serial Cell Counter registers or the Load Performance Meters (0x000) register. This bit is reset immediately after a read to this register.

OCDI:

The OCDI bit is set high when the cell delineation state machine enters or exits the SYNC state. The current value of the OCD state is available in the OCDV bit in the associated Receive High-Speed Serial Cell Filtering Configuration/Status register. The OCDI bit is reset immediately after a read to this register.

OVR:

The OVR bit is the overrun status of the associated accumulation holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred, and that the contents of the receive cell counter and HCS error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Registers 0x44, 0x54:
RXD1, RXD2 High-Speed Serial HCS Error Count

Bit	Type	Function	Default
Bit 7	R	HCSERR[7]	X
Bit 6	R	HCSERR[6]	X
Bit 5	R	HCSERR[5]	X
Bit 4	R	HCSERR[4]	X
Bit 3	R	HCSERR[3]	X
Bit 2	R	HCSERR[2]	X
Bit 1	R	HCSERR[1]	X
Bit 0	R	HCSERR[0]	X

HCSERR[7:0]:

If any of the CELLCRC, CNTCELLERR, and PREPEND bits of the Receive High-Speed Serial Configuration register is logic 0, the HCSERR[7:0] bits indicate the number of HCS error events while in the SYNC cell delineation state that occurred during the last accumulation interval on the associated RXD1+/- or RXD2+/-link.

If the CELLCRC, CNTCELLERR, and PREPEND bits are logic 1, the HCSERR[7:0] bits indicate the number of cells with non-zero cell CRC-8 or HCS remainders while in the SYNC cell delineation state. (Simultaneous non-zero cell CRC-8 and HCS remainders result in a single increment).s.

The contents of this register become valid a maximum of 300 ns after a transfer is triggered by a write to this register, one of the associated (i.e. this link only) Receive High-Speed Serial Cell Counter registers or the Load Performance Meters (0x00) register, and remain valid until another transfer is triggered.

The count saturates at all ones.

Registers 0x45, 0x55:
RXD1, RXD2 High-Speed Serial Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Registers 0x46, 0x56:
RXD1, RXD2 High-Speed Serial Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Registers 0x47, 0x57:
RXD1, RXD2 High-Speed Serial Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[23]	X
Bit 6	R	RCELL[22]	X
Bit 5	R	RCELL[21]	X
Bit 4	R	RCELL[20]	X
Bit 3	R	RCELL[19]	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[23:0]:

The RCELL[23:0] bits indicate the number of valid cells received during the last accumulation interval. Cells filtered due to HCS errors or as stuff cells are not counted. No cells are transferred when the cell delineation state machine is in either the HUNT or PRESYNC state. Cells lost due to FIFO overflows are excluded from the count. The counter should be polled at least every 30 seconds to avoid saturation.

The contents of these registers become valid a maximum of 300 ns after a transfer is triggered by a write to these registers, the associated Receive High-Speed Serial HCS Error Count register or the Load Performance Meters (0x00) register, and remain valid until another transfer is triggered.

The count saturates at all ones.

Register 0x5C: Transmit Logical Channel FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	FOVRE	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset all the logical channels of the Transmit Logical Channel FIFO. When FIFORST is set to logic 0, the FIFO channels operate normally. When FIFORST is set to logic 1, all the FIFOs are immediately emptied and ignore writes. The FIFOs remain empty and continue to ignore writes until logic 0 is written to FIFORST. This results in a continuous stream of stuff cells on TXD1+/- and TXD2+/-.

If a user cell is currently being sent over the LVDS link it will likely be corrupted by the reset. If the header portion of the cell has been sent then this corruption will not be detected at the receiver if header error detection is enabled. However it will likely be detected if cell error detection is enabled. See Transmit High-Speed Serial Configuration Register, CELLCRC bit, and RXD1, RXD2 Serial Configuration Register, CELLCRC bit for details.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE and the Master Interrupt Enable bit of the Master Configuration register are set to logic 1, the interrupt is enabled.

Register 0x5D: Transmit Logical Channel FIFO Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	FOVRI	X

FOVRI:

The FOVRI bit indicates an interrupt due to a Transmit Logical Channel FIFO overrun error condition. This interrupt is generated when a write attempt is performed to a FULL channel. Generally, the FOVRI status bit should never be asserted; its assertion would indicate that the flow control protocol is being ignored. This bit is reset immediately after a read to this register.

Register 0x5E: Transmit Logical Channel FIFO Depth

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	FDEPTH[5]	0
Bit 4	R/W	FDEPTH[4]	0
Bit 3	R/W	FDEPTH[3]	0
Bit 2	R/W	FDEPTH[2]	0
Bit 1	R/W	FDEPTH[1]	1
Bit 0	R/W	FDEPTH[0]	0

FDEPTH[5:0]:

The FDEPTH[5:0] bits are used to set the total number of available cells per logical channel of the Transmit FIFO. The value of FDEPTH[5:0] varies according to the configuration of the modem interface. If the SCI-PHY interface is used (the SCYPHY pin is set to logic 1), the FIFO Depth is to be set to 0b000010. If the Clock Serial Data Interface is used, the FIFO depth is to be set to 0b000100. Setting FDEPTH[5:0] to others values may cause FIFO malfunction.

Register 0x60: Transmit High-Speed Serial Configuration

Bit	Type	Function	Default
Bit 7	R/W	DSCR	0
Bit 6	R/W	HSCR	1
Bit 5		Unused	X
Bit 4	R/W	DHCS	0
Bit 3	R/W	CELLCRC	0
Bit 2	R/W	PREPEND	0
Bit 1	R/W	USRHDR[1]	1
Bit 0	R/W	USRHDR[0]	0

This register configures the format of the cells transmitted on both the TXD1+/- and the TXD2+/- serial links.

USRHDR[1:0]:

The USRHDR[1:0] bits determine the length of the User Header field of the transmitted cells. The User Header defaults to six bytes.

USRHDR[1:0]	Bytes in User Header
00	4
01	5
10	6
11	Reserved

PREPEND:

The PREPEND bit determines if the User Prepend field is inserted into the transmitted cells. If PREPEND is logic 1, a two byte User Prepend is inserted after the System Prepend field.

CELLCRC:

The CELLCRC bit determines whether the entire high-speed serial data structure is protected by a CRC-8 code word. The PREPEND bit must be logic 1 for this bit to have effect. If CELLCRC and PREPEND are logic 1, the second User Prepend byte is overwritten by the CRC-8 syndrome for the

preceding cell. If CELLCRC is logic 0, the contents of the second User Prepend byte are transported transparently.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet for a single cell is inverted prior to insertion. After the insertion, DHCS is automatically reset to logic 0. To invert the HCS octet in another cell, DHCS must be set to logic 1 again.

DSCR and HSCR:

The Disable Scramble enable (DSCR) and Header Scramble enable (HSCR) bits control the scrambling of the cell. When DSCR is logic one, cell header and payload scrambling is disabled. When DSCR is logic zero, payload scrambling is enabled and cell header scrambling is determined by HSCR. HSCR enables scrambling of the System Prepend, User Prepend, User Header, and HCS byte collectively. The operation of the DSCR and HSCR bits is summarized below:

DSCR	HSCR	Operation
1	X	Cell payload and header scrambling is disabled. THIS CONFIGURATION SHOULD ONLY BE USED FOR DIAGNOSTIC PURPOSES.
0	0	Cell payload is scrambled. Cell header is left unscrambled. THIS CONFIGURATION SHOULD ONLY BE USED FOR DIAGNOSTIC PURPOSES.
0	1	Cell payload and header are both scrambled.

Register 0x61: Transmit High-Speed Serial Cell Count Status

Bit	Type	Function	Default
Bit 7	R/W	XFERE	0
Bit 6	R	XFERI	X
Bit 5	R	OVR	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register indicates whether the associated Transmit Cell Count registers have been updated with new data and whether this data overwrites unacknowledged data.

OVR:

The OVR bit is the overrun status of the associated Transmit Cell Count registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and thus the contents of the Transmit Cell Count registers have been overwritten. OVR is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of Transmit Cell Count data has occurred. A logic 1 in this bit position indicates that the associated Transmit Cell Count registers have been updated. This update is initiated by writing to one of the associated Transmit Cell Count register locations or by writing to the Load Performance Meters (0x000) register. XFERI is set to logic 0 when this register is read.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the associated Transmit Cell Count registers. When XFERE and the Master Interrupt Enable bit of the Master Configuration register are set to logic 1, the INTB output is asserted low if the XFERI bit is a logic 1.

Register 0x62: Transmit High-Speed Serial Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 0x63: Transmit High-Speed Serial Cell Counter

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x64: Transmit High-Speed Serial Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[23]	X
Bit 6	R	TCELL[22]	X
Bit 5	R	TCELL[21]	X
Bit 4	R	TCELL[20]	X
Bit 3	R	TCELL[19]	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[23:0]:

The TCELL[23:0] bits indicate the number of cells inserted into the transmission stream during the last accumulation interval. Stuff cells inserted into the transmission stream for rate decoupling are not counted.

A write to any one of the Transmit Cell Counter registers for a particular serial link or a write to the Load Performance Meters (0x00) register loads the registers with the current counter value and resets the internal 24 bit counter. The counter should be polled at least every 30 seconds to avoid saturating. The contents of these registers become valid within 300 ns after a transfer is triggered by a write to any of the link-associated Transmit Cell Count registers or to the Load Performance Meters (0x00) register, and remain valid until another transfer is triggered.

The count saturates at all ones.

Register 0x68: Receive Serial Indirect Channel Select

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	DRHCSE	0
Bit 4		Unused	X
Bit 3	R/W	CHAN[3]	0
Bit 2	R/W	CHAN[2]	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

This register provides the channel number used to access the channel provision RAM of the receive Clocked Serial Data Interface. Writing to this register triggers an indirect channel register access.

CHAN[3:0]:

The indirect channel number bits (CHAN[3:0]) indicate the channel to be configured or interrogated in the indirect access.

DRHCSE:

Disable Reset of the HCS Error Count (DRHCSE) disables automatic reset of the HCS Error Counter (HCSERR). When the bit is set to logic 0, automatic reset of the HCS Error Counter is enabled. If an indirect read is initiated (i.e., CRWB written with logic 1) with DRHCSE logic 0, the HCS Error Counter is reset to zero upon completion of the indirect read. When the DRHCSE bit is set to logic 1, automatic reset of the HCS Error Counter is disabled.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel provision RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the Receive Serial Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The data read can be found in the Receive Serial Indirect Channel Data registers.

CBUSY:

The indirect access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to the Receive Serial Indirect Channel Select register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Receive Serial Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than two REFCLK cycles.

Register 0x69:
Receive Serial Indirect Channel Configuration

Bit	Type	Function	Default
Bit 7	R/W	PROV	0
Bit 6	R/W	HCSPASS	0
Bit 5	R/W	UNASSFLTR	0
Bit 4	R/W	IDLEPASS	0
Bit 3	R/W	DDSCR	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DDELIN	0
Bit 0		Unused	X

This register contains data read from the channel provision RAM of the Receive Clocked Serial Data Interface after an indirect channel read operation or data to be inserted into the channel provision RAM in an indirect channel write operation.

The bits to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. The bits reflect the value written until the completion of a subsequent indirect channel read operation.

The reset state of the bits enables standard ATM cell processing as stipulated in ITU-T Recommendation I.432.1.

DDELIN:

The indirect disable delineate enable bit (DDELIN) configures the TC processor to perform cell delineation and header error detection on the incoming data stream. When DDELIN is set to logic 0, the cell alignment is established and maintained on the incoming data stream. When DDELIN is set to logic 1, the RTTC does not perform any processing on the incoming stream, but passes data through transparently.

Reserved:

This bit must be logic 0 for correct operation.

DDSCR:

The DDSCR bit controls the descrambling of the cell payload with the polynomial $x^{43} + 1$. When DDSCR is set to logic 1, cell payload descrambling is disabled. When DDSCR is set to logic 0, payload descrambling is enabled.

IDLEPASS:

The IDLEPASS bit controls the function of the idle cell filter. When IDLEPASS is written with a logic 0, all idle cells (first four bytes of cell are ‘H00, ‘H00, ‘H00, ‘H01) are filtered out. When IDLEPASS is logic 1, idle cells are passed on to the cell buffer.

UNASSPASS:

When UNASSPASS is written with a logic 0, all unassigned cells (first four bytes of cell are ‘H00, ‘H00, ‘H00, ‘H00) are filtered out. When UNASSPASS is logic 1, unassigned cells are passed on the cell buffer.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of an HCS error. When HCSPASS is logic 0, cells containing an HCS error are dropped. When HCSPASS is a logic 1, cells are passed to the external cell buffer regardless of errors detected in the HCS. Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states.

PROV:

The indirect provision enable bit (PROV) reports the channel provision enable flag read from the channel provision RAM after an indirect channel read operation has completed. When PROV is set to logic 1, the TC processor will process data on the channel specified by CHAN[3:0]. When PROV is set to logic 0, the TC processor will ignore data on the channel specified by CHAN[3:0].

Register 0x6A:
Receive Serial Indirect Channel Interrupt Enables

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	OOCDE	0
Bit 2	R/W	HCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	LCDE	0

This register contains data read from the channel provision RAM of the Receive Clocked Serial Data Interface after an indirect read operation or data to be inserted into the channel provision RAM in an indirect write operation.

The bits to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. The bits reflect the value written until the completion of a subsequent indirect channel read operation.

LCDE:

The LCDE bit enables the generation of an interrupt due to a change in the LCD state. When LCDE is set to logic 1, the interrupt is enabled.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set to logic 1, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of an HCS error. When HCSE is set to logic 1, the interrupt is enabled.

OOCDE:

The OOCDE bit enables the generation of an interrupt due to a change in cell delineation state. When OOCDE is set to logic 1, the interrupt is enabled.

Register 0x6B:
Receive Serial Indirect Channel Interrupt and Status

Bit	Type	Function	Default
Bit 7	R	OOCDV	X
Bit 6	R	LCDV	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	OOCDI	X
Bit 2	R	HCSI	X
Bit 1	R	FOVRI	X
Bit 0	R	LCDI	X

This register contains data read from the channel provision RAM of the Receive Clocked Serial Data Interface after an indirect read operation.

LCDI:

The LCDI bit is set to logic 1 when there is a change in the loss of cell delineation (LCD) state. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set to logic 1 when a FIFO overrun has occurred or is about to occur. Normally the occurrence of the FOVRI interrupt indicates that one or more user cells have been discarded due to the buffer overflow condition. However, if the overflow pending condition exists only temporarily (and when only IDLE cells are being received) it is possible that no user cells were actually discarded. This bit is reset immediately after a read to this register.

HCSI:

The HCSI bit is set to logic 1 when an HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI:

The OOCDI bit is set to logic 1 when the logical channel enters or exits the SYNC state. The OOCDV bit indicates whether the logical channel is in the SYNC state or not. The OOCDI bit is reset immediately after a read to this register.

LCDV:

The LCDV bit gives the Loss of Cell Delineation state. When LCD is logic 1, an out of cell delineation (OCD) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LCD is logic 0, no OCD has persisted for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[7:0] register bits in the LCD Count Threshold register.

OOCDV:

The OOCDV bit is set to logic 1 when the logical channel is not currently in the SYNC state.

Register 0x6C:
Receive Serial Indirect Channel HCS Error Count

Bit	Type	Function	Default
Bit 7	R	HCSERR[7]	X
Bit 6	R	HCSERR[6]	X
Bit 5	R	HCSERR[5]	X
Bit 4	R	HCSERR[4]	X
Bit 3	R	HCSERR[3]	X
Bit 2	R	HCSERR[2]	X
Bit 1	R	HCSERR[1]	X
Bit 0	R	HCSERR[0]	X

This register contains data read from the channel provision RAM of the Receive Clocked Serial Data Interface after an indirect read operation.

HCSERR[7:0]:

The HCSERR[7:0] bits indicate the number of HCS error events that occurred during the last accumulation interval of the receive Clock Serial Data Interface. When the number of HCS error events during the last accumulation interval exceeds 255, the HCSERR[7:0] retains value of FFH until the next accumulation interval.

Register 0x6D: Receive Serial LCD Count Threshold

Bit	Type	Function	Default
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[7:0]:

The LCDC[7:0] bits represent the number of consecutive cell periods the receive cell processor of the Clock Serial Data Interface must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not deasserted until the receive cell processor is in cell delineation for the number of cell periods specified by LCDC[7:0].

The default value of LCD[7:0] of 104 translates to 73 ms at 600 kb/s.

Register 0x70: Transmit Serial Indirect Channel Select

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	CHAN[3]	0
Bit 2	R/W	CHAN[2]	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

This register provides the channel number used to access the channel provision RAM of the transmit Clocked Serial Data Interface. Writing to this register triggers an indirect channel register access.

CHAN[3:0]:

The indirect channel number bits (CHAN[3:0]) indicate the channel to be configured or interrogated in the indirect access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel provision RAM. Writing a logic zero to CRWB triggers an indirect write operation. Data to be written is taken from the Transmit Serial Indirect Channel Data registers. Writing a logic one to CRWB triggers an indirect read operation. The read can be found in the Transmit Serial Indirect Channel Data registers.

CBUSY:

The indirect access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to the Transmit Serial Indirect Channel Select register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Transmit Serial Indirect Channel Data registers or to determine when a new indirect write operation may commence.

Register 0x71:Transmit Serial Indirect Channel Data

Bit	Type	Function	Default
Bit 7	R/W	DHCS	0
Bit 6	R/W	HSCR	0
Bit 5	R/W	DSCR	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register contains data read from the channel provision RAM of the Transmit Clocked Serial Data Interface after an indirect channel read operation or data to be inserted into the channel provision RAM in an indirect channel write operation.

DSCR:

The indirect scrambling disable bit (DSCR) configures scrambling. The scramble disable bit to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DSCR is logic 1, scrambling is disabled. When DSCR is logic 0, either the 48 byte payload or the entire bit stream (if HSCR is logic 1) is scrambled. DSCR reflects the value written until the completion of a subsequent indirect channel read operation.

HSCR:

The indirect header scrambling enable bit (HSCR) configures header scrambling. The header scramble enable bit to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When HSCR is logic 1 and DSCR is logic 0, the header is scrambled in addition to the payload. When HSCR is logic 0 and DSCR is logic 0, only the cell payload is scrambled. HSCR reflects the value written until the completion of a subsequent indirect channel read operation.

DHCS:

The Disable HCS (Header Check Sequence) bit (DHCS) configures the insertion of the HCS in the fifth byte of the cell. The value of DHCS to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DHCS is logic 0, the CRC-8 calculation over the first four bytes of the cell overwrites the fifth byte. When DHCS is logic 1, the fifth byte of the cell passes through unmodified. (It is still subject to scrambling.) DHCS reflects the value written until the completion of a subsequent indirect channel read operation.

Register 0x74:Transmit Serial Alignment Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	ALIGN	0

ALIGN:

The alignment enable bit (ALIGN) allows ATM/Data octet alignment to frame boundaries based on recognizing gaps in the clock. When this bit is set to logic 1, the ATM /Data octets are aligned to the inferred frame alignment, with the most significant bit output first during the clock gap. No frame alignment is inferred when this bit is set to logic 0.

To be detected, the gap polarity must match the value of the LTXCINV bit of the Master Configuration register. When the rising edge of clock signals on LTXC[15:0] is used to output the data (LTXCINV set to logic 0), gaps during which the clock is forced to logic 0 are detected. When the falling edge of the clock signals on LTXC[15:0] are used to output the data (LTXCINV set to logic 1), gaps during which the clock is forced to logic 1 are detected.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-DUPLEX. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[7]) is high.

The S/UNI-DUPLEX supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced with the exception of the RXD1+/-, RXD2+/-, TXD1+/- and TXD2+/- pins via the JTAG test port.

A limited RAM built-in-self-test (BIST) is available.

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x80: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-DUPLEX test features. All bits, except PMCTST and PMCATST, are reset to zero by a reset or a software reset of the S/UNI-DUPLEX.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-DUPLEX. While the HIZIO bit is a logic one, all output pins of the S/UNI-DUPLEX except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-DUPLEX for board level testing. When IOTST is a logic one, all blocks are held in test mode.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-DUPLEX to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-DUPLEX for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-DUPLEX microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST:

The PMCATST bit is used to configure the analog portion of the S/UNI-DUPLEX for PMC's manufacturing tests. PMCATST is cleared when CSB is high and RSTB is low or when PMCATST is written as logic 0.

Register 0x83: Miscellaneous Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	TCADIS	0
Bit 4	R/W	LINKSELBP	0
Bit 3	R/W	SELOCD	0
Bit 2	R/W	CKLSEL[2]	0
Bit 1	R/W	CLKSEL[1]	0
Bit 0	R/W	CLKSEL[0]	0

CLKSEL[2:0]:

The CLKSEL[2:0] bits can be used to output a internally generated clock on the RX8K output to increase the observability of the device for test purpose. When CLKSEL[2:0] is set to 0b00 (default mode), the RX8K output is extracted from one of the receive high-speed serial links, RXD1+/- or RXD2+/-. When set to other values, an internally generated clock is muxed on the RX8K output, as described in the following table:

CLKSEL[2:0]	Clock
00000	RX8K
00001	ACT_RCLK
00010	SYSCLK

00011	CSDCLK
00100	DCLK
00101	CCLK
00110	L1_RCLK
00111	L2_RCLK

SELOCD:

The SELOCD bit allows usage of the OCD signal instead of the LCD signal to gate to gate the ACTIVEBIT extracted from the high-speed serial links. This is useful to speed up simulation, LCD being a very slow signal.

LINKSELBP:

The LINKSELBP allows to bypass the sequenced automatic link selection circuit. When LINKSELBP is set to logic 1, the high-speed serial link selection is immediate. When set to logic 0, the high-speed serial link selection will be performed prior just prior to an incoming cell (idle or data) on the “to be active” serial link.

TCADIS:

The TCADIS bit disables the transmission of the flow control information in the upstream direction of the inactive high-speed serial link. Its usage is intended for test purposes. When set to logic 1, the S/UMI-DUPLEX will indicates on the inactive high-speed serial link that it can not accept cells on any logical channel. When set to logic 0, the flow control bits for the logical channel are identical to the flow control bits of the active channel. The flow control bits of the active high-speed serial link are not affected by the TCADIS.

11.1 RAM Built-In-Self-Test

The S/UNI-DUPLEX contains built-in-self-test (BIST) circuitry for production testing of the device. A subset of the functionality is available for in situ screening against damage during handling and board manufacture.

The tests are controlled through the microprocessor port. Clock signals need to be applied to the device. The only other signals involved are the REFCLK, TCK and TX8K inputs.

11.1.1 128x8 RAM

The following procedure tests the six 128x8 RAMs simultaneously:

1. Hold REFCLK, TCK and TX8K low.

2. Set the RESET bit of the Master Reset and Identity register (0x00) to logic 1 to place the device in a known state.

3. Write the following register locations to select the test mode and initialize the BIST circuitry:

    1. Write 0x02 to 0xB1, 0xB5, 0xB9

    2. Write 0x01 to 0xB0, 0xB4, 0xB8

    3. Write 0x55 to 0xB2, 0xB6, 0xBA

    These registers do not have default values and must be written.

4. Clear the RESET bit of the Master Reset and Identity register (0x00) to logic 0.

5. Set the IOTST bit of the Master Test register (0x80) to logic 1. This activates the BIST test mode.

6. Start toggling the REFCLK, TCK and TX8K inputs at up to a maximum frequency of 4 MHz. All clocks need be phase and frequency locked.

7. After exactly 2045 clock cycles read the following registers and compare against the expected data. Any discrepancies represent a test failure. The two bits being compared are flags that are cleared when at least one RAM bit location returns an incorrect value. Letting the test run indefinitely simply causes the test sequences to be repeated.

A[7:0]	Expected D[7:0]
0xB2, 0xB6, 0xBA	xxxx0011

11.1.2 2048x8 RAM

The following procedure tests the two 2048x8 RAMs: simultaneously:

1. Hold REFCLK and TCK low.

2. Set the RESET bit of the Master Reset and Identity register (0x00) to logic 1 to place the device in a known state.

3. Write the following register locations to select the test mode and initialize the BIST circuitry:

1. Write 0x02 to 0xDD
2. Write 0x01 to 0xDC
3. Write 0x55 to 0xDE

These registers do not have default values and must be written.

4. Clear the RESET bit of the Master Reset and Identity register (0x00) to logic 0.
5. Set the IOTST bit of the Master Test register (0x80) to logic 1. This activates the BIST test mode.
6. Start toggling the REFCLK and TCK inputs at up to a maximum frequency of 4 MHz. All clocks need be phase and frequency locked.
7. After exactly 32765 clock cycles read the following register and compare against the expected data. Any discrepancies represent a test failure. The two bits being compared are flags that are cleared when at least one RAM bit location returns an incorrect value. Letting the test run indefinitely simply causes the test sequences to be repeated.

A[7:0]	Expected D[7:0]
0xDE	xxxx0011

11.1.3 4096x8 RAM

The following procedure tests the two 4096x8 RAMs simultaneously:

1. If SCIANY is set to logic 1, OFCLK and REFCLK are to be used. If SCIANY is set to logic 0, TCK and REFCLK are used. Keep clock signals low.
2. Set the RESET bit of the Master Reset and Identity register (0x00) to logic 1 to place the device in a known state.
3. Write the following register locations to select the test mode and initialize the BIST circuitry:
    1. Write 0x02 to 0xBD
    2. Write 0x01 to 0xBC
    3. Write 0x55 to 0xBE

These registers do not have default values and must be written.

4. Clear the RESET bit of the Master Reset and Identity register (0x00) to logic 0.

5. Manually select link 1 as the active link by writing 0x00 to the Master Configuration register (0x01).

6. Set the IOTST bit of the Master Test register (0x80) to logic 1. This activates the BIST test mode.

7. Start toggling the OFCLK and REFCLK or TCK and REFCLK (depending on the SCIANY input) at up to a maximum frequency of4 MHz. Both clocks need be phase and frequency locked.

8. After 65533 clock cycles read the following register and compare against the expected data. Any discrepancies represent a test failure. The two bits being compared are flags that are cleared when at least one RAM bit location returns an incorrect value. Letting the test run indefinitely simply causes the test sequences to be repeated.

A[7:0]	Expected D[7:0]
0xBE	xxxx0011

11.2 JTAG Test Port

The S/UNI-DUPLEX JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 1H

Part Number - 7350H

Manufacturer's identification code - 0CDH

Device identification - 173500CDH (with CDSDIS tied to VSS).

Length - 100 bits

Table 18: Boundary Scan Register

Pin/Enable	Register Bit	Cell Type	Enable	Pin/Enable	Register Bit	Cell Type	Enable
hiz_oen	0	ENABLE		oavalid_lrxd_1	50	IO_CELL	octrl_oen
rstob	1	OUT_CELL		oenb_lrxd_2	51	IO_CELL	octrl_oen
ica_lrxc_13	2	IO_CELL	ica_oen	oca_lrxc_2	52	IO_CELL	oca_oen

ica_oen	3	ENABLE		oca_oen	53	OUT_CELL	
ienb_lrxd_13	4	IO_CELL	ictrl_oen	osx_lrxc_3	54	IO_CELL	odat_oen
iaddr_0_lrxc_14	5	IO_CELL	ictrl_oen	osoc_lrxd_3	55	IO_CELL	odat_oen
iaddr_1_lrxd_14	6	IO_CELL	ictrl_oen	odat_0_ltxc_2	56	IO_CELL	odat_oen
ictrl_oen	7	ENABLE		odat_1_lrxc_4	57	IO_CELL	odat_oen
iaddr_2_ltxc_14	8	IO_CELL	ictrl_oen	odat_2_lrxd_4	58	IO_CELL	odat_oen
iaddr_3_lrxc_15	9	IO_CELL	ictrl_oen	odat_3_lrxd_5	59	IO_CELL	odat_oen
iaddr_4_lrxd_15	10	IO_CELL	ictrl_oen	odat_4_lrxc_6	60	IO_CELL	odat_oen
iavalid_ltxc_15	11	IO_CELL	ictrl_oen	oanyphy_ltxd_2	61	IO_CELL	csd_oen
ibus8_ltxd_14	12	IO_CELL	csd_oen	ofclk_lrxc_5	62	IN_CELL	
imaster_ltxd_15	13	IO_CELL	csd_oen	obus8_ltxd_4	63	IO_CELL	csd_oen
intb	14	OUT_CELL		odat_5_lrxd_6	64	IO_CELL	odat_oen
sciany	15	IN_CELL		odat_oen	65	ENABLE	
csb	16	IN_CELL		odat_6_lrxc_7	66	IO_CELL	odat_oen
rdb	17	IN_CELL		odat_7_lrxd_7	67	IO_CELL	odat_oen
ale	18	IN_CELL		odat_8_ltxc_3	68	IO_CELL	odat_oen
wrb	19	IN_CELL		ltxd_3	69	IO_CELL	csd_oen
a[7]	20	IN_CELL		odat_9_ltxc_4	70	IO_CELL	odat_oen
a[6]	21	IN_CELL		odat_10_lrxc_8	71	IO_CELL	odat_oen
a[5]	22	IN_CELL		odat_11_lrxd_8	72	IO_CELL	odat_oen
rstb	23	IN_CELL		odat_12_ltxc_5	73	IO_CELL	odat_oen
a[4]	24	IN_CELL		odat_13_lrxc_9	74	IO_CELL	odat_oen
a[3]	25	IN_CELL		odat_14_lrxd_9	75	IO_CELL	odat_oen
a[2]	26	IN_CELL		odat_15_lrxc_10	76	IO_CELL	odat_oen
a[1]	27	IN_CELL		oprty_lrxd_10	77	IO_CELL	odat_oen
a[0]	28	IN_CELL		ianyphy_ltxd_5	78	IO_CELL	csd_oen
tx8k	29	IN_CELL		csd_oen	79	ENABLE	
d[7]	30	IO_CELL	d_oen	isx_ltxc_6	80	IN_CELL	
d[6]	31	IO_CELL	d_oen	isoc_ltxd_6	81	IO_CELL	csd_oen
d[5]	32	IO_CELL	d_oen	idat_0_ltxc_7	82	IN_CELL	
d[4]	33	IO_CELL	d_oen	idat_1_ltxd_7	83	IO_CELL	csd_oen
rclk	34	OUT_CELL	hiz_oen	idat_2_ltxc_8	84	IN_CELL	
d_oen	35	ENABLE		idat_3_ltxd_8	85	IO_CELL	csd_oen
rx8k	36	OUT_CELL	hiz_oen	idat_4_ltxd_9	86	IO_CELL	csd_oen
d[3]	37	IO_CELL	d_oen	ifclk_ltxc_9	87	IN_CELL	
d[2]	38	IO_CELL	d_oen	idat_5_ltxc_10	88	IN_CELL	
d[1]	39	IO_CELL	d_oen	idat_6_ltxd_10	89	IO_CELL	csd_oen
d[0]	40	IO_CELL	d_oen	idat_7_lrxc_11	90	IN_CELL	
ltxd_0	41	IO_CELL	csd_oen	idat_8_lrxd_11	91	IN_CELL	
refclk	42	IN_CELL		idat_9_ltxc_11	92	IN_CELL	
omaster_ltxd_1	43	IO_CELL	csd_oen	idat_10_ltxd_11	93	IO_CELL	csd_oen
oaddr_0_lrxc_0	44	IO_CELL	octrl_oen	idat_11_lrxc_12	94	IN_CELL	
oaddr_1_lrxd_0	45	IO_CELL	octrl_oen	idat_12_lrxd_12	95	IN_CELL	
oaddr_2_ltxc_0	46	IO_CELL	octrl_oen	idat_13_ltxc_12	96	IN_CELL	
octrl_oen	47	ENABLE		idat_14_ltxd_12	97	IO_CELL	csd_oen

oaddr_3_ltxc_1	48	IO_CELL	octrl_oen	idat_15_ltxc_13	98	IN_CELL	
oaddr_4_lrxc_1	49	IO_CELL	octrl_oen	iprty_ltxd_13	99	IO_CELL	csd_oen

NOTES:

1. When set high, HIZ_OEN forces all OUT_CELL and IO_CELL except INTB and RSTOB to high impedance.

2. RX8K_OEN is the first bit of the boundary scan chain scanned in and out.

11.2.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Fig. 12 Input Observation Cell (IN_CELL)

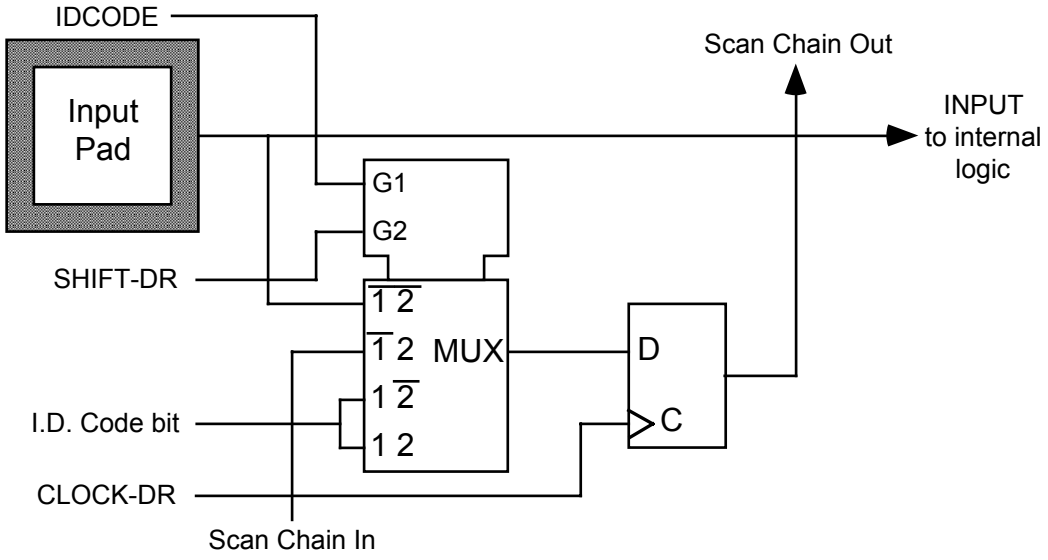


Fig. 13 Output Cell (OUT_CELL)

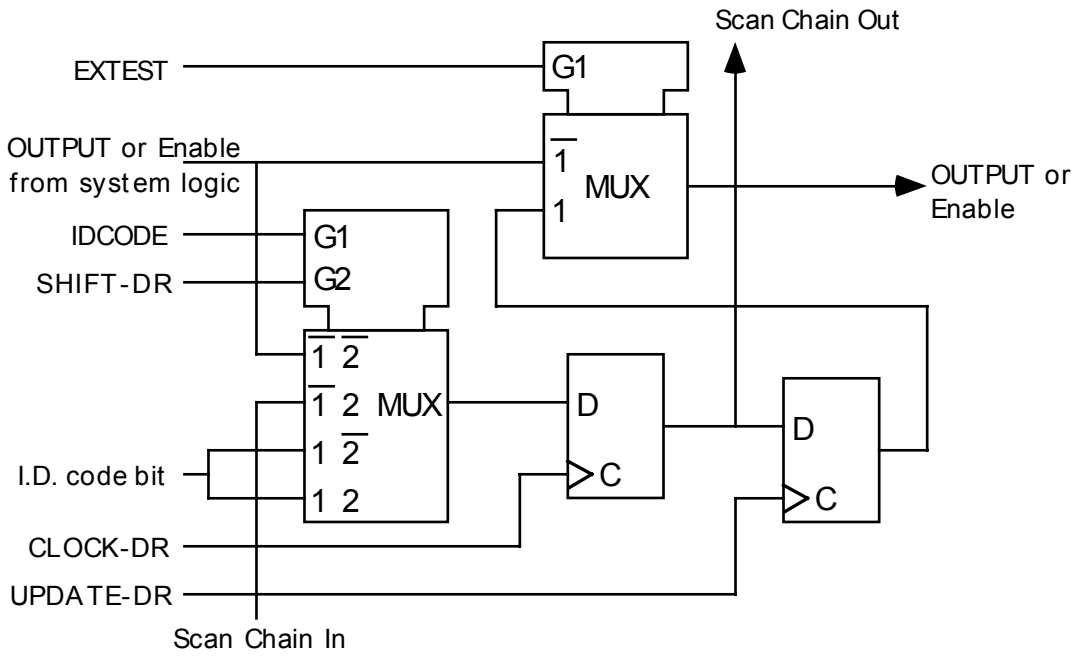


Fig. 14 Bidirectional Cell (IO_CELL)

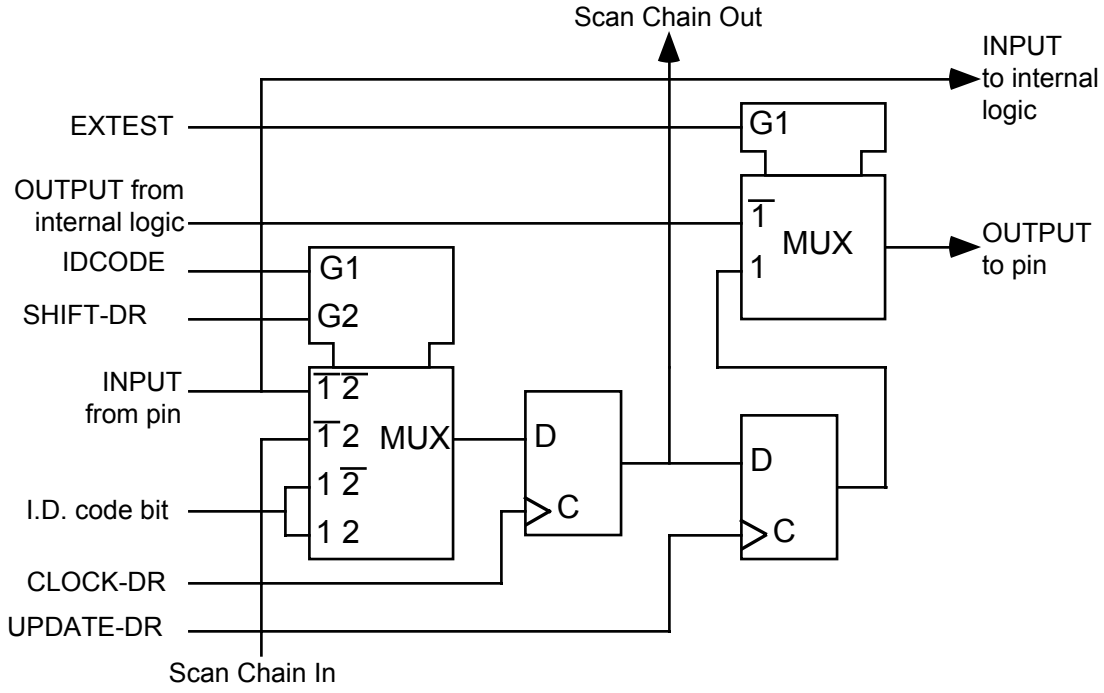
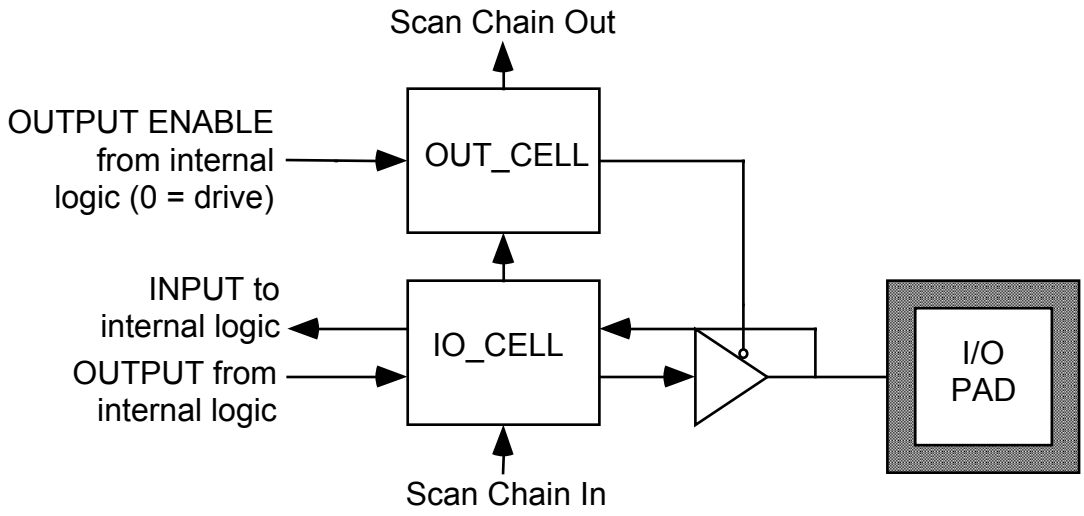


Fig. 15 Layout of Output Enable and Bidirectional Cells



12 OPERATION

12.1 Microprocessor Inband Communication

In the upstream direction, the S/UNI-DUPLEX broadcasts control channel cells on both the active and spare high-speed serial links. The contents of the cells shall distinguish the two control channels if necessary. In the downstream direction, each high-speed serial link has a dedicated queue for the control channel cells.

The S/UNI-DUPLEX includes hardware support for CRC-32 generation and verification. It consists of two accumulator registers, the Insert CRC-32 Accumulator register for control channel in the upstream direction and the Extract CRC-32 Accumulator for control channel in the downstream direction. To allow context change, each accumulator register can be preset, read and written by the microprocessor.

12.1.1 Inserting Cells Into Control Channels

Cells are inserted into control channels by manipulating the Microprocessor Insert FIFO Control and Microprocessor Insert FIFO Ready registers. The following steps are required to insert a cell:

1. Poll the INSRDY bit in the Microprocessor Insert FIFO Ready. Alternately, service the interrupts that result from setting the INSRDYE bit in the Microprocessor Cell Buffer Interrupt Control and Status register.

2. If CRC-32 calculation is required set the INSCRCPR of the Microprocessor Insert FIFO Control register to logic 0 to enable the CRC-32 process. The Insert CRC-32 Accumulation register can be preset by writing a logic 1 to INSCRCPR prior to enabling the CRC-32 calculation.

   If the cell is not the first of the message, write the Insert CRC-32 Accumulator register with the value stored at the end of the previous cell for the same control channel. This step is not necessary if the last cell inserted belonged to the same control channel as the current cell.

   Insertion of the CRC-32 field is done by setting the INSCRCEND bit of the Microprocessor Insert FIFO Control register to logic 1 prior to writing the last cell of the CPCS-PDU. The S/UNI-DUPLEX will overwrite the data of the last four bytes of the cell payload written by the microprocessor with the ones complement of the content of the Insert CRC-32 Accumulator register.

3. Write the cell content to the Microprocessor Cell Data register. Cell data is entered in the format illustrated in Fig. 11.

4. If the cell is not the last of the message, read and store the contents of the Insert CRC-32 accumulator register. This step is not necessary if the next cell to be inserted belongs to the same control channel as the current cell.

The above sequence is repeated as needed to insert more cells. The assertion of the INSRDY bit of the Insert FIFO indicates that the FIFO is ready again to be written to. Setting INSRST of the Insert FIFO Control register to logic 1 prior to writing the last cell byte allows the overwriting of the cell data.

12.1.2 Reading Cell Data From a Control Channel

Reading cell data from a control channel is done by manipulating the Microprocessor Extract FIFO Control and Microprocessor Extract FIFO Ready registers. The following steps are required to read a cell from one of the Extract FIFOs.

1. Poll the bit of EXTRDY[1:0] in the Microprocessor Extract FIFO Ready registerhigh-speed. The EXTRDY[0] and EXTRDY[1] bits indicate the status of the FIFO receiving control channel cells from the RXD1+/- and RXD2+/- high-speed links, respectively. Alternately, service the interrupts that result from setting the EXTRDYE bit in the Microprocessor Cell Buffer Interrupt Control and Status register.

2. Select the Extract FIFO corresponding to the desired high-speed link by writing its identification number to the EXTFSEL bit of the Microprocessor Extract FIFO Control register. A logic 0 selects the RXD1+/- FIFO while a logic 1 selects the RXD2+/- FIFO.

3. Read the header of the cell to determine if it is the end of message and to which virtual channel it belongs.

4. If CRC-32 protection is required, set the EXTCRCPR of the Microprocessor Extract FIFO Control and Status register to logic 0 to enable the CRC-32 process. The Extract CRC-32 accumulation register can be preset for the first cell of a message by writing a logic 1 to EXTCRCPR prior to enable the CRC-32 calculation. If the cell is not the first one of a message and does not belong to the same control channel as the previous cell read, initialize the Extract CRC-32 Accumulator registers to the value saved from the previous cell read for the control channel.

   CRC-32 field check is done by setting the EXTCRCCHK bit of the Microprocessor Extract FIFO Control register to logic 1. This causes the

S/UNI-DUPLEX to verify that the content of the CRC-32 Accumulator register is equal to the expected CRC-32 remainder polynomial when the last byte of the cell is read from the Extract FIFO. The microprocessor can verify the CRC-32 field check result either through interrupt servicing or polling techniques.

When interrupt servicing is used, the microprocessor enables the CRC-32 field check prior to reading the last cell of the CPCS-PDU. An interrupt is raised if a CRC-32 error is found and the EXTCRCERRE bit is set.

When polling is used, the EXTCRCERRE bit is kept to logic 0 and CRC-32 field check is always enabled. The microprocessor verifies the value of the EXTCRCERRI bit after reading the last cell of a CPCS-PDU.

5. Read the cell content from the Microprocessor Cell Data register. Cell data is extracted in the format illustrated in Fig. 11.

6. If the cell is not the last of the message, read and store the content of the Extract CRC-32 Accumulator register. This step is not necessary if the next cell extracted is known to belong to the same control channel as the current cell.

The above sequence is repeated as needed to read more cells. The assertion of the bit of EXTRDY[1:0] of an Extract FIFO indicates that the FIFO is ready again to be read from. Setting EXTABRT of the Extract FIFO Control register to logic 1 allows the microprocessor to discard a cell without reading the remaining content.

12.2 Interaction Between Bus and LVDS Configurations

Since the far-end and near-end devices are configured independently it is important to take into account how the optional fields (the Any-PHY address field, the H5 (H5/UDF) header bytes, and the user prepend word) are treated on an end-to-end basis. The following table summarizes the possible cell format options and summarizes the resultant impact on the cell contents at the receiving end.

Note the following:

- The S/UNI-DUPLEX's LVDS links will be connected to other S/UNI-DUPLEX or to S/UNI-VORTEX devices. The following tables identify registers appropriate for a S/UNI-DUPLEX to S/UNI-DUPLEX connection. The results are similar for a S/UNI-DUPLEX to S/UNI-VORTEX. The S/UNI-VORTEX supports a more limited number of configurations (it does not support 8-bit

parallel bus, master bus mode or clocked serial data). Refer to the S/UNI-VORTLEX datasheet for details.

- The parallel bus of the S/UNI-DUPLEX is fully compliant to Utopia Level 2 bus protocol only when configured as a bus master. In this case, cell length is either 53 bytes or 27 16-bit words depending if the interface bus width is set to 8 or 16 bit.

- When used as a bus slave, the parallel bus input and output ports can operate in SCI-PHY or Any-PHY mode. When configured as a SCI-PHY bus slave, the input port can be remains compliant to Utopia Level 2 (default setting), but the output port becomes a proxy, a single addressable PHY carrying the cell traffic for up to the 32 PHYs. The PHY ID is encoded in a system prepend byte or 16-bit word (depending if the interface bus width is set to 8 or 16 bit). To keep the cell compatible with Utopia Level 2 format, the PHY ID can be routed in the H5 (H5/UDF for 16-bit bus) field of the cell by setting the INADDUDF bit of the SCI-PHY/Any-PHY Output Configuration register to logic 1.

- When operating in SCI-PHY (master or slave mode) or in Any-PHY slave mode, prepend words can be added to the cell, up to two bytes for the 8-bit (PRELEN[1:0]=0b10) cell format and one word in 16-bit (PRELEN[1:0]=0b01) cell format. The H5 (H5/UDF) field of the cell can be omitted as determined by setting the H5UDF of the SCI-PHY/Any-PHY Input Configuration 1 and SCI-PHY/Any-PHY Output Configuration registers to logic 0.

- Both input and output parallel interface can operate in Any-PHY mode, meaning Any-PHY bus timing and addressing must be used. Setting the INADDUDF bit of the register SCI-PHY/Any-PHY Output Configuration register to 1 when the bus is configured as Any-PHY has no effect. Although the S/UNI-DUPLEX only supports 32 logic channels, it is possible to specify the base address of the input port in a larger addressing range with the Extended Address Match and Extended Address Mask registers. The value of the Extended Address Match register is also appended to the PHY ID of cells read from the output port.

- For a given configuration set by the values of the H5UDF, INADDUDF and PRELEN[1:0], cell length may vary depending of the mode of the parallel bus, determined by the value of the IMASTER, IBUS8, IANYPPHY, OMASTER, OBUS8 and OANYPHY inputs. The following is an example of the various cell lengths produced by the input port default configuration (H5UDF=1, PRELEN[1:0]=00):

  SCI-PHY/Utopia 8-bit master: 53B
  SCI-PHY/Utopia 8-bit slave: 53B
  Any-PHY 8-bit slave: 54B (base cell + address)

SCI-PHY/Utopia16-bit master: 54B (base cell + UDF)
SCI-PHY/Utopia16-bit slave: 54B (base cell + UDF)
Any-PHY 16-bit slave: 56B (base cell + UDF + 2 address)

The similar output port default configuration produces the following cell lengths:

SCI-PHY/Utopia 8-bit master: 53B
SCI-PHY 8-bit slave: 54B (base cell + address)
Any-PHY 8-bit slave: 54B (base cell + address)
SCI-PHY/Utopia16-bit master 54B (base cell + UDF)
SCI-PHY16-bit slave: 56B (base cell + 2 address)
Any-PHY16-bit slave: 56B (base cell + UDF + 2 address)

In Table 19 to Table 23, these would be referred as 53/53/54(54/54/56) and 53/54/54(54/54/56) byte bus length.

- When the input side is configured as a 8-bit parallel bus or as a clocked serial data interface and the output side is configured as a 16-bit parallel bus, the UDF is undefined at the far end independently of the LVDS link configuration. When the input side is configured as a 16-bit parallel bus and the output side is configured as a 8-bit parallel bus or as a clocked serial data interface, the UDF is stripped at the far end.

- When using the CSD (Clock Serial Data interface), the cell size is fixed at 53 bytes. By default, cell delineation is enable on the Clocked Serial Data receive port (Receive Serial Indirect Channel Configuration register 0x69, DDELIN=0). The HCS value is used only to acquire and maintain cell delineation and does not need to be carried to the other side. Similarly, by default the HCS value is generated by the Clock Serial Data transmit interface (Transmit Serial Indirect Channel Data register 0x71, DHCS=0) and does need to be carried over the LVDS link.

- When unframed data is transported through the Clocked Serial Data interface, data is packet in 53 byte packet and carried transparently. All five fields of the cell header are used and must be carried.

- For control cells written or read via the microprocessor port, bytes 0&1 correspond to the microprocessor port's unique PHY address field. However since this field is fixed there is no useful information in these bytes. Bytes 10&11 are always undefined. Bytes 2&3 correspond to the user prepend bytes, and bytes 8&9 correspond to the H5&HDF bytes.

- The PHY address field is transported across the LVDS in an extra word added to each user cell. Therefore it is not necessary that the H5 (H5/UDF) field be sent over the LVDS link **even if the output bus interfaces is configured to embed the PHY address in the H5 (H5/UDF) field**. This will slightly increase the effective throughput of the LVDS, but it will impact control

cells inserted and extracted via the microprocessor port as described in section 12.1.

- Many valid combinations are not shown in Table 19 to Table 23. Some of the missing combinations are readily derived from the table. Other combinations make little sense. For example, there is no use sending prepend information over the LVDS link if the receiving bus is not configured for prepends. Even if the near-end bus is configured for prepend it is more bandwidth efficient to turn off prepend on the LVDS link (the default setting) and hence discard the prepend at the near-end bus interface.

Table 19 LVDS Link 59 Byte Cell Configurations

Far-End			Near-End				Resultant Cell contents at far-end Bus or Microprocessor
	input Reg 0x0C			output Reg 0x14			LVDS: both ends must match e.g. Reg 0x40, 0x50 and 0x60
SCIANY	H5UDF	PRELEN[1..0]	SCIANY	H5UDF	INADDUDF	PRELEN[1..0]	DEFAULT CONFIGURATION • 5 system, 6 header bytes, 48 data bytes USRHDR: 6 PREPEND: 0 CELLCRC: 0 • Control cell prepend bytes 2&3 are undefined, header bytes 8&9 are valid at far-end microprocessor.
1	1	0	1	1	0	0	• Cells are transferred from a 53/53/54(54/54/56) byte bus to a 53/54/54(54/56/56) byte bus. • H5/UDF byte(s) is (are) valid, and there is no cell prepend other than the PHY address if Any-PHY is used.
0	X	X	1	1	0	0	• Cells are transferred from the CSD receive port and a 53/54/54(54/56/56) byte bus. • The content of H5 is output at the far-end, UDF is undefined if present.
1	1	0	0	X	X	0	• Cells are transferred from a 53/53/54(54/54/56) byte bus to the CSD transmit port. • If DHCS=0, H5 is passed transparently. If DHCS=1, it is replaced by the calculated HCS value.
1	0	0	1	X	1	0	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR END DEVICE. • Cells are transferred from a 52/52/53(52/52/54) byte bus to a XX/53/XX(XX/54/XX) byte bus (SCI-PHY slave only). • Neither an address field nor a cell prepend exist. The PHY address is contained in H5 (H5/UDF).
1	1	0	1	X	1	0	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR END DEVICE. • Cells are transferred from a 53/53/54(54/54/56) byte bus to a XX/53/XX(XX/54/XX) byte bus (SCI-PHY slave only). • Near-end H5 (H5/UDF) is stripped. • Neither an address field nor a cell prepend exist. The PHY address is contained in H5 (H5/UDF).
0	X	X	1	X	1	0	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR END DEVICE. • Cells are transferred from the CSD receive port to a XX/53/XX(XX/54/XX) byte bus (SCI-PHY slave only). • Neither an address field nor a cell prepend exist. The PHY address is contained in the H5 (H5/UDF).

Table 20 LVDS Link 58 Byte Cell Configurations

Far-End	Near-End	Resultant Cell contents at far-end Bus or Microprocessor

	input Reg 0x0C			output Reg 0x14			LVDS: both ends must match e.g. Reg 0x40, 0x50 and 0x60
SCIANY	H5UDF	PRELEN[1..0]	SCIANY	H5UDF	INADDUDF	PRELEN[1..0]	DEFAULT CONFIGURATION • 5 system, 6 header bytes, 48 data bytes USRHDR: 5 PREPEND: 0 CELLCRC: 0 • Control cell prepend bytes 2&3 are undefined and header byte 9 bytes are undefined at the far-end microprocessor. Header byte 8 is defined.
1	1	0	1	1	0	0	• Cells are transferred from a 53/53/54(54/54/56) byte bus to a 53/54/54(54/56/56) byte bus. • The content of H5 is output at the far-end, UDF is stripped/undefined if present. There is no cell prepend other than the PHY address if Any-PHY is used.
0	X	X	1	1	0	0	• Cells are transferred from the CSD receive port and a 53/54/54(54/56/56) byte bus. • The content of H5 is output at the far-end, UDF is undefined if present.
1	1	0	0	X	X	0	• Cells are transferred from a 53/53/54(54/54/56) byte bus to the CSD transmit port. • If DHCS=1, H5 is passed transparently. If DHCS=0, it is replaced by the calculated HCS value.
1	0	0	1	X	1	0	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR END DEVICE. • Cells are transferred from a 52/52/53(52/52/54) byte bus to a XX/53/XX(XX/54/XX) byte bus (SCI-PHY slave only). • Neither an address field nor a cell prepend exist. The PHY address is contained in H5 (H5/UDF).
1	1	0	1	X	1	0	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR END DEVICE. • Cells are transferred from a 53/53/54(54/54/56) byte bus to a XX/53/XX(XX/54/XX) byte bus (SCI-PHY slave only). • Near-end H5 (H5/UDF) is stripped. • Neither an address field nor a cell prepend exist. The PHY address is contained in H5 (H5/UDF).
0	X	X	1	X	1	0	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR END DEVICE. • Cells are transferred from the CSD receive port and a XX/53/XX(XX/54/XX) byte bus (SCI-PHY slave only). • Neither an address field nor a cell prepend exist. The PHY address is contained in H5 (H5/UDF).

Table 21 LVDS Link 57 Byte Cell Configurations

Far-End			Near-End				Resultant Cell contents at far-end Bus or Microprocessor
	Reg 0x0C			Reg 0x14			LVDS: both ends must match e.g. Reg 0x40, 0x50 and 0x60
SCIANY	H5UDF	PRELEN[1..0]	SCIANY	H5UDF	INADDUDF	PRELEN[1..0]	DEFAULT CONFIGURATION • 5 system, 6 header bytes, 48 data bytes USRHDR: 4 PREPEND: 0 CELLCRC: 0 • Control cell prepend bytes 2&3 and header bytes 8&9 are undefined at far-end microprocessor.
1	1	0	1	1	0	0	• Cells are transferred from a 53/53/54(54/54/56) byte bus to a 53/54/54(54/56/56) byte bus. • H5 (H5/UDF) exists but is undefined at the far end bus. There is no cell prepend other than the PHY address if Any-PHY is used.
1	0	0	1	0	0	0	• Cells are transferred from a 52/52/53(52/52/54) byte bus to a 52/52/53(52/52/54) byte bus. • There is no cell H5 (H5/UDF) or prepend other than the PHY address if Any-PHY is used.
0	X	X	1	1	0	0	CAN NOT BE USED FOR CLOCKED SERIAL DATA CLEAR CHANNEL MODE • Cells are transferred from the CSD receive port to a 53/54/54(54/56/56) byte bus. • H5 (H5/UDF) is undefined at the far end.
1	1	0	0	X	X	0	CAN NOT BE USED FOR CLOCKED SERIAL DATA CLEAR CHANNEL MODE • Cells are transferred from a 53/53/54(54/54/56) byte bus to the CSD transmit port. • H5 is not transported and must be generated at the transmit interface (DHCS=0).
1	0	0	1	X	1	0	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR-END DEVICE. • Cells are transferred from a 52/52/53(52/52/54) byte bus to a XX/53/XX(XX/54/XX) byte bus (SCI-PHY slave only). • Neither an address field nor a cell prepend exist. The PHY address is contained in H5 (H5/UDF).
1	1	0	1	X	1	0	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR-END DEVICE. • Cells are transferred from a 53/53/54(54/54/56) byte bus to a XX/53/XX(XX/54/XX) byte bus (SCI-PHY slave only). • Near-end H5 (H5/UDF) is stripped. • Neither an address field nor a cell prepend exist. The PHY address is contained in H5 (H5/UDF).

0	X	X	1	X	1	0	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR END DEVICE. CAN NOT BE USED FOR CLEAR CHANNEL MODE • Cells are transferred from the CSD receive port to a XX/53/XX(XX/54/XX) byte bus (SCI-PHY slave only). • Neither an address field nor a cell prepend exist. The PHY address is contained in H5 (H5/UDF).
1	0 or 1	0 or 2	1	1	0	1	• Cells are transferred from a 52 to 58 byte bus to a 54/54/55(56/58/58) byte bus. • At far-end the prepend(s) and H5 (H5/UDF) fields are undefined. Word 0 contains the PHY address in SCI-PHY slave and Any-PHY mode

Table 22 LVDS Link 61 Byte Cell Configurations

Far-End			Near-End				Resultant Cell contents at far-end Bus or Microprocessor
	input Reg 0x0C			output Reg 0x14			LVDS: both ends must match e.g. Reg 0x40, 0x50 and 0x60
SCIANY	H5UDF	PRELEN[1..0]	SCIANY	H5UDF	INADDUDF	PRELEN[1..0]	DEFAULT CONFIGURATION • 5 system, 2 prepend, 6 header and 48 data bytes USRHDR: 6 PREPEND: 1 CELLCRC: 0 • Control cell prepend bytes 2&3 and header bytes 8&9 are valid at far-end microprocessor.
1	1	2	1	1	0	1	NEAR-END IBUS8=1, FAR-END OBUS8=1 • Cells are transferred from a 54/54/55(XX/XX/XX) byte bus to a 54/55/55(XX/XX/XX) byte bus. • Prepend and H5 bytes are valid. NEAR-END IBUS8=1, FAR-END OBUS8=0 • Cells are transferred from a 54/54/55(XX/XX/XX) byte bus to a XX/XX/XX(56/58/58) byte bus. • Prepend MSB and H5 bytes are valid. Prepend LSB and UDF bytes are undefined. NEAR-END IBUS8=0, FAR-END OBUS8=1 • Cells are transferred from a XX/XX/XX(56/56/58) byte bus to a 54/55/55(XX/XX/XX) byte bus. • Prepend and H5 bytes are valid. NEAR-END IBUS8=0, FAR-END OBUS8=0 • Cells are transferred from a XX/XX/XX(56/56/58) byte bus to a XX/XX/XX(56/56/58) byte bus. • Prepends and H5/UDF bytes are valid.
1	1	2	1	1	0	2	THIS CONFIGURATION IS VALID ONLY IF NEAR-END IBUS8=0 AND THE FAR-END OBUS8=1 • Cells are transferred from a 55/55/56(XX/XX/XX) byte bus to a 55/56/56(XX/XX/XX) byte bus. • Prepend (2 bytes) and H5 bytes are valid.
1	1	2	1	1	0	1	THIS CONFIGURATION IS VALID ONLY IF NEAR-END IBUS8=1 • Cells are transferred from a 55/55/56(XX/XX/XX) byte bus to a 54/55/55(56/58/58) byte bus. • Prepend (2 bytes) and H5 bytes are valid. UDF undefined if used.
1	1	1	1	1	0	2	THIS CONFIGURATION IS VALID ONLY IF NEAR-END OBUS8=1 • Cells are transferred from a 54/54/55(56/56/58) byte bus to a 55/56/56(XX/XX/XX) byte bus. • Prepend (2 bytes) and H5 bytes are valid.

Table 23 LVDS Link 59 Byte Cell Configurations with CRC

Far-End	Near-End	Resultant Cell contents at far-end Bus or Microprocessor

	input Reg 0x0C			output Reg 0x14			LVDS: both ends must match e.g. Reg 0x40, 0x50 and 0x60
SCIANY	H5UDF	PRELEN[1..0]	SCIANY	H5UDF	INADDUDF	PRELEN[1..0]	DEFAULT CONFIGURATION • 5 system, 2 prepend, 4 header and 48 data bytes USRHDR: 4 PREPEND: 1 CELLCRC: 1 • Control cell prepend byte 2 is carried as is, but prepend byte 3 is overwritten with the CRC8. Header bytes 8&9 are undefined.
1	1	0	1	1	0	1	• Cells are transferred from a 53/53/54(54/54/56) byte bus to a 54/55/55(56/58/58) byte bus. • At far-end the prepend and H5/UDF fields are all present. The first byte the prepend is undefined, the second byte contains the CRC8 from the previous cell. H5 (H5/UDF) is undefined.
1	X	X	1	1	0	1	• Cells are transferred from the CSD receive port to a 54/55/55(56/58/58) byte bus. • At far-end the prepend and H5/UDF fields are all present. The first byte the prepend is undefined, the second byte contains the CRC8 from the previous cell. H5 (H5/UDF) is undefined
1	1	1	0	X	X	X	• Cells are transferred from a 54/54/55(56/56/58) byte bus to the CSD transmit port.
1	1	0	1	X	1	1	THIS CONFIGURATION IS VALID ONLY IF OMASTER=0 AND OANYPHY=0 AT THE FAR-END. • Cells are transferred from a 53/53/54(54/54/56) byte bus to a XX/54/XX(XX/56/XX) byte bus (SCI-ANY slave only). • At far-end the prepend(s) and H5(H5/UDF) fields are all present. The first byte the prepend is undefined, the second byte (OBUS8=0) contains the CRC8 from the previous cell. • At far-end the H5 (H5/UDF) field contains the PHY address.

12.3 Maximum Cell Bit Rate

The maximum cell bit rate transferred over the LVDS link is a function the LVDS bit rate and the ratio of transport overhead (system prepend & unused user defined field) versus cell data. Since the system prepend is fixed at 5 bytes, the absolute maximum throughput is achieved when the cell length is 56 bytes, i.e. the transported cells included 2 prepend bytes, H5 and UDF.

$Ratio_{max}$ = 56/61 = 91.8%, $CellBR_{max}$ = 91.8% * 200 = 183.6 Mb/s

$Ratio_{min}$ = 52/61 = 85.2%, $CellBR_{min}$ = 85.2% * 200 = 170.5Mb/s

In addition to the LVDS stream capacity, the total Clocked Serial Data interface throughput is limited by the aggregate number of clock actives edges of all lines in each direction, independently of the idle and discarded cells. The instantaneous aggregate bit rate of all clocked serial data receive lines (including idle and discarded cells) has to be equal or less than the LVDS bit rate.

12.4 Minimum Programming

Besides the bus configuration described in the previous section, very little configuration is required to make the part function. The S/UNI-DUPLEX can operate in SCI-PHY/Utopia master mode or in Clocked Serial Data without external intervention. In addition to the registers described below, the following bit is commonly modified:

1. MINTE bit of the Master Configuration register (0x001) – This bit must be logic 1 to enable interrupt servicing. If MINTE is logic 0, the INTB output will be unconditionally high-impedance. Note that individual interrupt sources must enabled in addition to setting MINTE.

The following three sections apply when operating the S/UNI-DUPLEX in parallel bus mode (SCIANY=1).

12.4.1 SCI-PHY/Utopia Master Mode

Although the default setting allows cell traffic to go, system performances may be improved by modifying the following registers.

1. PHYID[5:0] bits SCI-PHY/Any-PHY Input Configuration 2 and SCI-PHY/Any-PHY Output Polling Range registers (0x0D, 0x15) – These bits are used to define the polling range of the SCI/PHY/Any-PHY input and output interface.

2. Input Cell Available Enable registers (0x10, 0x11, 0x12 and 0x13) – These registers can be used to dynamically remove PHYs from in the input port polling list. Setting a bit of these registers to logic 0 removes the corresponding PHY ID from the polling list.

12.4.2 SCI-PHY Slave

1. Output Address Match register (0x0A) – This register is used to set the proxy PHY ID for selection and transfer of cells on the SCI-PHY/Any-PHY output interface.

2. OCAEN bit of the Master Configuration register (0x001) – This bit must be a logic 1 before the OCA output responds to polling.

12.4.3 Any-PHY Slave

In addition to the register required for the SCI-PHY slave, the following registers may need to be set at configuration

1. Extended Address Match and Extended Address Mask registers (0x06, 0x07, 0x08 and 0x09) – These registers are used to define the base address of the ANY-PHY input port. Cells are accepted by the S/UNI-DUPLEX if the value in the Extended Address field of Word 0 agrees with the Extended Address Match registers over the range of bits specified by the Extended Address Mask registers. The value of the Extended Address Match registers content is also appended to the PHY ID of cells output on the Any-PHY output port.

12.4.4 Clocked Serial Data Interface

This sections applies when operating the S/UNI-DUPLEX in clocked serial data mode (SCIANY=0).

1. LTXCINV and LRXCINV of Master Configuration register (0x01)– Select the active edge of the receive and transmit serial clocks. The falling edge of LTXC[15:0] is used when to LTXCINV is set to logic 1. The falling edge of LRXC[15:0] is used when to LRXCINV is set to logic 1.

2. Transmit Logical Channel FIFO Depth register (0x5C) – This register control the DEPTH of the FIFO associated with cell traffic output on the LVDS links. By default, the FIFO is configured as a 32x2 cell FIFO to support the parallel bus configuration. The FIFO can be reconfigured as 16x4 cell FIFO by writing a value of 04 in register 0x5C. This maximizes system performances by allowing longer traffic bursts at the Clocked Serial Data receive interface.

3. DDELIN bit of the Receive Serial Indirect Channel Configuration register (0x69) and DHCS bit of the Transmit Serial Indirect Channel Data register (0x71) – These bits allow carrying raw data (arbitrary stream format) through the Clocked Serial Data interface. When DDELIN is set to logic 1, the RTTC does not perform any processing on the incoming stream, but passes data through transparently. Similarly when DHCS is logic 1, the fifth byte of the cell passes through the Clocked Serial Data transmit port unmodified. Both bits are written and read through indirect access by first selecting the serial channel by writing the CHAN[3:0] bits to the Receive Serial Indirect Channel (0x68)Select or the Transmit Serial Indirect Channel Select (0x70). Writing a logic 0 to CRWB of the same registers triggers an indirect write operation. Writing a logic 1 to CRWB of the same registers triggers an indirect read operation.

4. ALIGN bit of the Transmit Serial Alignment Control register (0x74) – This bit allows ATM/DATA octet alignment to frame boundaries based on recognizing gaps in the transmit serial clock. When this bit is set to logic 1, the ATM /Data octets are aligned to the inferred frame alignment, with the most significant bit output first during the clock gap on all sixteen transmit channels.

12.4.5 Redundant Link Management

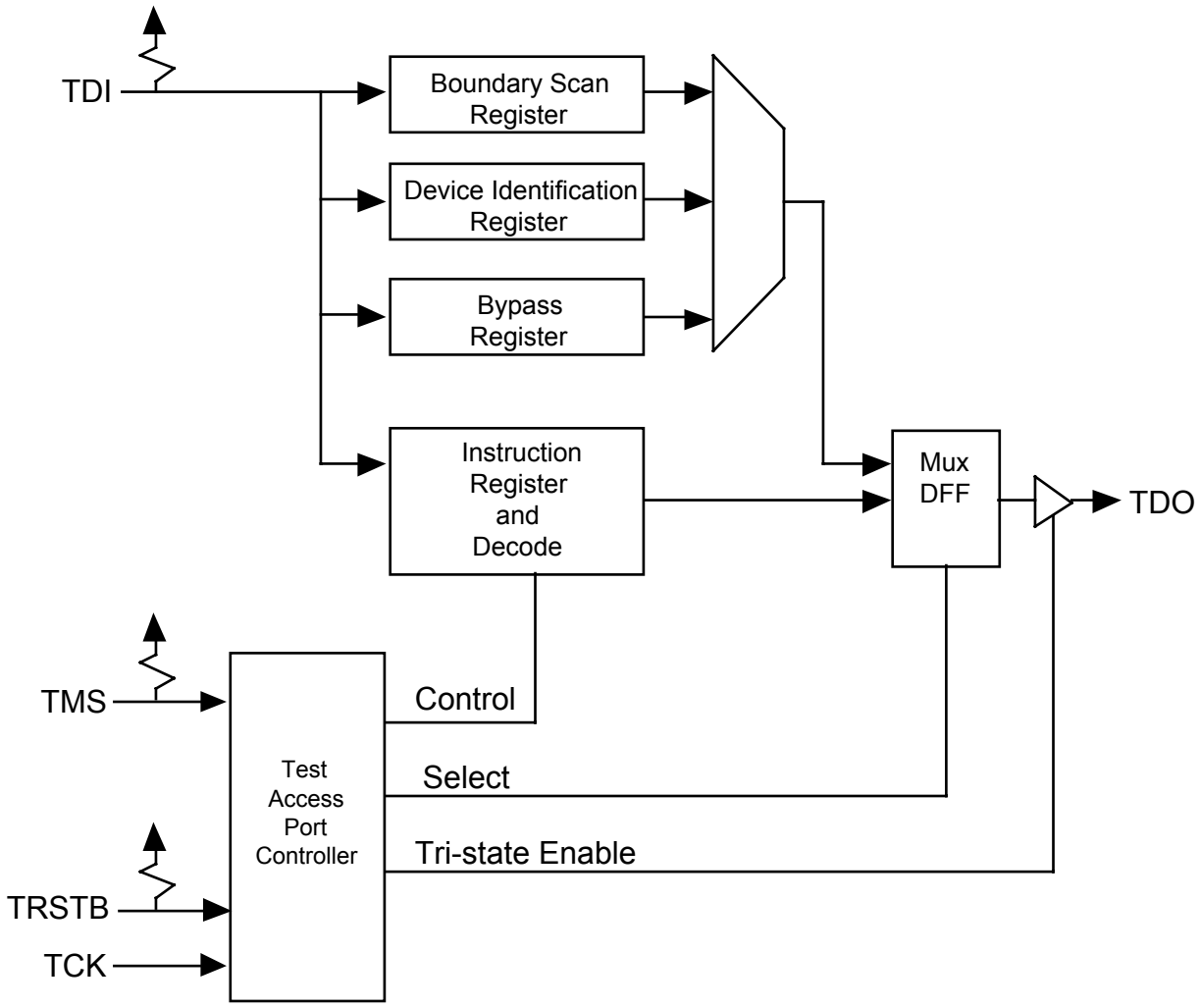
Upon power up, the S/UNI-DUPLEX is configured to automatically select the active LVDS link based on the value of the ACTIVE bit extracted from the LDVS receive links. It is also possible to externally control the selection process with the following register bits.

1. RXAUTOSEL and ACTIVE bits of the Master Configuration register (0x01) – When RXAUTOSEL is set to logic 1 (default value) the active LVDS serial link selection is done based on the value of the ACTIVE bit extracted from the receive high-speed data streams. When RXAUTOSEL is set tot logic 0, the active LVDS serial link is determined by the value of the ACTIVE bit. A logic 0 sets the link 1 (RXD1+/-) active, a logic 1 sets the link 2 (RXD2+/-) active. Since link switching is performed on cell boundaries, a delay may happen between writing a new ACTIVE bit value and reading back its value.

12.5 JTAG Support

The S/UNI-DUPLEX supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standard. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Fig. 16.

Fig. 16 Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

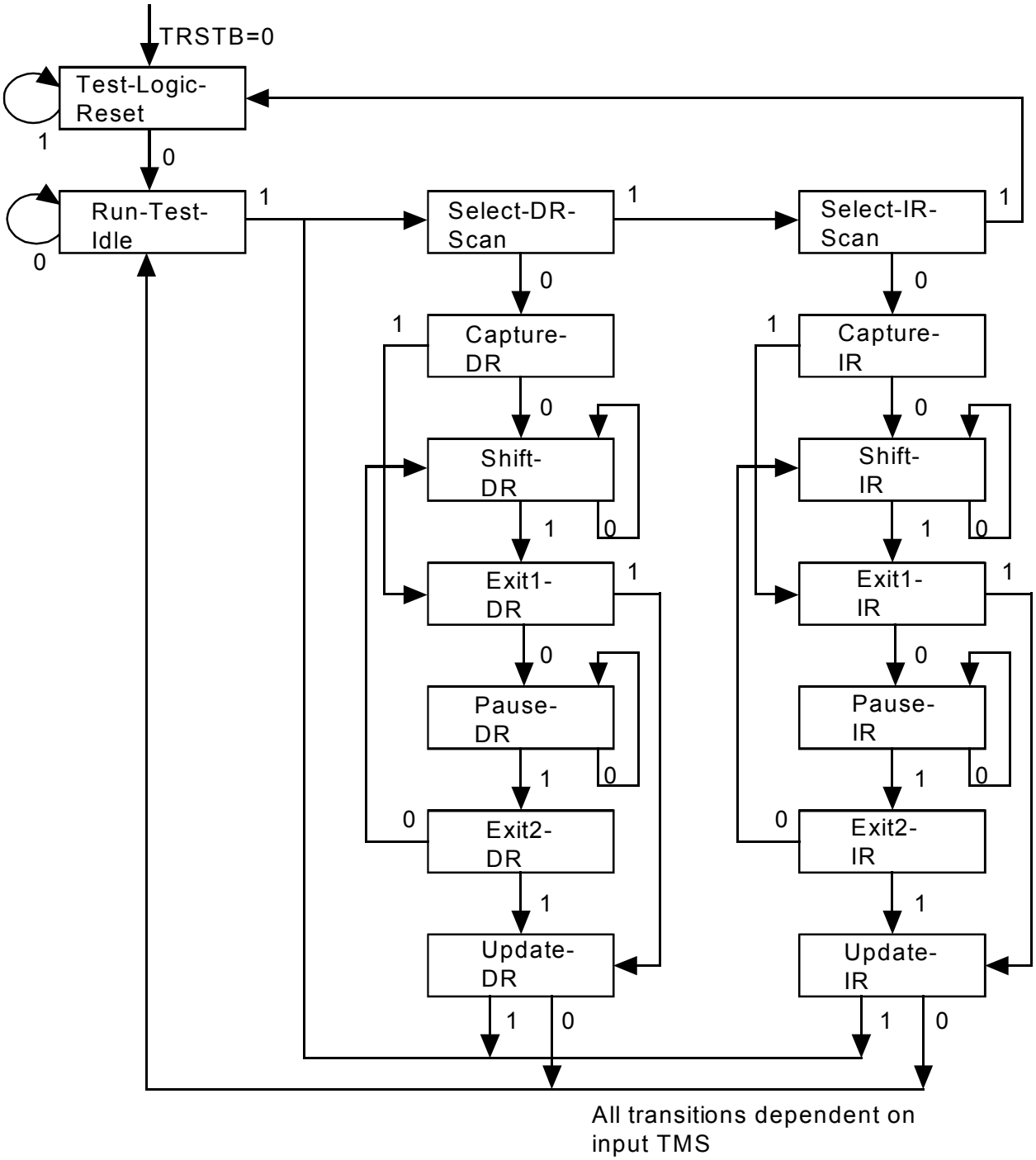
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be

sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is illustrated in Fig. 17.

Fig. 17 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

12.5.1 Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13 FUNCTIONAL TIMING

While the following diagrams present representative waveforms, they are not an attempt to unambiguously describe the interfaces. The Pin Description is intended to denote the detailed pin behavior and constraints on use.

13.1 SCI-PHY/Any-PHY Interface

Fig. 18 is an example of the functional timing of the SCI-PHY/Any-PHY Interface when configured as a 16-bit SCI-PHY Level 2 compliant input bus slave. “A”, “B”, “C” and “D” represent any arbitrary address values out of the 32 possible SCI-PHY addresses. Since up to 32 PHY devices can reside on the SCI-PHY bus, the bus master can poll PHY “1Fh”, provided that IAVALID signal is used. The polls of logical channels “B” and “C” illustrate that polls in consecutive cycles are permitted.

Once a logic high is returned on ICA in response to a poll, a cell may be transferred. The transfer can be paused by deasserting IENB. The logical channel “A” is reselected before the transfer resumes.

Fig. 18 SCI-PHY Interface, Input Bus Slave Transfer Timing

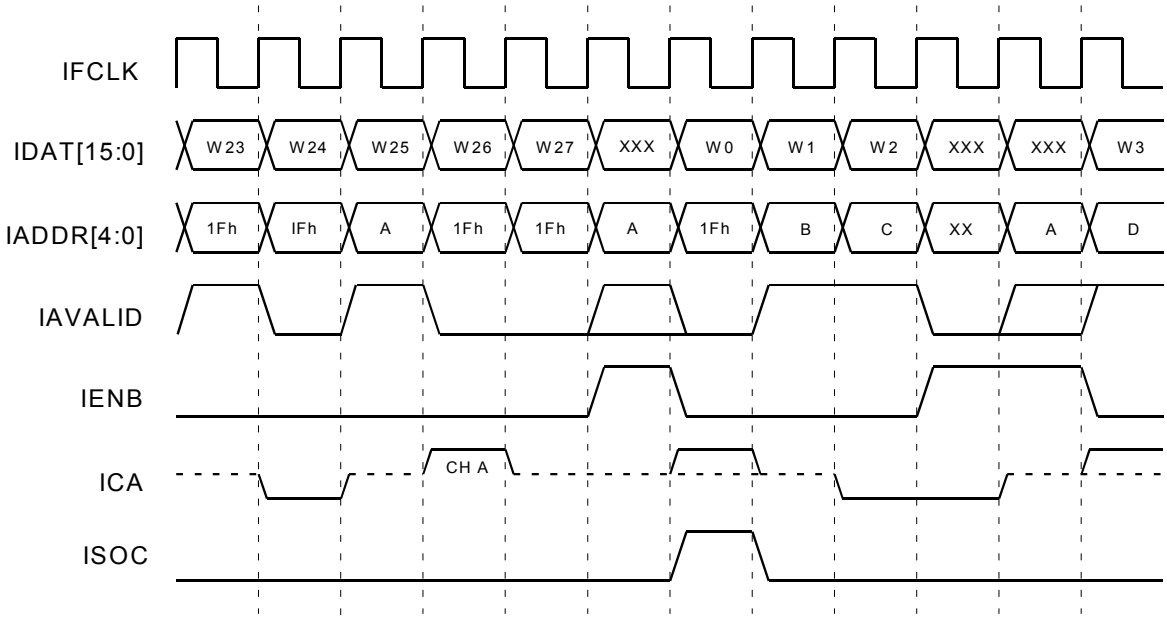


Fig. 19 gives an example of the functional timing of the SCI-PHY/Any-PHY Interface when configured as a 16-bit SCI-PHY Level 2 compliant input bus master. When polling PHY devices, the S/UNI-DUPLEX inserts null cycles by deasserting the IAVALID output and forcing the IADDR[4:0] bus to “1Fh” to prevent bus contention. Once a ready to transfer PHY is found (PHY at address “C” in this example), its address is maintained on the address bus till the current transfer is completed. The PHY is then selected and the transfer initiated. The S/UNI-DUPLEX transfers the complete cell without pause.

Fig. 19 SCI-PHY Interface, Input Bus Master Transfer Timing

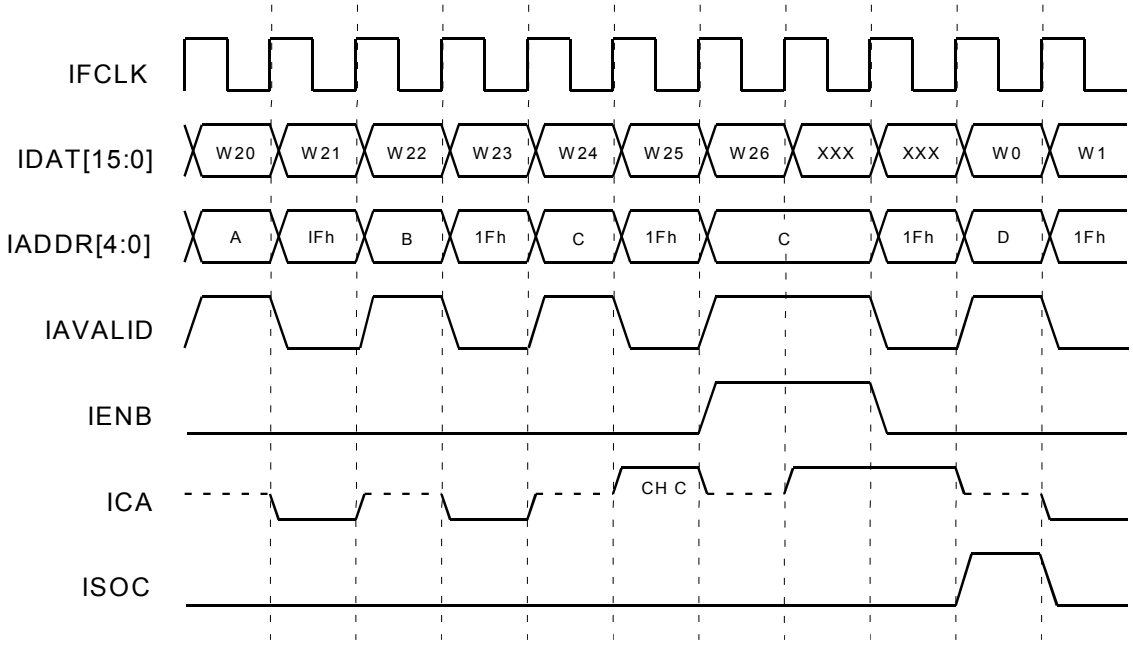


Fig. 20 gives an example of the functional timing of the of the SCI-PHY/Any-PHY Interface when configured as a 16-bit Any-PHY compliant input bus slave. In this example, the IAVALID pin is used as the IADDR[5] line of the IADDR[5:0] bus (the null address becomes 3Fh) and the Extended Address register is unused.The polls of logical channels “A”, “B” and “C” illustrate that polls in consecutive cycles are permitted. The S/UNI-DUPLEX responds to polling of logical channel “D” by asserting ICA high on the second following clock cycle. Logical channel “D” is selected by the bus master assertion of ISX and a cell transfer is initiated. The IENB input is not required to be deasserted at the end of a cell transfer. Upon completion of the cell transfer, the interface autonomously deselects itself.

The transfer can be paused by deasserting IENB. The cell transfer from the same logical channel resumes immediately when IENB is reasserted low.

Fig. 20 Any-PHY Interface, Input Bus Slave Transfer Timing

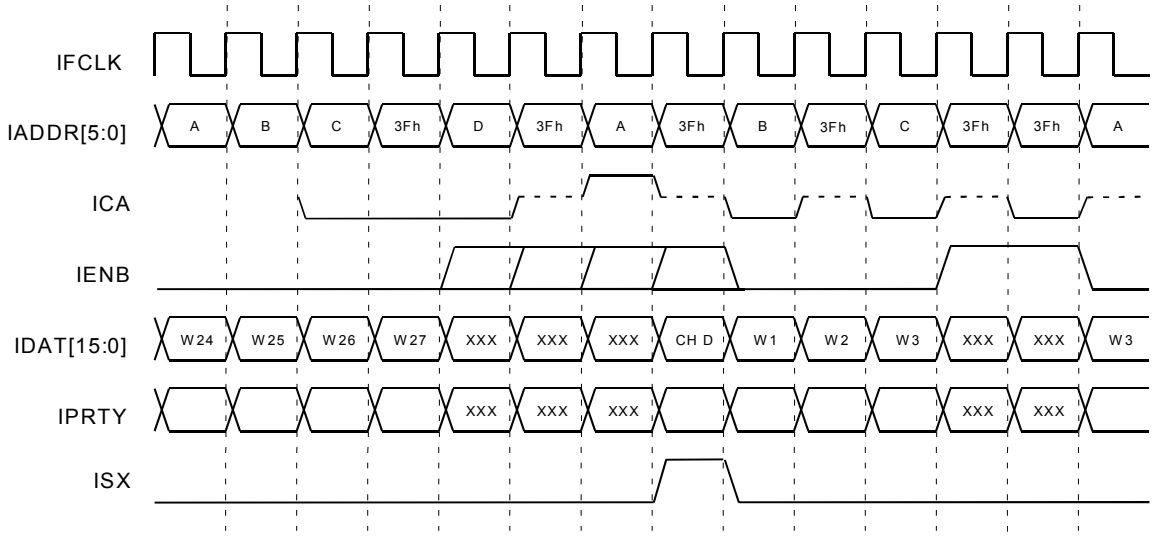


Fig. 21 is an example of the functional timing of the SCI-PHY/Any-PHY Interface when configured as a 8-bit SCI-PHY Level 2 compliant output bus slave. In this example, address “A” corresponds to the content of the Output Address Match register of the S/UNI-DUPLEX. The SCI-PHY/Any-PHY Output Interface acts a proxy for its 32 logical channels. Once it returns a logic high on OCA in response to a poll, a cell may be transferred. The logical channel ID is output as the first word of the cell, its most significant bits derived from the contents of the Extended Address Match registers.

The transfer can be paused by deasserting OENB. The interface must be reselected before the transfer can resume.

Fig. 21 SCI-PHY Interface, Output Bus Slave Transfer Timing

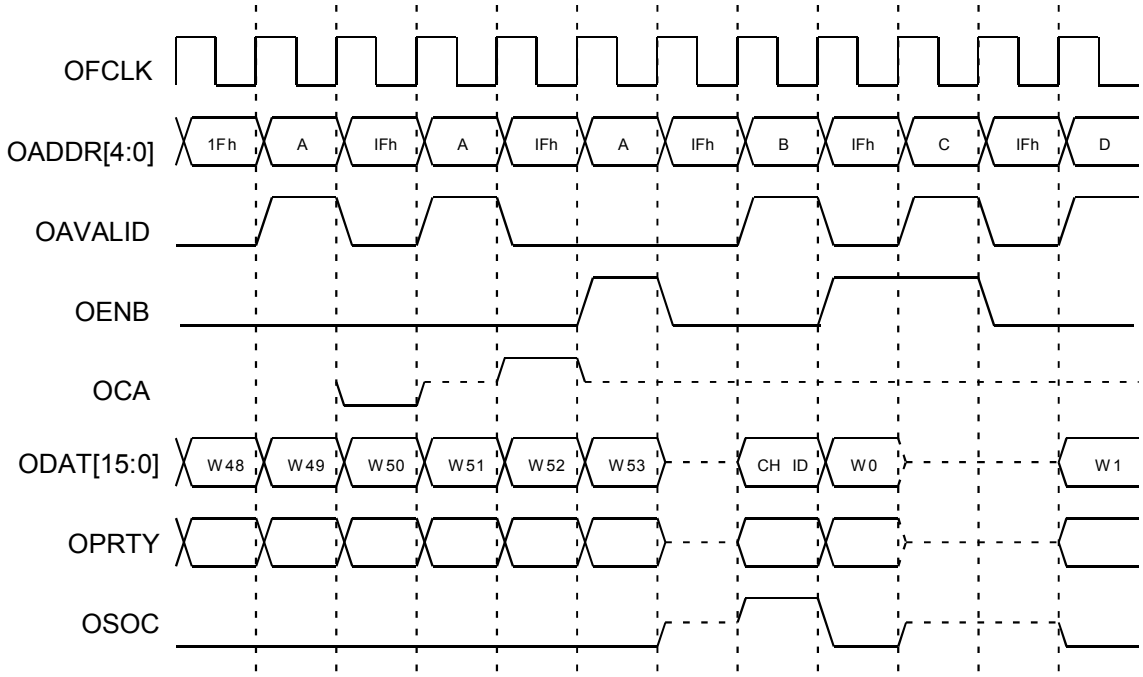


Fig. 22 is an example of the functional timing of the SCI-PHY/Any-PHY Interface when configured as a 8-bit Utopia Level 2 compliant output bus master. The S/UNI-DUPLEX polls PHY devices round robin with OADDR[4:0] and OAVALID while performing a cell transfer. The PHY at address “A” responds to polling by asserting OCA high. Because of internal processing delays of the S/UNI-DUPLEX interface, the polling process stops only after the address of next PHY of the round robin sequence is set on the bus. IADDR[4:0] value is reverted to the preceding polled PHY address until the cell transfer is completed. The S/UNI-DUPLEX selects PHY “A” for a cell transfer and resumes the round robin polling process.

Fig. 22 SCI-PHY Interface, Output Bus Master Transfer Timing

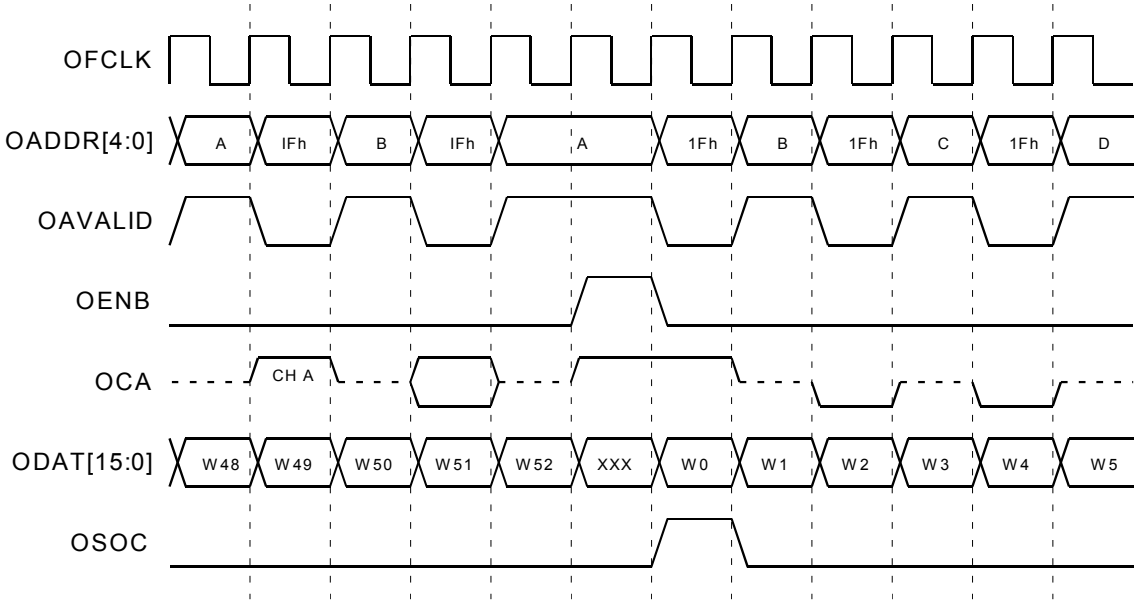
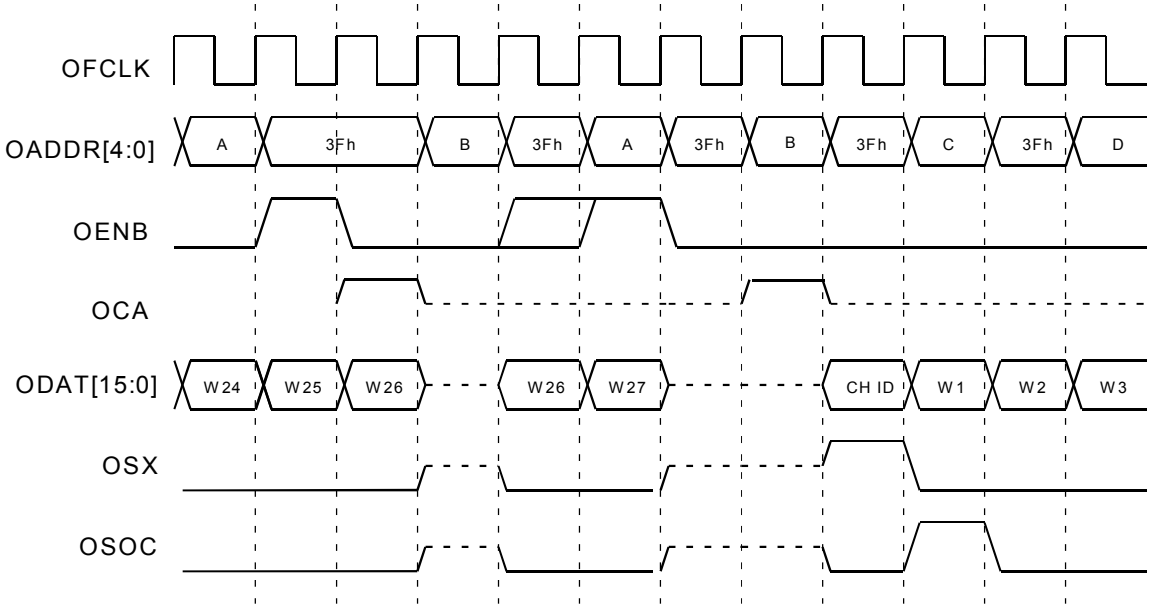


Fig. 23 is an example of the functional timing of the SCI-PHY/Any-PHY Interface when configured as a 16-bit Any-PHY compliant output bus slave. In this example, address “A” (since the Output Address Match register is 5 bit wide, the most significant bit is ignored) corresponds to the content of the Output Address Match register of the S/UNI-DUPLEX. In this example, OAVALID is used as the OADDR[5] line. OAVALID has to be logic low for a match to occur. The SCI-PHY/Any-PHY output interface acts a proxy for its 32 logical channels. Once it returns a logic high on OCA in response to a poll, a cell may be transferred. Coincident with the OSX output, the logical channel ID is output as the first word of the cell, its most significant bits derived from the contents of the Extended Address Match registers. The OENB input is not required to be deasserted at the end of a cell transfer. Upon completion of the cell transfer, the interface autonomously deselects itself.

The transfer can be paused by deasserting OENB. The cell transfer from the same logical channel resumes immediately when OENB is reasserted low.

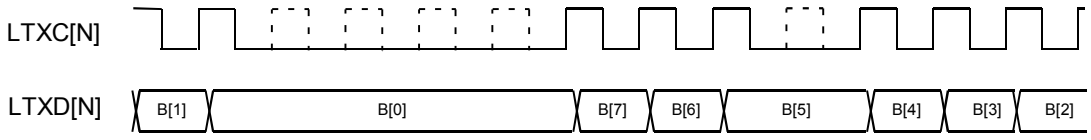
Fig. 23 Any-PHY Interface, Output Bus Slave Transfer Timing



13.2 Clocked Serial Data Interface

The timing relationship of the transmit clock (LTXC[N]) and data (LTXD[N]) signals is shown in Fig. 24. The transmit data is viewed as a contiguous serial stream. Data bytes are transmitted from most significant bit to least significant bit. Bits are updated on the rising or falling edge of LTXC[N], as determined be the value of the LTXCINV bit of the Master Configuration register (in Fig. 24, LTXCINV is set to logic 0). A transmit link may be stalled by holding the corresponding LTXC[N] low.

Fig. 24 Clocked Serial Data Transmit Interface



When the ALIGN bit of the Transmit Serial Framing Bit Threshold register is set to logic 1, a clock gap longer that the minimum detectable period causes the most significant bit of the data octet to be output during the gap period. The S/UNI-DUPLEX can detect clock gaps of 8 line clock periods over the entire LTXC[15:0] clock line frequency range. The range of the frequency at which 1 bit framing gap can be detected changes linearly with the speed of the high-speed links. When operating the LVDS link at 200 Mb/s (REFCLK frequency set to 25 MHz), the S/UNI-DUPLEX will detect one bit clock gap for line frequency range of 200 kHz to 8 MHz.

To be detected, the gap polarity must match the value of the LTXCINV bit of the Master Configuration register. When the rising edge of clock signals on LTXC[15:0] is used to output the data (LTXCINV set to logic 0), gaps during which the clock is forced to logic 0 are detected. In Fig. 25, bits are byte aligned to a 1 bit clock gap. When the falling edge of the clock signals on LTXC[15:0] are used to output the data (LTXCINV set to logic 1), gaps during which the clock is forced to logic 1 are detected. In Fig. 26, bits are output on the falling edge of the byte aligned to an 8 bit clock gap.

Fig. 25 Clocked Serial Data Transmit Interface, 1 Bit Gap

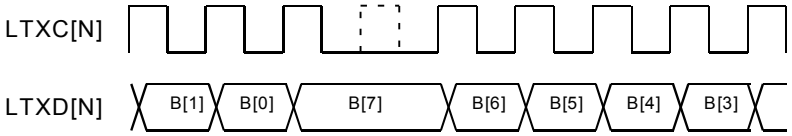
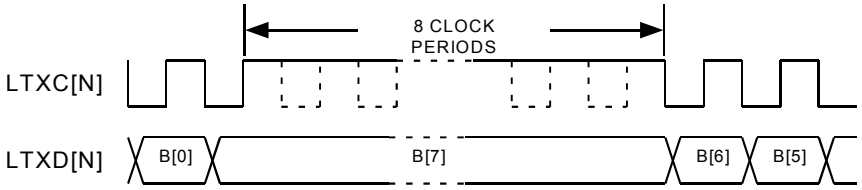
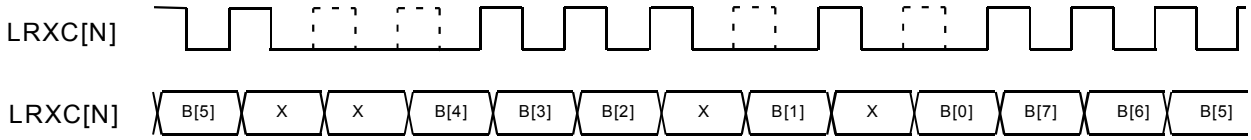


Fig. 26 Clocked Serial Data Transmit Interface, 8 Bit Gap



The timing relationship of the receive clock (LRXC[N]) and data (LRXD[N]) signals is shown in Fig. 27. The receive data is viewed as a contiguous serial stream, with the most significant bit of the ATM/Data byte received first. Bits that are to be processed are clocked in either on the rising or falling edge of LRXC[N], determined by the value of the LRXCINV bit of the Master Configuration register. In Fig. 27, the rising edge of LRXC[N] is used. Bits that should be ignored ("X" in Fig. 27) are squelched by holding LRXC[N] low. When ATM cells are received, the S/UNI Duplex performs cell delineation on the received bits to recover byte alignment.

Fig. 27 Clocked Serial Data Receive Interface



14 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Case Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C

15 D.C. CHARACTERISTICS

T_A = -40°C to +85°C, V_{DD} =3.3 V ±10%

(Typical Conditions: T_C = 25°C, V_{DD} = 3.3 V)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	3	3.3	3.6	Volts	
V_{BIAS}	5 V Tolerant Bias	VDD	5.0	5.5	Volts	
V_{IL}	Input Low Voltage (TTL Only)	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{BIAS} +0.5	Volts	Guaranteed Input HIGH Voltage for, A[8:0], RDB, WRB, CSB, ALE, D[7:0], TX8K, REFCLK, TDI, TCK and TMS,
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage for IENB, IADDR[4:0], IAVALID, IDAT[15:0], ISOC, ISX, ICA, IPRTY, IFCLK, OENB, OADDR[4:0], OAVALID, OCA, OFCLK, IANYPHY, OANYPHY, IMASTER, OMASTER, IBUS8, OBUS8, LRXD[15:0], LRXC[15:0], LTXC[15:0] and SCIANY.
V_{OL}	Output or Bidirectional Low Voltage (TTL Only)		0.1	0.4	Volts	V_{DD} = min, I_{OL} = -2 mA minimum. Note 3
V_{OH}	Output or Bidirectional High Voltage (TTL Only)	2.4	3.0		Volts	V_{DD} = min, I_{OH} = 2 mA minimum. Note 3

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{T+}	Reset Input High Voltage	2.0		V_{BIAS} +0.5	Volts	TTL Schmitt for RSTB and TRSTB
V_{T-}	Reset Input Low Voltage			0.8	Volts	RSTB and TRSTB
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	RSTB and TRSTB

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{ICM}	LVDS Input Common-Mode Range	0		2.4	V	
$\|V_{IDM}\|$	LVDS Input Differential Sensitivity			100	mV	
$\|V_{HYST}\|$	LVDS Input Differential Hysteresis	25			mV	
R_{IN}	LVDS Differential Input Impedance	10			KΩ	
V_{LOH}	LVDS Output voltage high		1375	1475	mV	R_{LOAD}=100Ω ±1%
V_{LOL}	LVDS Output voltage low	925	1025		mV	R_{LOAD}=100Ω ±1%
V_{ODM}	LVDS Output Differential Voltage	250	350	400	mV	R_{LOAD}=100Ω ±1% Note 5
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Single-Ended	70		130	Ω	V_{CM}=1.0V and 1.4V
ΔR_O	LVDS Output Impedance Mismatch between TXOP and TXON			10	%	V_{CM}=1.0V and 1.4V
$\|\Delta V_{ODM}\|$	Change in $\|V_{ODM}\|$ between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
ΔV_{OCM}	Change in V_{OCM} between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
I_{SPN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together
I_{ILPU}	Input Low Current	+20	+83	+200	µA	V_{IL} = GND. Notes 1, 3
I_{IHPU}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$. Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$. Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
I_{DDOP}	Operating Current Processing Cells			450	mA	V_{DD} = 3.6 V, Outputs Unloaded, RXD1+/-, RXD2+/-, TXD1+/- and TXD2+/-200 Mb/s OFCLK = IFCLK = 52 MHz Note 4

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.

2. Input pin or bi-directional pin without internal pull-up resistor

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

4. When IMASTER = OMASTER = 0 and SCIANY = 1. OFCLK = IFCLK = 33 MHz when IMASTER = OMASTER = 1.

5 When the device is in reset, the differential voltage is approximately 80 mV. Once the device is out of reset, the voltage returns to the normal level.

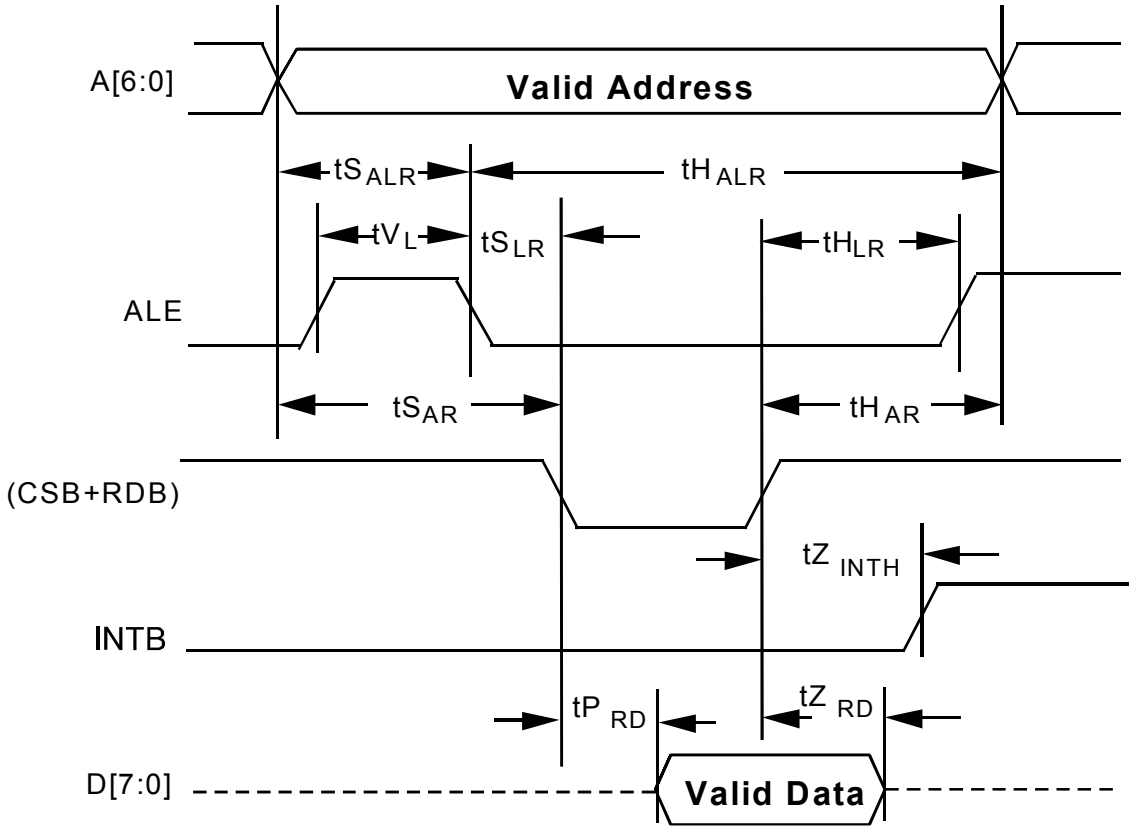
16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 3.3 V ±10%)

Microprocessor Interface Read Access (Fig. 28)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Fig. 28: Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

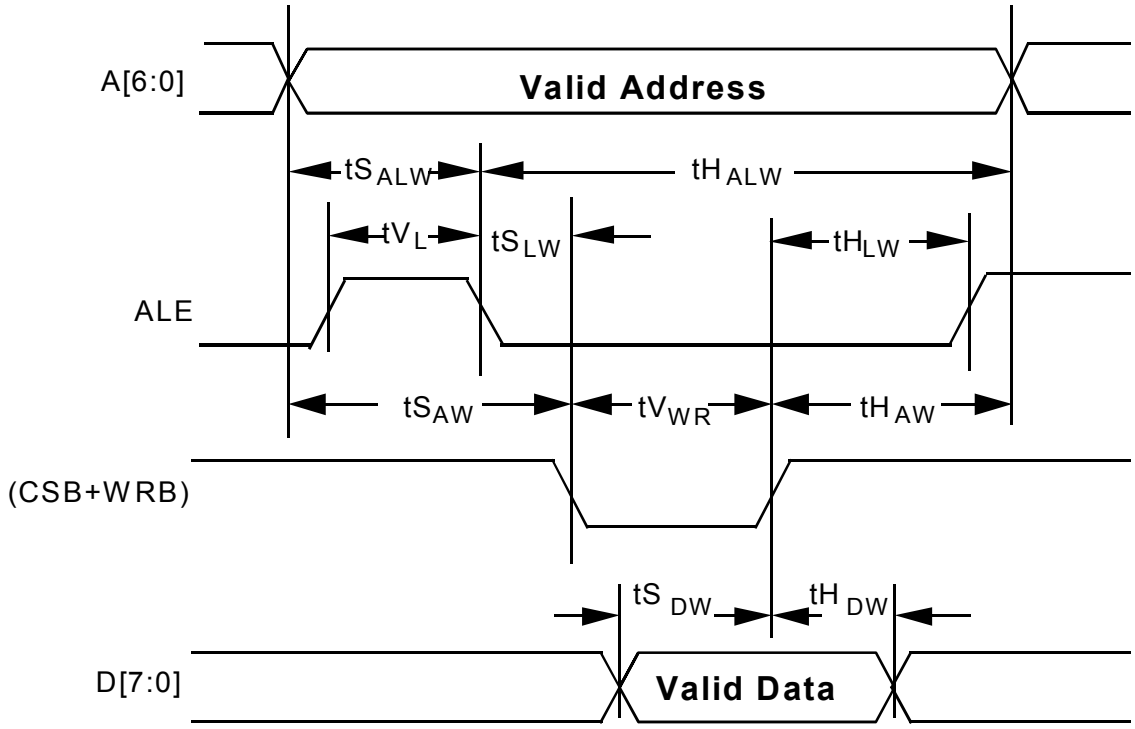
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Microprocessor Interface Write Access (Fig. 29)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 29: Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2 In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

3 Parameter tH_{AW} is not applicable if address latching is used.

4 When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5 When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

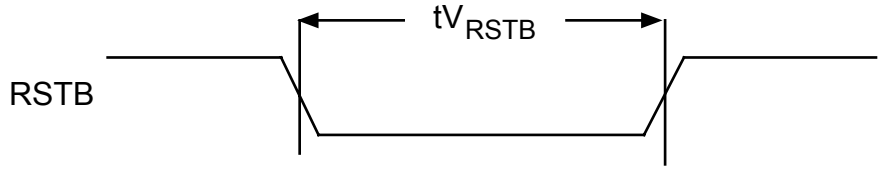
17 A.C. TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 3.3 V ±10%)

RSTB Timing (Fig. 30)

Symbol	Parameter	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Fig. 30: RSTB Timing



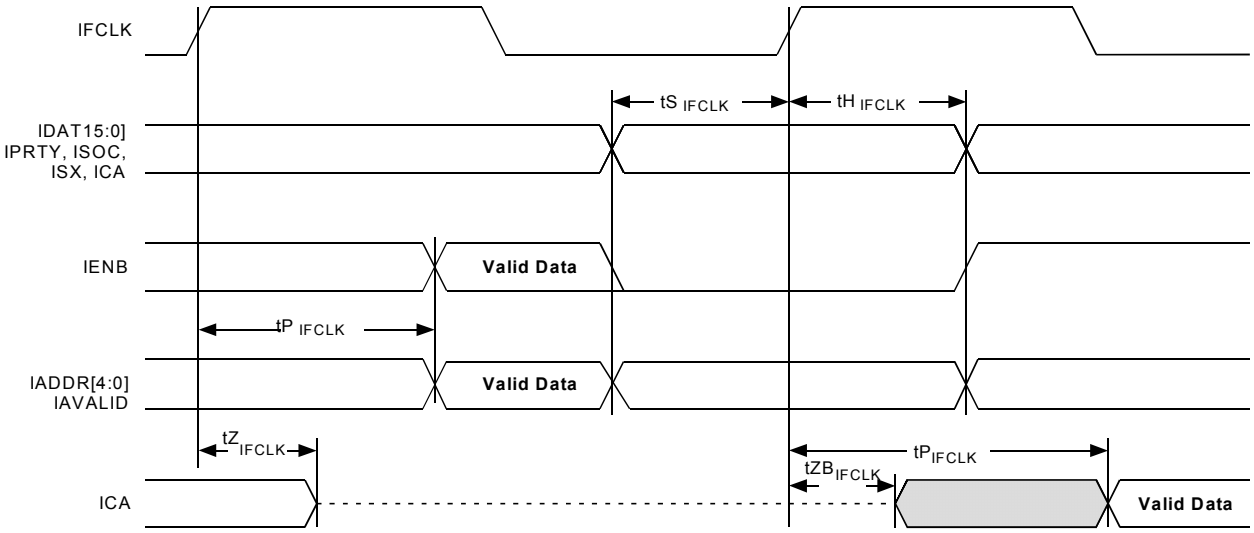
REFCLK Timing

Symbol	Parameter	Min	Max	Units
f_{REFCLK}	REFCLK Frequency	12.5	25	MHz
D_{REFCLK}	REFCLK Duty Cycle	20	80	%
	REFCLK Frequency Tolerance		100	ppm

Ingress SCI-PHY/Any-PHY Interface (Fig. 31)

Symbol	Description	Min	Max	Units
	IFCLK Frequency (IMASTER = 0)	0	52	MHz
	IFCLK Frequency (IMASTER = 1)	0	33	MHz
	IFCLK Duty Cycle	40	60	%
tS_{IFCLK}	IDAT[15:0], IADDR[4:0], IPRTY, ISOC, IENB, IAVALID, ISX and ICA Set-up time to IFCLK	3		ns
tH_{IFCLK}	IDAT[15:0], IADDR[4:0], IPRTY, ISOC, IENB, IAVALID, ISX and ICA Hold time to IFCLK	1		ns
tP_{IFCLK}	IFCLK High to IENB, IADDR[4:0], IAVALID and ICA Valid	2	12	ns
tZ_{IFCLK}	IFCLK High to ICA High Impedance	2	12	ns
tZB_{IFCLK}	IFCLK High to ICA Driven	0		ns

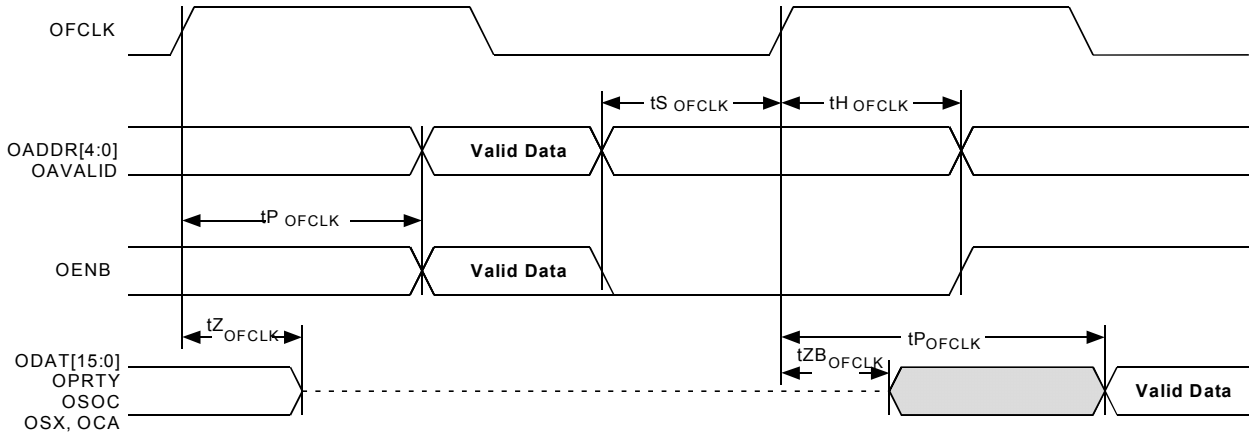
Fig. 31: Ingress SCI-PHY/Any-PHY Interface Timing



Egress SCI-PHY/Any-PHY Interface (Fig. 32)

Symbol	Description	Min	Max	Units
	OFCLK Frequency (OMASTER = 0)	0	52	MHz
	OFCLK Frequency (OMASTER = 1)	0	33	MHz
	OFCLK Duty Cycle	40	60	%
tS_{OFCLK}	OCA, OENB, OADDR[4:0] and OAVALID Set-up time to OFCLK	3		ns
tH_{OFCLK}	OCA, OENB, OADDR[4:0] and OAVALID Hold time to OFCLK	1		ns
tP_{OFCLK}	OFCLK High to OSOC, ODAT[15:0] OPRTY, OENB, OADDR[4:0], OAVALID and OCA Valid	2	12	ns
tZ_{OFCLK}	OFCLK High to Output High Impedance	2	12	ns
tZB_{OFCLK}	OFCLK High to Driven	0		ns

Fig. 32: Egress SCI-PHY/Any-PHY Interface Timing

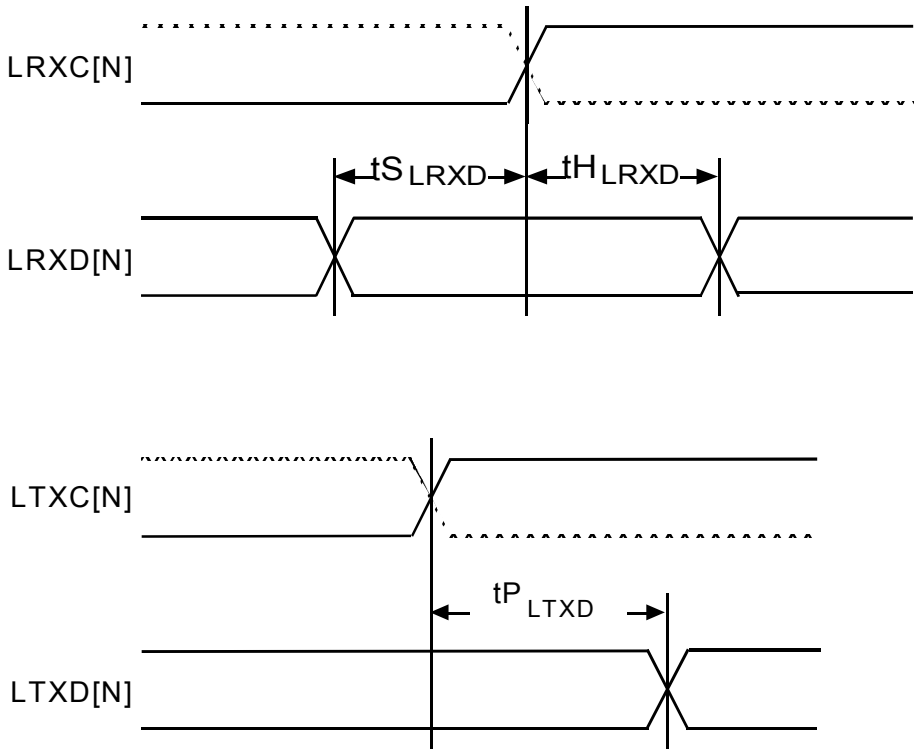


Clocked Serial Data Interface (Fig. 33)

Symbol	Description	Min	Max	Units
	LTXC[N], LRXC[N] Frequency		52	MHz
	LTXC[N], LRXC[N] Duty Cycle	40	60	%
tS_{LRXD}	LRXD[N] Set-up Time to LRXC[N] (see note)	8		ns
tH_{LRXD}	LRXD[N] Hold Time to LRXC[N] (see note)	5		ns
tP_{LTXD}	LTXC[N] to LTXD[N] Valid (see note)	1	13	ns

Note:
Polarity of the active edge of LTXC[N] and LRXC[N] is determined by the respective value of the LRXCINV and LTXCINV bits in the Master Configuration register.

Fig. 33: Clocked Serial Data Interface



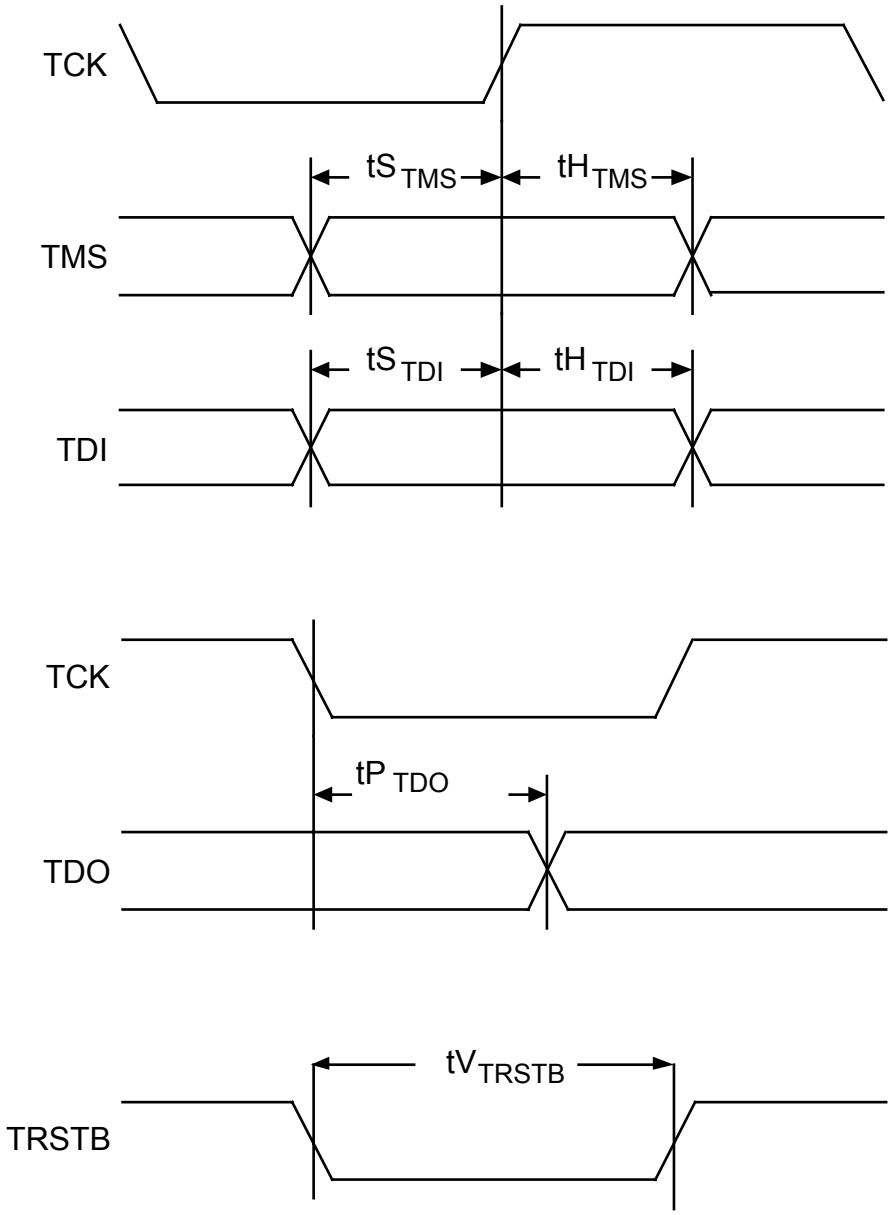
High-Speed Serial Interface

Symbol	Description	Min	Max	Units
	RXD1+/-, RXD2+/- Bit Rate	$8f_{REFCLK}$ -100ppm	$8f_{REFCLK}$ +100ppm	Mb/s
t_{FALL}	V_{ODM} fall time, 20%-80%	300	700	ps
t_{RISE}	V_{ODM} rise time, 20%-80%	300	700	ps
t_{SKEW}	Differential Skew		50	ps

JTAG Port Interface (Fig. 34)

Symbol	Description	Min	Max	Units
	TCK Frequency		4	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns
tV_{TRSTB}	TRSTB Pulse Width	100		ns

Fig. 34: JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs with the exception of the LTXD[15:0], RX8K, RCLK outputs. The LTXD[15:0], RX8K, RCLK output propagation delays are measured with a 20 pF load

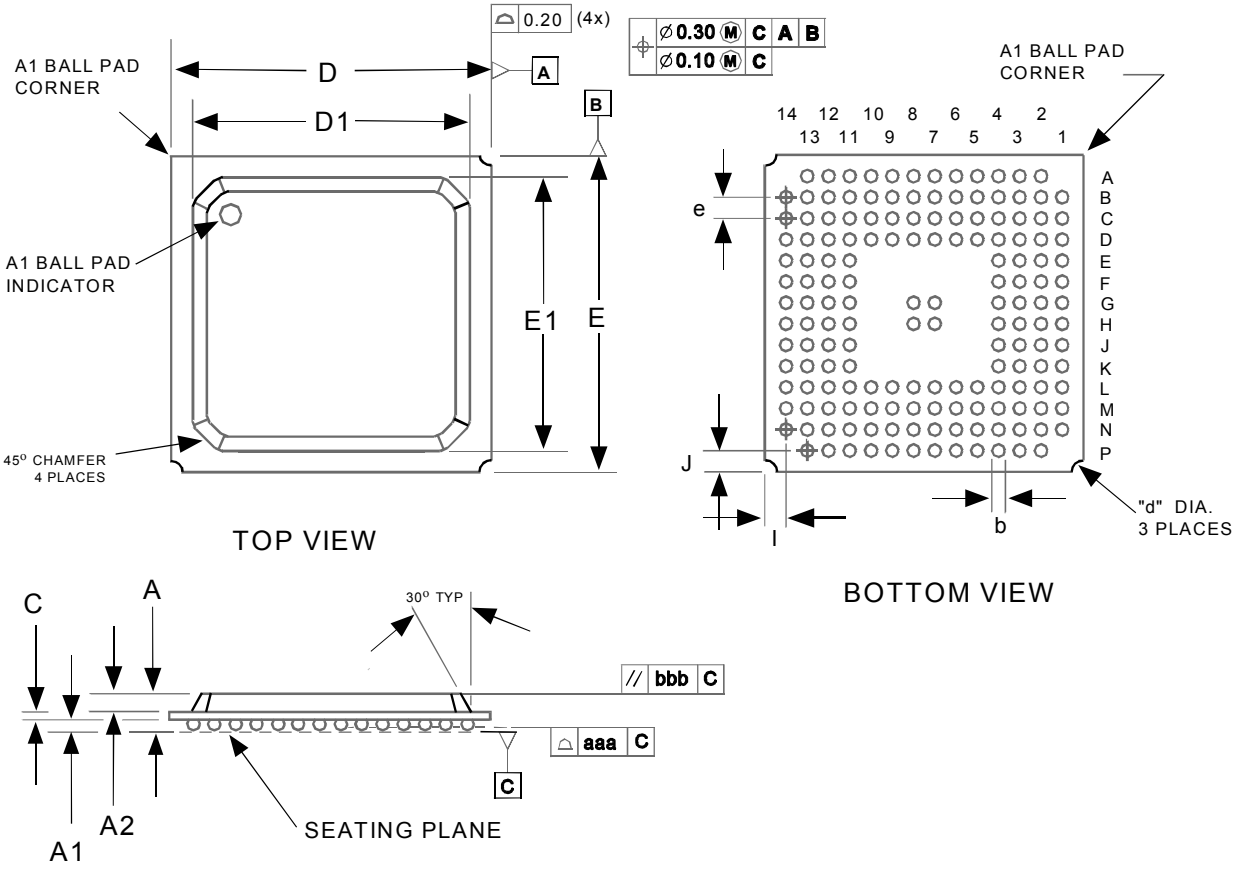
18 ORDERING AND THERMAL INFORMATION

PART NO.	DESCRIPTION
PM7350-PI	160 Plastic Ball Grid Array (PBGA)

PART NO.	CASE TEMPERATURE	Theta Ja	Theta Jc
PM7350-PI	-40°C to 85°C	30 °C/W	- °C/W

19 MECHANICAL INFORMATION

The S/UNI-DUPLEX comes in a 15 x 15 x 1.81 mm 160 PBGA (4 layer) package.



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES COPLANARITY.
3) DIMENSION bbb DENOTES PARALLEL.

PACKAGE TYPE : 160 PLASTIC BALL GRID ARRAY - PBGA																
BODY SIZE : 15 x 15 x 1.61 MM (2 layer)																
Dim	A (2 layer)	A (4 layer)	A1	A2	C (2 layer)	C (4 layer)	D	D1	E	E1	l	J	e	b	aaa	bbb
Min.	1.40	1.60	0.30	0.80	0.30	0.50	-	12.50	-	12.50	-	-	-	0.40	-	-
Nom.	1.61	1.81	0.40	0.85	0.36	0.56	15.00	13.00	15.00	13.00	1.00	1.00	1.00	0.50	-	-
Max.	1.80	2.02	0.50	0.90	0.40	0.62	-	13.70	-	13.70	-	-	-	0.60	0.15	0.35

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