PM0073
Programming manual

STM32Wxxx Flash memory microcontrollers

Introduction

This programming manual describes how to program the Flash memory of STM32W108 microcontrollers for the wireless line.

The STM32Wxxx embedded Flash memory can be programmed using in-circuit programming or in-application programming.

The **in-circuit programming (ICP)** method is used to update the entire contents of the Flash memory, using the JTAG, SWD protocol or the boot loader to load the user application into the microcontroller. ICP offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices.

In contrast to the ICP method, **in-application programming (IAP)** can use any communication interface supported by the microcontroller (I/Os, USB, CAN, UART, I^2C, SPI, etc.) to download programming data into memory. IAP allows the user to re-program the Flash memory while the application is running. Nevertheless, part of the application has to have been previously programmed in the Flash memory using ICP.

The Flash interface implements instruction access and data access based on the AHB protocol. It implements a prefetch buffer that speeds up CPU code execution. It also implements the logic necessary to carry out Flash memory operations (Program/Erase). Program/Erase operations can be performed over the whole product voltage range. Read/Write protections and option bytes are also implemented.

Table 1. Applicable products

Type	Part numbers
Microcontroller	STM32W108CB, STM32W108HB, STM32W108C8, STM32W108CC, STM32W108CZ

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Glossary

This section gives a brief definition of acronyms and abbreviations used in this document:

- The ARM® Cortex™-M3 core integrates two debug ports:
  - JTAG debug port (JTAG-DP) provides a 5-pin standard interface based on the Joint Test Action Group (JTAG) protocol.
  - SWD debug port (SWD-DP) provides a 2-pin (clock and data) interface based on the Serial Wire Debug (SWD) protocol.
    For both JTAG and SWD protocols, please refer to the *Cortex M3 Technical Reference Manual.*
- Word: data/instruction of 32-bit length
- Half word: data/instruction of 16-bit length
- Byte: data of 8-bit length
- FPEC (Flash memory program/erase controller): write operations to the main memory and the information block are managed by an embedded Flash program/erase controller (FPEC).
- IAP (in-application programming): IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.
- ICP (in-circuit programming): ICP is the ability to program the Flash memory of a microcontroller using the JTAG protocol, the SWD protocol or the bootloader while the device is mounted on the user application board.
- I-Code: this bus connects the Instruction bus of the Cortex™-M3 core to the Flash instruction interface. Prefetch is performed on this bus.
- D-Code: this bus connects the D-Code bus (literal load and debug access) of the Cortex™-M3 to the Flash Data Interface.
- Option bytes: product configuration bits stored in the Flash memory
- OBL: option byte loader.
- AHB: advanced high-performance bus.

1 Overview

1.1 Features

- 64 Kbytes, 128 Kbytes, 192 Kbytes or 256 Kbytes of Flash memory
- Memory organization:
  - Main Flash Block (MFB)
  - Fixed Information Block (FIB)
  - Customer Information Block (CIB)

Flash memory interface (FLITF) features:

- Read interface with prefetch buffer (2 × 64-bit words)
- Option byte Loader
- Flash Program / Erase operation
- Read / Write protection
- Low-power mode

1.2 Flash module organization

The memory organization is based on the available user Flash memory according to the tables below.

Table 2. Flash module organization for 64-Kbyte Flash memory devices

Block	Name	Base addresses	Size (bytes)
Main memory	Page 0	0x0800 0000 - 0x0800 03FF	1 Kbyte
	Page 1	0x0800 0400 - 0x0800 07FF	1 Kbyte
	Page 2	0x0800 0800 - 0x0800 0BFF	1 Kbyte
	Page 3	0x0800 0C00 - 0x0800 0FFF	1 Kbyte
	Page 4	0x0800 1000 - 0x0800 13FF	1 Kbyte
	. . .	. . .	. . .
	Page 63	0x0800 FC00 - 0x0800 FFFF	-
Information block	System memory	0x0804 0000 - 0x0804 07FF	2 Kbytes
	Option Bytes	0x0804 0800 - 0x0804 080F	16
	Customer specific data	0x0804 0810 - 0x0804 09FF	496
Flash Program/Erase Controller (FPEC) registers	Flash controller clock enable register	0x4000 402C	4
	Flash controller clock status register	0x4000 4030	4
Flash memory interface registers	FLASH_ACR	0x4000 8000 - 0x4000 8003	4
	FLASH_KEYR	0x4000 8004 - 0x4000 8007	4
	FLASH_OPTKEYR	0x4000 8008 - 0x4000 800B	4
	FLASH_SR	0x4000 800C - 0x4000 800F	4
	FLASH_CR	0x4000 8010 - 0x4000 8013	4
	FLASH_AR	0x4000 8014 - 0x4000 8017	4
	Reserved	0x4000 8018 - 0x4000 801B	4
	FLASH_OBR	0x4000 801C - 0x4000 801F	4
	FLASH_WRPR	0x4000 8020 - 0x4000 8023	4

Table 3. Flash module organization for 128-Kbyte Flash memory devices

Block	Name	Base addresses	Size (bytes)
Main memory	Page 0	0x0800 0000 - 0x0800 03FF	1 Kbyte
	Page 1	0x0800 0400 - 0x0800 07FF	1 Kbyte
	Page 2	0x0800 0800 - 0x0800 0BFF	1 Kbyte
	Page 3	0x0800 0C00 - 0x0800 0FFF	1 Kbyte
	Page 4	0x0800 1000 - 0x0800 13FF	1 Kbyte
	. . .	. . .	. . .
	Page 127	0x0801 FC00 - 0x0801 FFFF	1 Kbyte
Information block	System memory	0x0804 0000 - 0x0804 07FF	2 Kbytes
	Option Bytes	0x0804 0800 - 0x0804 080F	16
	Customer specific data	0x0804 0810 - 0x0804 09FF	496
Flash Program/Erase Controller (FPEC) registers	Flash controller clock enable register	0x4000 402C	4
	Flash controller clock status register	0x4000 4030	4
Flash memory interface registers	FLASH_ACR	0x4000 8000 - 0x4000 8003	4
	FLASH_KEYR	0x4000 8004 - 0x4000 8007	4
	FLASH_OPTKEYR	0x4000 8008 - 0x4000 800B	4
	FLASH_SR	0x4000 800C - 0x4000 800F	4
	FLASH_CR	0x4000 8010 - 0x4000 8013	4
	FLASH_AR	0x4000 8014 - 0x4000 8017	4
	Reserved	0x4000 8018 - 0x4000 801B	4
	FLASH_OBR	0x4000 801C - 0x4000 801F	4
	FLASH_WRPR	0x4000 8020 - 0x4000 8023	4

Table 4. Flash module organization for 192-Kbyte Flash memory devices

Block	Name	Base addresses	Size (bytes)
Main memory	Page 0	0x0800 0000 - 0x0800 07FF	2 Kbytes
	Page 1	0x0800 0800 - 0x0800 0FFF	2 Kbytes
	Page 2	0x0800 1000 - 0x0800 17FF	2 Kbytes
	Page 3	0x0800 1800 - 0x0800 1FFF	2 Kbytes
	Page 4	0x0800 2000 - 0x0800 27FF	2 Kbytes
	. . .	. . .	. . .
	Page 95	0x0802 F800 - 0x0802 07FF	2 Kbytes
Information block	System memory	0x0804 0000 - 0x0804 07FF	2 Kbytes
	Option Bytes	0x0804 0800 - 0x0804 080F	16
	Customer specific data	0x0804 0810 - 0x0804 0FFF	2032
	Extended System memory Page 0	0x0804 1000 - 0x0804 17FF	2 Kbytes
	Extended System memory Page 1	0x0804 1800 - 0x0804 1FFF	2 Kbytes
	Extended System memory Page 2	0x0804 2000 - 0x0804 27FF	2 Kbytes
	. . .	. . .	. . .
	Extended System memory Page 15	0x0804 4800 - 0x804 4FFF	2 Kbytes
Flash Program/Erase Controller (FPEC) registers	Flash controller clock enable register	0x4000 402C	4
	Flash controller clock status register	0x4000 4030	4
Flash memory interface registers	FLASH_ACR	0x4000 8000 - 0x4000 8003	4
	FLASH_KEYR	0x4000 8004 - 0x4000 8007	4
	FLASH_OPTKEYR	0x4000 8008 - 0x4000 800B	4
	FLASH_SR	0x4000 800C - 0x4000 800F	4
	FLASH_CR	0x4000 8010 - 0x4000 8013	4
	FLASH_AR	0x4000 8014 - 0x4000 8017	4
	Reserved	0x4000 8018 - 0x4000 801B	4
	FLASH_OBR	0x4000 801C - 0x4000 801F	4
	FLASH_WRPR	0x4000 8020 - 0x4000 8023	4

Table 5. Flash module organization for 256-Kbyte Flash memory devices

Block	Name	Base addresses	Size (bytes)
Main memory	Page 0	0x0800 0000 - 0x0800 07FF	2 Kbytes
	Page 1	0x0800 0800 - 0x0800 0FFF	2 Kbytes
	Page 2	0x0800 1000 - 0x0800 17FF	2 Kbytes
	Page 3	0x0800 1800 - 0x0800 1FFF	2 Kbytes
	Page 4	0x0800 2000 - 0x0800 27FF	2 Kbytes
	. . .	. . .	. . .
	Page 127	0x0803 F800 - 0x0803 FFFF	2 Kbytes
Information block	System memory	0x0804 0000 - 0x0804 07FF	2 Kbytes
	Option Bytes	0x0804 0800 - 0x0804 080F	16
	Customer specific data	0x0804 0810 - 0x0804 0FFF	2032
	Extended System memory Page 0	0x0804 1000 - 0x0804 17FF	2 Kbytes
	Extended System memory Page 1	0x0804 1800 - 0x0804 1FFF	2 Kbytes
	Extended System memory Page 2	0x0804 2000 - 0x0804 27FF	2 Kbytes
	. . .	. . .	. . .
	Extended System memory Page 15	0x0804 4800 - 0x804 4FFF	2 Kbytes
Flash Program/Erase Controller (FPEC) registers	Flash controller clock enable register	0x4000 402C	4
	Flash controller clock status register	0x4000 4030	4
Flash memory interface registers	FLASH_ACR	0x4000 8000 - 0x4000 8003	4
	FLASH_KEYR	0x4000 8004 - 0x4000 8007	4
	FLASH_OPTKEYR	0x4000 8008 - 0x4000 800B	4
	FLASH_SR	0x4000 800C - 0x4000 800F	4
	FLASH_CR	0x4000 8010 - 0x4000 8013	4
	FLASH_AR	0x4000 8014 - 0x4000 8017	4
	Reserved	0x4000 8018 - 0x4000 801B	4
	FLASH_OBR	0x4000 801C - 0x4000 801F	4
	FLASH_WRPR	0x4000 8020 - 0x4000 8023	4

The Flash memory is organized as 32-bit wide memory cells that can be used for storing both code and data constants. The Flash module is located at a specific base address in the memory map of each STM32Wxxx microcontroller type. For the base address, please refer to the *STM32Wxxx datasheet*.

The information block is divided into three parts:

- System memory is used to boot the device in System memory Boot mode. The area is reserved for use by STMicroelectronics and contains the bootloader which is used to reprogram the Flash memory using the USART1 serial interface. It is programmed by STMicroelectronics when the device is manufactured, and protected against spurious write/erase operations.
- Option bytes
- Customer-specific data which contains data defined by the user.The extended system memory (when available) contains an over-the-air bootloader which is used to reprogram the Flash memory using RF messages. It is programmed by STMicroelectronics when the device is manufactured, and protected against spurious write/erase operations.

Write operations to the main memory block and the option bytes are managed by an embedded Flash Program/Erase Controller (FPEC). The high voltage needed for Program/Erase operations is internally generated.

The main Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Page Write Protection
- Read Protection

Refer to *Section 2.3: Protections* for more details.

During a write operation to the Flash memory, any attempt to read the Flash memory will stall the bus. The read operation will proceed correctly once the write operation has completed. This means that code or data fetches cannot be made while a write/erase operation is ongoing.

The internal RC oscillator (OSCHF) is always on, but the FPEC clock needs to be enabled by writing ‘1’ to the FLASH_CLKER register and waiting for FLASH_CLKSR to set bit 0 to ‘1’.

The Flash memory can be programmed and erased using in-circuit programming and in-application programming.

Note: In the low-power modes, all Flash memory accesses are aborted. Refer to the STM32Wxxx datasheet for further information.

2 Reading/programming the STM32Wxxx embedded Flash memory

This section describes how to read from or program to the STM32Wxxx embedded Flash memory.

2.1 Read operation

The embedded Flash module can be addressed directly, as a common memory space. Any data read operation accesses the content of the Flash module through dedicated read senses and provides the requested data.

The read interface consists of a read controller on one side to access the Flash memory and an AHB interface on the other side to interface with the CPU. The main task of the read interface is to generate the control signals to read from the Flash memory and to prefetch the blocks required by the CPU. The prefetch block is only used for instruction fetches over the I-Code bus. The Literal pool is accessed over the D-Code bus. Since these two buses have the same Flash memory as target, D-code bus accesses have priority over prefetch accesses.

2.1.1 Instruction fetch

The Cortex™-M3 core fetches the instruction over the I-Code bus and the literal pool (constant/data) over the D-code bus. The cache block aims at increasing the efficiency of the I-Code bus in terms of power consumption and overall access time.

Cache buffer

The device is provided with one line of a direct mapped cache (8 bytes wide). The cache stores the most recent instruction line read by the Flash memory. To optimize the power consumption and the overall CPU execution time, it is suggested to enable the cache by setting bit FLASH_ACR[4] to '1'. Any Flash instruction read access will provide two 32-bit wide instructions; the first one is directly read by the CPU and the second one will be stored into the cache making it available for the next CPU instruction request.

Access time tuner

In order to maintain the control signals to read the Flash memory, the ratio of the prefetch controller clock period to the access time of the Flash memory has to be programmed in the Flash access control register. This value gives the number of cycles needed to maintain the control signals of the Flash memory and correctly read the required data. After reset, the value is zero and only one cycle is required to access the Flash memory.

2.1.2 D-Code interface

The D-Code interface consists of a simple AHB interface on the CPU side and a request generator to the Arbiter of the Flash access controller. D-code accesses have priority over prefetch accesses. This interface uses the Access Time Tuner block of the prefetch buffer.

2.1.3 Flash access controller

Mainly, this block is a simple arbiter between the read requests of the prefetch/I-code and D-Code interfaces.

D-Code interface requests have priority over I-Code requests.

2.2 Flash program and erase controller (FPEC)

The FPEC block handles the program and erase operations of the Flash memory. The FPEC consists of seven 32-bit registers.

- FPEC key register (FLASH_KEYR)
- Option byte key register (FLASH_OPTKEYR)
- Flash control register (FLASH_CR)
- Flash status register (FLASH_SR)
- Flash address register (FLASH_AR)
- Option byte register (FLASH_OBR)
- Write protection register (FLASH_WRPR)

An ongoing Flash memory operation will not block the CPU as long as the CPU does not access the Flash memory.

Note: These registers can be accessed for writing only in Privileged mode.

2.2.1 Key values

The key values are as follows:

- RDPRT key = 0x00A5
- KEY1 = 0x45670123
- KEY2 = 0xCDEF89AB

2.2.2 Unlocking the Flash memory

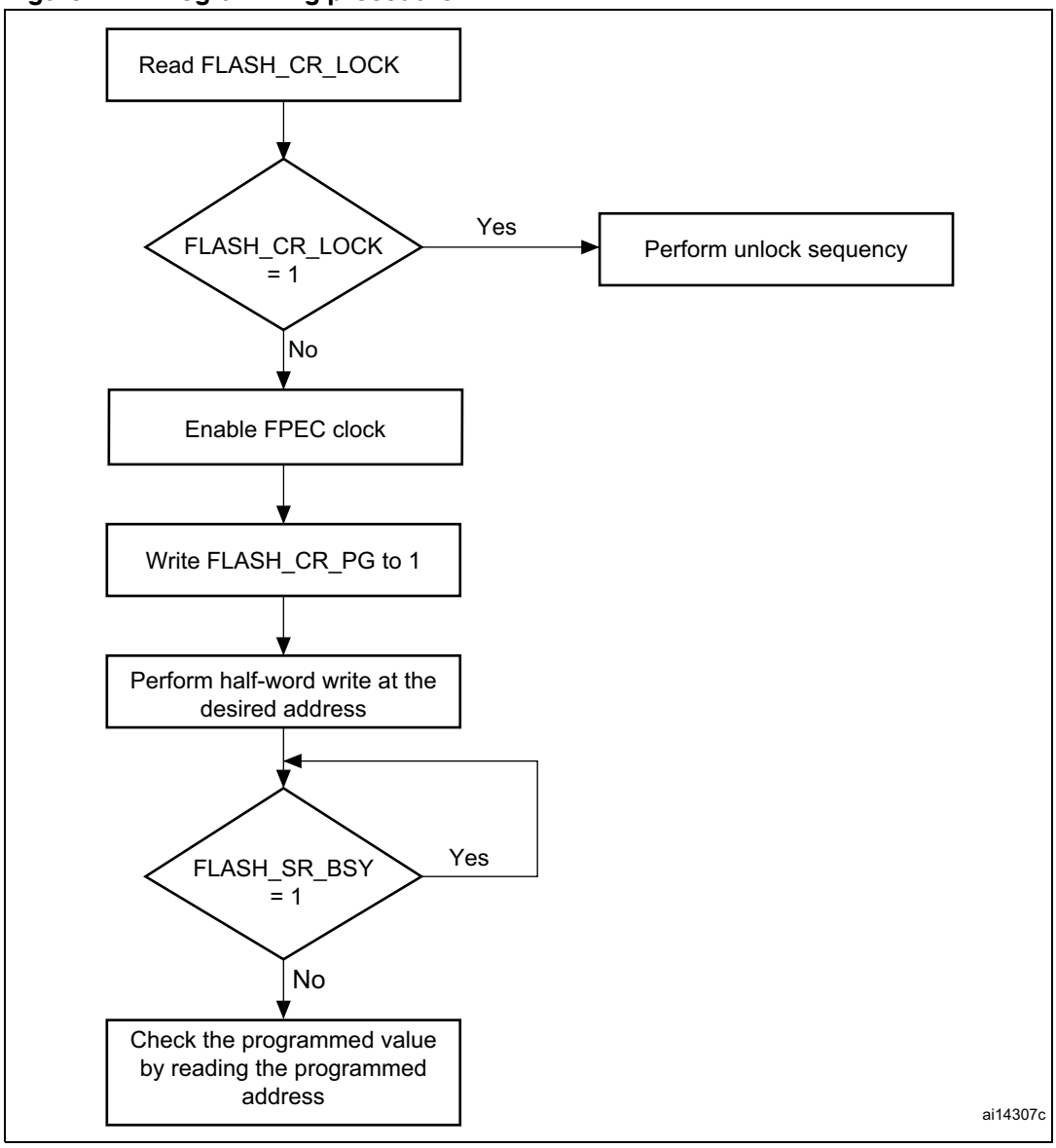
After reset, the FPEC block is protected. The FLASH_CR register is not accessible in write mode. An unlocking sequence should be written to the FLASH_KEYR register to open up the FPEC block. This sequence consists of two write cycles, where two key values (KEY1 and KEY2) are written to the FLASH_KEYR address (refer to *Section 2.2.1: Key values* for key values). Any wrong sequence locks up the FPEC block and FLASH_CR register until the next reset.

Also a bus error is returned on a wrong key sequence. This is done after the first write cycle if KEY1 does not match, or during the second write cycle if KEY1 has been correctly written but KEY2 does not match. The FPEC block and FLASH_CR register can be locked by the user's software by writing the LOCK bit of the FLASH_CR register to 1. In this case, the FPEC can be unlocked by writing the correct sequence of keys into FLASH_KEYR.

2.2.3 Main Flash memory programming

The main Flash memory can be programmed 16 bits at a time. The program operation is started when the CPU writes a half-word into a main Flash memory address with the PG bit of the FLASH_CR register set. Any attempt to write data that is not half-word long will result in a bus error response from the FPEC. If a read/write operation is initiated during programming (BSY bit set), the CPU stalls until the ongoing main Flash memory programming is over.

Figure 1. Programming procedure



Standard programming

In this mode, the CPU programs the main Flash memory by performing standard half-word write operations. The PG bit in the FLASH_CR register must be set. FPEC preliminarily reads the value at the addressed main Flash memory location and checks that it has been erased. If not, the program operation is skipped and a warning is issued by the PGERR bit in the FLASH_SR register (the only exception to this is when 0x0000 is programmed. In this case, the location is correctly programmed to 0x0000 and the PGERR bit is not set). If the addressed main Flash memory location is write-protected by the FLASH_WRPR register, the program operation is skipped and a warning is issued by the WRPRTERR bit in the FLASH_SR register. The end of the program operation is indicated by the EOP bit in the FLASH_SR register.

The main Flash memory programming sequence in standard mode is as follows:

1. Enable the FPEC clock.
2. Check that no main Flash memory operation is ongoing by checking the BSY bit in the FLASH_SR register.
3. Set the PG bit in the FLASH_CR register.
4. Perform the data write (half-word) at the desired address.
5. Wait for the BSY bit to be reset.
6. Read the programmed value and verify.

Note: The registers are not accessible in write mode when the BSY bit of the FLASH_SR *register is set.*

2.2.4 Flash memory erase

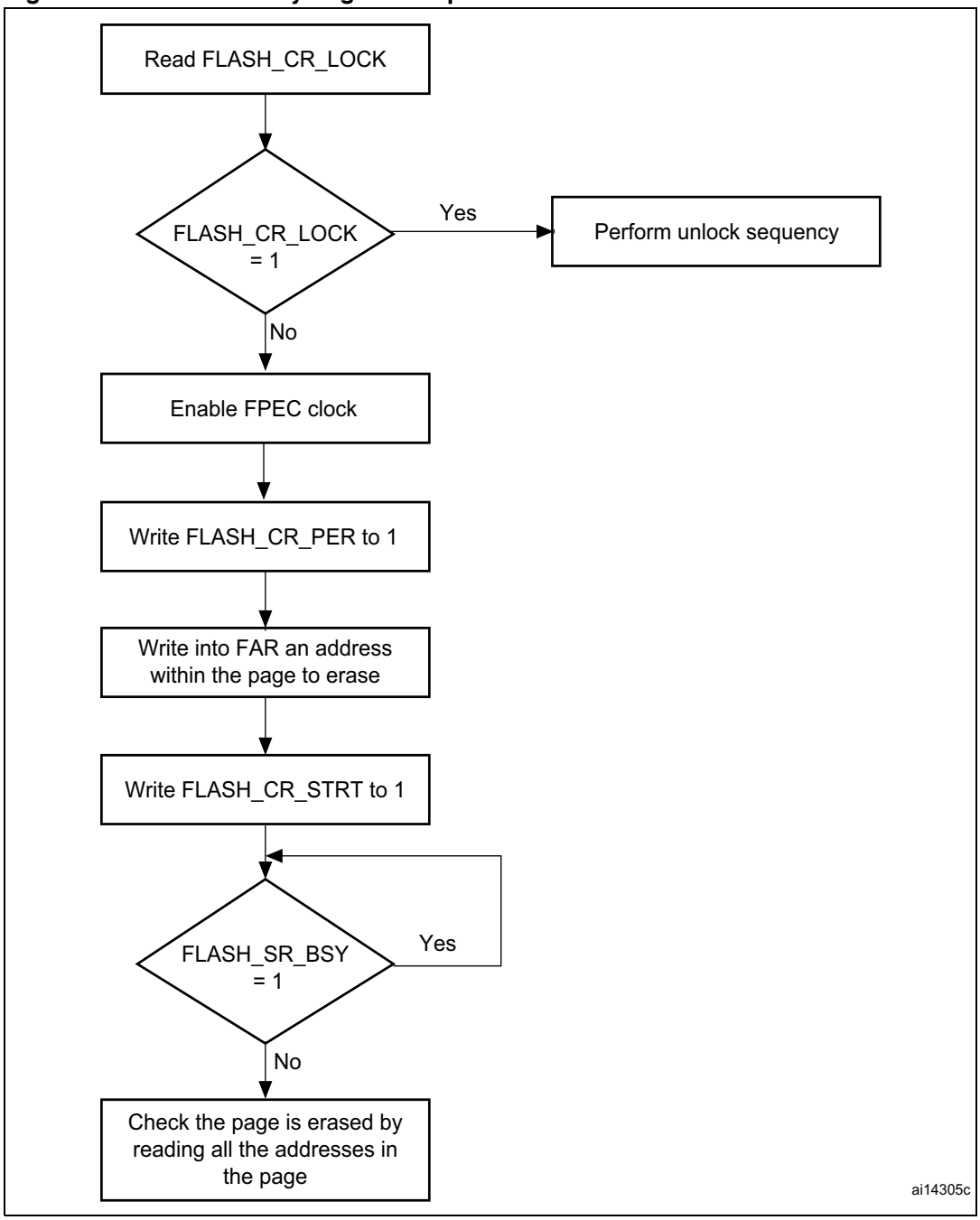
The Flash memory can be erased page by page or completely (Mass Erase).

Page Erase

A page of the Flash memory can be erased using the Page Erase feature of the FPEC. To erase a page, the procedure below should be followed:

1. Enable the FPEC clock.
2. Check that no Flash memory operation is ongoing by checking the BSY bit in the FLASH_CR register.
3. Set the PER bit in the FLASH_CR register.
4. Program the FLASH_AR register to select a page to erase.
5. Set the STRT bit in the FLASH_CR register.
6. Wait for the BSY bit to be reset.
7. Read the erased page and verify.

Figure 2. Flash memory Page Erase procedure

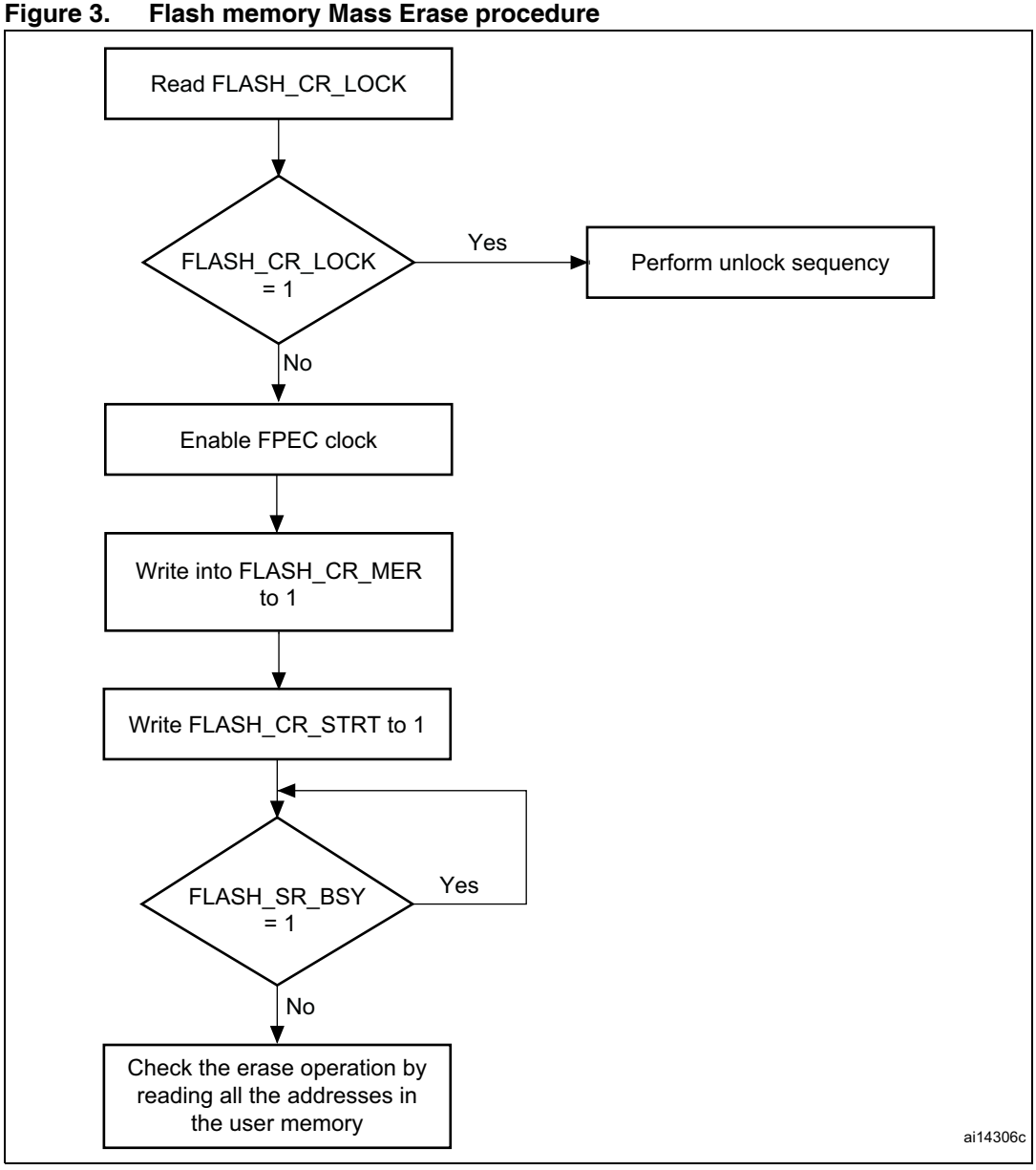


Mass Erase

The Mass Erase command can be used to completely erase the user pages of the Flash memory. The information block is unaffected by this procedure. The following sequence is recommended:

1. Enable the FPEC clock.
2. Check that no Flash memory operation is ongoing by checking the BSY bit in the FLASH_SR register.
3. Set the MER bit in the FLASH_CR register.
4. Set the STRT bit in the FLASH_CR register.
5. Wait for the BSY bit to be reset.
6. Read all the pages and verify.

Figure 3. Flash memory Mass Erase procedure



2.2.5 Option byte programming

The option bytes are programmed differently from normal user addresses. The number of option bytes is limited to 8 (4 for write protection, 1 for read protection, 1 for configuration and 2 for user data storage). Wireless line devices do not use the configuration byte nor the 2 user data bytes and all of them are marked as reserved; furthermore, some bytes are used for customer specific data that can be programmed with a similar procedure as the option bytes, but with the PG bit set instead of the OPTPG bit in the FLASH_CR register. After unlocking the FPEC, the user has to authorize the programming of the option bytes by writing the same set of KEYS (KEY1 and KEY2) to the FLASH_OPTKEYR register to set the OPTWRE bit in the FLASH_CR register (refer to *Section 2.2.1: Key values* for key values). Then the user has to set the OPTPG bit in the FLASH_CR register and perform a half-word write operation at the desired Flash address.

FPEC preliminarily reads the value of the addressed option byte and checks that it has been erased. If not, the program operation is skipped and a warning is issued by the WRPRTERR bit in the FLASH_SR register. The end of the program operation is indicated by the EOP bit in the FLASH_SR register.

The FPEC takes the LSB and automatically computes the MSB (which is the complement of the LSB) and starts the programming operation. This guarantees that the option byte and its complement are always correct.

The sequence is as follows:

1. Enable the FPEC clock.
2. Check that no Flash memory operation is ongoing by checking the BSY bit in the FLASH_SR register.
3. Unlock the OPTWRE bit in the FLASH_CR register.
4. Set the OPTPG bit in the FLASH_CR register.
5. Write the data (half-word) to the desired address.
6. Wait for the BSY bit to be reset.
7. Read the programmed value and verify.

When the Flash memory read protection option is changed from protected to unprotected, a Mass Erase of the main Flash memory is performed before reprogramming the read protection option. If the user wants to change an option other than the read protection option, then the mass erase is not performed. The erased state of the read protection option byte protects the Flash memory.

When programming the customer specific data of a wireless line device, the FPEC does not perform the complement operations and these areas can be programmed with any value by the user.

The sequence to program customer-specific data is as follows:

1. Enable the FPEC clock.
2. Check that no Flash memory operation is ongoing by checking the BSY bit in the FLASH_SR register.
3. Unlock the OPTWRE bit in the FLASH_CR register.
4. Set the PG bit in the FLASH_CR register.
5. Write the data (half_word) to the desired address.
6. Wait for the BSY bit to be reset.
7. Read the programmed value and verify.

Erase procedure

The option byte erase sequence (OPTERASE) is as follows:

1. Enable the FPEC clock.
2. Check that no Flash memory operation is ongoing by reading the BSY bit in the FLASH_SR register.
3. Unlock the OPTWRE bit in the FLASH_CR register.
4. Set the OPTER bit in the FLASH_CR register.
5. Set the STRT bit in the FLASH_CR register.
6. Wait for BSY to reset.
7. Read the erased option bytes and verify.

2.3 Protections

The user area of the Flash memory can be protected against read by untrusted code. The pages of the Flash memory can also be protected against unwanted write due to loss of program counter contexts. The write-protection granularity is four pages.

2.3.1 Read protection

The read protection is activated by setting the RDP option byte, and then by applying a system reset to reload the new RDP option byte.

Note: If the read protection is set while the debugger is still connected through JTAG/SWD, apply a POR (power-on reset) instead of a system reset (without debugger connection).

Once the protection byte has been programmed:

- Main Flash memory read access is not allowed except for the user code (when booting from main Flash memory itself with the debug mode not active).
- Pages 0-3 are automatically write-protected. The rest of the memory can be programmed by the code executed from the main Flash memory (for IAP, constant storage, etc.); it is protected against write/erase (but not against mass erase) in debug mode or when booting from the embedded SRAM.
- All features linked to loading code into and executing code from the embedded SRAM are still active (JTAG/SWD and boot from embedded SRAM) and this can be used to disable the read protection. When the read protection option byte is altered to a memory-unprotect value, a mass erase is performed.
- Flash memory access through data read using JTAG, SWV (serial wire viewer), SWD (serial wire debug) and boundary scan are not allowed.

The Flash memory is protected when the RDP option byte and its complement contain the pair of values shown in *Table 6: Flash memory protection status*.

Table 6. Flash memory protection status

RDP byte value	RDP complement value	Read protection status
0xFF	0xFF	Protected
RDPRT	Complement of RDP byte	Not protected
Any value	Not the complement value of RDP	Protected

Note: Erasing the option byte block will not trigger a Mass Erase as the erased value (0xFF) corresponds to a protected value.

Unprotection

To disable the read protection from the embedded SRAM:

1. Program the read protection code (RDP) 0x00A5 to protect the memory. This operation will fail since the option bytes are not erased, but it will force a Mass Erase of the main Flash memory which will work regardless of the status of the write protection bytes.
2. Erase the entire option byte area. As a result, the RDP will be 0xFF. At this stage, the read protection is still enabled.
3. Program the correct RDP code 0x00A5 to unprotect the memory. This operation first forces a Mass Erase of the main Flash memory.
4. Reset the device (POR Reset) to reload the option bytes (and the new RDP code), and to disable the read protection.

Note: The read protection can be disabled using the bootloader (in this case, only a System Reset is necessary to reload the option bytes). For more details, refer to AN2606.

2.3.2 Write protection

Write protection is implemented with a granularity of:

- four pages per bit for 64- and 128-Kbyte Flash memory devices,
- two pages per bit for 192- and 256-Kbyte Flash memory devices.

If a program or an erase operation is performed on a protected page, the Flash memory returns a protection error flag on the Flash memory Status Register (FLASH_SR).

The write protection is activated by configuring the WRP[3:0] option bytes, and then by applying a system reset to reload the new WRPx option bytes.

Unprotection

To disable the write protection, two application cases are provided:

Case 1 - Read protection disabled after the write unprotection:

1. Erase the entire option byte area by using the OPTER bit in the Flash memory control register (FLASH_CR).
2. Program the correct RDP code 0x00A5 to unprotect the memory. This operation first forces a Mass Erase of the main Flash memory.
3. Reset the device (system reset) to reload the option bytes (and the new WRP[3:0] bytes), and to disable the write protection.

Case 2 - Read protection maintained active after the write unprotection, useful for in-application programming with a user bootloader:

1. Erase the entire option byte area by using the OPTER bit in the Flash memory control register (FLASH_CR).
2. Reset the device (system reset) to reload the option bytes (and the new WRP[3:0] bytes), and to disable the write protection.

2.3.3 Option byte block write protection

The option bytes are always read-accessible and write-protected by default. To gain write access (Program/Erase) to the option bytes, a sequence of keys (same as for lock) has to be written into the OPTKEYR. A correct sequence of keys gives write access to the option bytes; this is indicated by OPTWRE in the FLASH_CR register being set. Write access can be disabled by resetting the bit through software.

2.4 Option byte description

There are eight option bytes. They are configured by the end user depending on the application requirements. As a configuration example, the watchdog may be selected in hardware or software mode.

A 32-bit word is split up as follows in the option bytes.

Table 7. Option byte format

31-24	23-16	15 -8	7-0
complemented option byte1	Option byte 1	complemented option byte0	Option byte 0

The organization of these bytes inside the information block is as shown in *Table 8: Option byte organization (wireless line devices)*.

The option bytes can be read from the memory locations listed in *Table 8: Option byte organization (wireless line devices)* or from the Option byte register (FLASH_OBR).

Note: The new programmed option bytes (user, read/write protection) are loaded after a system reset.

Table 8. Option byte organization (wireless line devices)

Address	[31:24]	[23:16]	[15:8]	[7:0]
0x0804 0800	nRsvd0	Rsvd0	nRDP	RDP
0x0804 0804	nRsvd2	Rsvd2	nRvsd1	Rvsd1
0x0804 0808	nWRP1	WRP1	nWRP0	WRP0
0x0804 080C	nWRP3	WRP3	nWRP2	WRP2

Table 9. Description of the option bytes and customer specific data for 64- and 128- Kbyte devices

Flash memory address	Option bytes
0x0804 0800	Bits [31:24] **nRsvd0** Bits [23:16] **Rsvd0:** Reserved, do not use (stored in FLASH_OBR[9:2]) Bits [15:8]: **nRDP** Bits [7:0]: **RDP:** Read protection option byte The read protection helps the user protect the software code stored in Flash memory. It is activated by setting the RDP option byte. When this option byte is programmed to a correct value (RDPRT key = 0x00A5), read access to the Flash memory is allowed. (The result of RDP level enabled/disabled is stored in FLASH_OBR[1].)
0x0804 0804	**Rsvdx**: Reserved, do not use. Bits [31:24]:] **nRsvd2** Bits [23:16]:] **Rsvd2** (stored in FLASH_OBR[25:18]) Bits [15:8]:] **nRsvd1** Bits [7:0]:] **Rsvd1** (stored in FLASH_OBR[17:10])
0x0804 0808	**WRPx**: Flash memory write protection option bytes Bits [31:24]: **nWRP1** Bits [23:16]: **WRP1** (stored in FLASH_WRPR[15:8]) Bits [15:8]: **nWRP0** Bits [7:0]: **WRP0** (stored in FLASH_WRPR[7:0])
0x0804 080C	**WRPx**: Flash memory write protection option bytes Bits [31:24]: **nWRP3** Bits [23:16]: **WRP3** (stored in FLASH_WRPR[31:24]) Bits [15:8]: **nWRP2** Bits [7:0]: **WRP2** (stored in FLASH_WRPR[23:16]) One bit of the user option bytes WRPx is used to protect 2 pages of 2 Kbytes in main memory block. – 0: Write protection active – 1: Write protection not active In total, 4 user option bytes are used to protect the 192/256-Kbyte main Flash memory. WRP0: Write-protects pages 0 to 31 WRP1: Write-protects pages 32 to 63 WRP2: Write-protects pages 64 to 95 WRP3: Write-protects pages 96 to 127
0x0804 0810-0x0840 09FFF	Customer specific data can be set to any value.

Table 10. Description of the option bytes and customer specific data for 192- and 256- Kbyte devices (continued)

Flash memory address	Option bytes
0x0804 0800	Bits [31:24] **nRsvd0** Bits [23:16] **Rsvd0:** Reserved, do not use (stored in FLASH_OBR[9:2]) Bits [15:8]: **nRDP** Bits [7:0]: **RDP:** Read protection option byte The read protection helps the user protect the software code stored in Flash memory. It is activated by setting the RDP option byte. When this option byte is programmed to a correct value (RDPRT key = 0x00A5), read access to the Flash memory is allowed. (The result of RDP level enabled/disabled is stored in FLASH_OBR[1].)
0x0804 0804	**Rsvdx**: Reserved, do not use. Bits [31:24]:] **nRsvd2** Bits [23:16]:] **Rsvd2** (stored in FLASH_OBR[25:18]) Bits [15:8]:] **nRsvd1** Bits [7:0]:] **Rsvd1** (stored in FLASH_OBR[17:10])
0x0804 0808	**WRPx**: Flash memory write protection option bytes Bits [31:24]: **nWRP1** Bits [23:16]: **WRP1** (stored in FLASH_WRPR[15:8]) Bits [15:8]: **nWRP0** Bits [7:0]: **WRP0** (stored in FLASH_WRPR[7:0])
0x0804 080C	**WRPx**: Flash memory write protection option bytes Bits [31:24]: **nWRP3** Bits [23:16]: **WRP3** (stored in FLASH_WRPR[31:24]) Bits [15:8]: **nWRP2** Bits [7:0]: **WRP2** (stored in FLASH_WRPR[23:16]) One bit of the user option bytes WRPx is used to protect 2 pages of 2 Kbytes in main memory block. – 0: Write protection active – 1: Write protection not active In total, 4 user option bytes are used to protect the 192/256-Kbyte main Flash memory. WRP0: Write-protects pages 0 to 15 WRP1: Write-protects pages 16 to 31 WRP2: Write-protects pages 32 to 47 WRP3[6:0]: Write-protects pages 48 to 61 WRP3[7]: Write-protects pages 62 to 127
0x0804 0810-0x08400 0FFF	Customer specific data can be set to any value.

On every system reset, the option byte loader (OBL) reads the information block and stores the data into the Option byte register (FLASH_OBR) and the Write protection register (FLASH_WRPR). Each option byte also has its complement in the information block. During option loading, by verifying the option bit and its complement, it is possible to check that the loading has correctly taken place. If this is not the case, an option byte error (OPTERR) is generated. When a comparison error occurs, the corresponding option byte is forced to 0xFF. The comparator is disabled when the option byte and its complement are both equal to 0xFF (Electrical Erase state).

All option bytes (but not their complements) are available to configure the product. The option registers are accessible in read mode by the CPU. See *Section 3: Register descriptions* for more details.

3 Register descriptions

In this section, the following abbreviations are used:

Table 11. Abbreviations

Abbreviation	Meaning
read/write (rw)	Software can read from and write to these bits.
read-only (r)	Software can only read these bits.
write-only (w)	Software can only write to this bit. Reading the bit returns the reset value.
read/clear (rc_w0)	Software can read as well as clear this bit by writing ‘0’. Writing ‘1’ has no effect on the bit value.
read/set (rs)	Software can read as well as set this bit. Writing ‘0’ has no effect on the bit value.
Reserved (Res.)	Reserved bit, must be kept at reset value.

Note: The Flash memory registers have to be accessed by 32-bit words (half-word and byte accesses are not allowed).

3.1 Flash access control register (FLASH_ACR)

Address offset: 0x00
Reset value: 0x0000 0031

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										PRFTBS	PRFTBE	HLFCYA	LATENCY		
										r	rw	rw	rw	rw	rw

Bits 31:6 Reserved, must be kept cleared.

Bit 5 **PRFTBS**: Prefetch buffer status
This bit provides the status of the prefetch buffer.
0: Prefetch buffer is disabled
1: Prefetch buffer is enabled

Bit 4 **PRFTBE**: Prefetch buffer enable
0: Prefetch is disabled
1: Prefetch is enabled

Bit 3 **HLFCYA**: Flash half cycle access enable
0: Half cycle is disabled
1: Half cycle is enabled

Bits 2:0 **LATENCY**: Latency
These bits represent the ratio of the FCLK period to the Flash access time.
000: Zero wait state, if FCLK = SCLK
001: One wait state, if FCLK = SCLK/2
010: Two wait states

3.2 FPEC key register (FLASH_KEYR)

Address offset: 0x04
Reset value: xxxx xxxx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FKEYR[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FKEYR[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Note: These bits are all write-only and will return a 0 when read.

Bits 31:0 **FKEYR**: FPEC key
These bits represent the keys to unlock the FPEC.

3.3 Flash OPTKEY register (FLASH_OPTKEYR)

Address offset: 0x08
Reset value: xxxx xxxx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPTKEYR[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPTKEYR[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Note: These bits are all write-only and will return a 0 when read.

Bits 31:0 **OPTKEYR**: Option byte key
These bits represent the keys to unlock the OPTWRE.

3.4 Flash status register (FLASH_SR)

Address offset: 0x0C
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										EOP	WRPRT ERR	Res.	PG ERR	Res.	BSY
										rw	rw		rw		r

Bits 31:6 Reserved, must be kept cleared.

Bit 5 **EOP**: End of operation

Set by hardware when a Flash operation (programming / erase) is completed. Reset by writing 1.

Note: EOP is asserted at the end of each successful program or erase operation.

Bit 4 **WRPRTERR**: Write protection error

Set by hardware when programming a write-protected address of the Flash memory.
Reset by writing 1.

Bit 3 Reserved, must be kept cleared.

Bit 2 **PGERR**: Programming error

Set by hardware when an address to be programmed contains a value different from '0xFFFF' before programming.
Reset by writing 1.

Note: The STRT bit in the FLASH_CR register should be reset before starting a programming operation.

Bit 1 Reserved, must be kept cleared

Bit 0 **BSY**: Busy

This indicates that a Flash operation is in progress. This is set at the beginning of a Flash operation and reset when the operation finishes or when an error occurs.

3.5 Flash control register (FLASH_CR)

Address offset: 0x10
Reset value: 0x0000 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			EOPIE	Res.	ERRIE	OPTWRE	Res.	LOCK	STRT	OPTER	OPTPG	Res.	MER	PER	PG
			rw		rw	rw		rw	rw	rw	rw		rw	rw	rw

Bits 31:13 Reserved, must be kept cleared.

Bit 12 **EOPIE**: End of operation interrupt enable
This bit enables the interrupt generation when the EOP bit in the FLASH_SR register goes to 1.
0: Interrupt generation disabled
1: Interrupt generation enabled

Bit 11 Reserved, must be kept cleared

Bit 10 **ERRIE**: Error interrupt enable
This bit enables the interrupt generation on an FPEC error (when PGERR / WRPRTERR are set in the FLASH_SR register).
0: Interrupt generation disabled
1: Interrupt generation enabled

Bit 9 **OPTWRE**: Option bytes write enable
When set, the option bytes can be programmed. This bit is set on writing the correct key sequence to the FLASH_OPTKEYR register.
This bit can be reset by software

Bit 8 Reserved, must be kept cleared.

Bit 7 **LOCK**: Lock
Write to 1 only. When it is set, it indicates that the FPEC and FLASH_CR are locked. This bit is reset by hardware after detecting the unlock sequence.
In the event of unsuccessful unlock operation, this bit remains set until the next reset.

Bit 6 **STRT**: Start
This bit triggers an ERASE operation when set. This bit is set only by software and reset when the BSY bit is reset.

Bit 5 **OPTER**: Option byte erase
Option byte erase chosen.

Bit 4 **OPTPG**: Option byte programming
Option byte programming chosen.

Bit 3 Reserved, must be kept cleared.

Bit 2 **MER**: Mass erase
Erase of all user pages chosen.

Bit 1 **PER**: Page erase
Page Erase chosen.

Bit 0 **PG**: Programming
Flash programming chosen.

3.6 Flash address register (FLASH_AR)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAR[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAR[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Updated by hardware with the currently/last used address. For Page Erase operations, this should be updated by software to indicate the chosen page.

Bits 31:0 **FAR**: Flash Address

Chooses the address to program when programming is selected, or a page to erase when Page Erase is selected.

Note: Write access to this register is blocked when the BSY bit in the FLASH_SR register is set.

3.7 Option byte register (FLASH_OBR)

Address offset 0x1C

Reset value: 0x03FF FFFC

Note: The reset value of this register depends on the value programmed in the option byte and the OPTERR bit reset value depends on the comparison of the option byte and its complement during the option byte loading phase.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														RDPRT	OPTERR
																														r	r

Bits 31:2 Reserved, must be kept cleared.

Bit 1 **RDPRT**: Read protection

When set, this indicates that the Flash memory is read-protected.

Note: This bit is read-only.

Bit 0 **OPTERR: Option byte error**

When set, this indicates that the loaded option byte and its complement do not match. The corresponding byte and its complement are read as 0xFF in the FLASH_OBR or FLASH_WRPR register.

Note: This bit is read-only.

3.8 Write protection register (FLASH_WRPR)

Address offset: 0x20

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRP[31:16]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRP[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 31:0 **WRP**: Write protect

This register contains the write-protection option bytes loaded by the OBL.
0: Write protection active
1: Write protection not active

Note: These bits are read-only.

3.9 Flash controller clock enable register (FLASH_CLKER)

Address: 0x4000402C

Reset value: 0x0000 0000

Note: This register is present in wireless line devices only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															EN
r/w																															r/w

Bits 31:1 Reserved, must be kept cleared.

Bit 0 EN: Request enabling of FPEC_CLK.
When set, FCLK is set to 12 MHz.

3.10 Flash controller clock status register (FLASH_CLKSR)

Address: 0x40004030
Reset value: 0x0000 0000

Note: This register is present in wireless line devices only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														BSY	ACK
																														r	r

Bits 31:2 Reserved, must be kept cleared.

Bit 1 **BSY**: Indicates FPEC is busy; therefore, keeps FPEC_CLK enabled.
Note: This bit is read-only.

Bit 0 **ACK**: Indicates FPEC_CLK (rc10mck in FLITF) is running and FCLK is 12 MHz.
Note: This bit is read-only.

3.11 Flash register map

Table 12. Flash interface - register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	**FLASH_ACR**	Reserved																										PRFTBS	PRFTBE	HLFCYA	LATENCY [2:0]		
	Reset value																											1	1	0	0	0	0
0x004	**FLASH_KEYR**	FKEYR[31:0]																															
	Reset value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0x008	**FLASH_OPTKEYR**	OPTKEYR[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0x00C	**FLASH_SR**	Reserved																										EOP	WRPRTERR	Reserved	PGERR	ERLYBSY	BSY
	Reset value																											0	0		0	0	0
0x010	**FLASH_CR**	Reserved																			EOPIE	Reserved	ERRIE	OPTWRE	Reserved	LOCK	STRT	OPTER	OPTPG	Reserved	MER	PER	PG
	Reset value																				0	0	0	0		1	0	0	0		0	0	0
0x014	**FLASH_AR**	FAR[31:0]																															
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x018	Reserved																																
0x01C	**FLASH_OBR**	Reserved																														RDPRT	OPTERR
	Reset value																															0	0
0x020	**FLASH_WRPR**	WRP[31:0]																															
	Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The base address of the following registers is 0x4000 4000. *These registers are present in wireless line devices only.*

Table 13. Flash Clock interface - register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x02C	**FLASH_CLKER**	Reserved																															EN
	Reset value																																0
0x030	**FLASH_CLKSR**	Reserved																														BSY	ACK
	Reset value																															0	0

4 Revision history

Table 14. Document revision history

Date	Revision	Changes
19-Aug-2010	1	Initial release.
21-Feb-2011	2	*Section 2.2.5: Option byte programming*: updated and added new information regarding customer specific data. *Section 2.3.1: Read protection*: updated *Unprotection*
13-Jul-2011	3	*Section 1: Overview* modified: 128 Kbytes of Flash memory replaced by 64 Kbytes, 128 Kbytes, 192 Kbytes, 256 Kbytes of Flash memory. *Table 2: Flash module organization for 64-Kbyte Flash memory devices*, *Table 3: Flash module organization for 128-Kbyte Flash memory devices*, *Table 4: Flash module organization for 192-Kbyte Flash memory devices*, *Table 5: Flash module organization for 256-Kbyte Flash memory devices* and *Table 6: Flash memory protection status* modified. *Figure 1: Programming procedure*, *Figure 2: Flash memory Page Erase procedure* and *Figure 3: Flash memory Mass Erase procedure* modified. *Section 2.3.2: Write protection* modified.
11-May-2012	4	Renamed following registers (and their constituent bits) throughout the document: – FPEC_CLK_REQ to FLASH_CLKER – FPEC_CLK_STAT to FLASH_CLKSR Added *Table 1: Applicable products*.
7-Sep-2012	5	Updated WRP2, WRP3[6:0] and WRP3[7] in *Table 10: Description of the option bytes and customer specific data for 192- and 256-Kbyte devices*.