

Fast CMOS 3.3V 16-Bit Buffer/Line Driver

Features

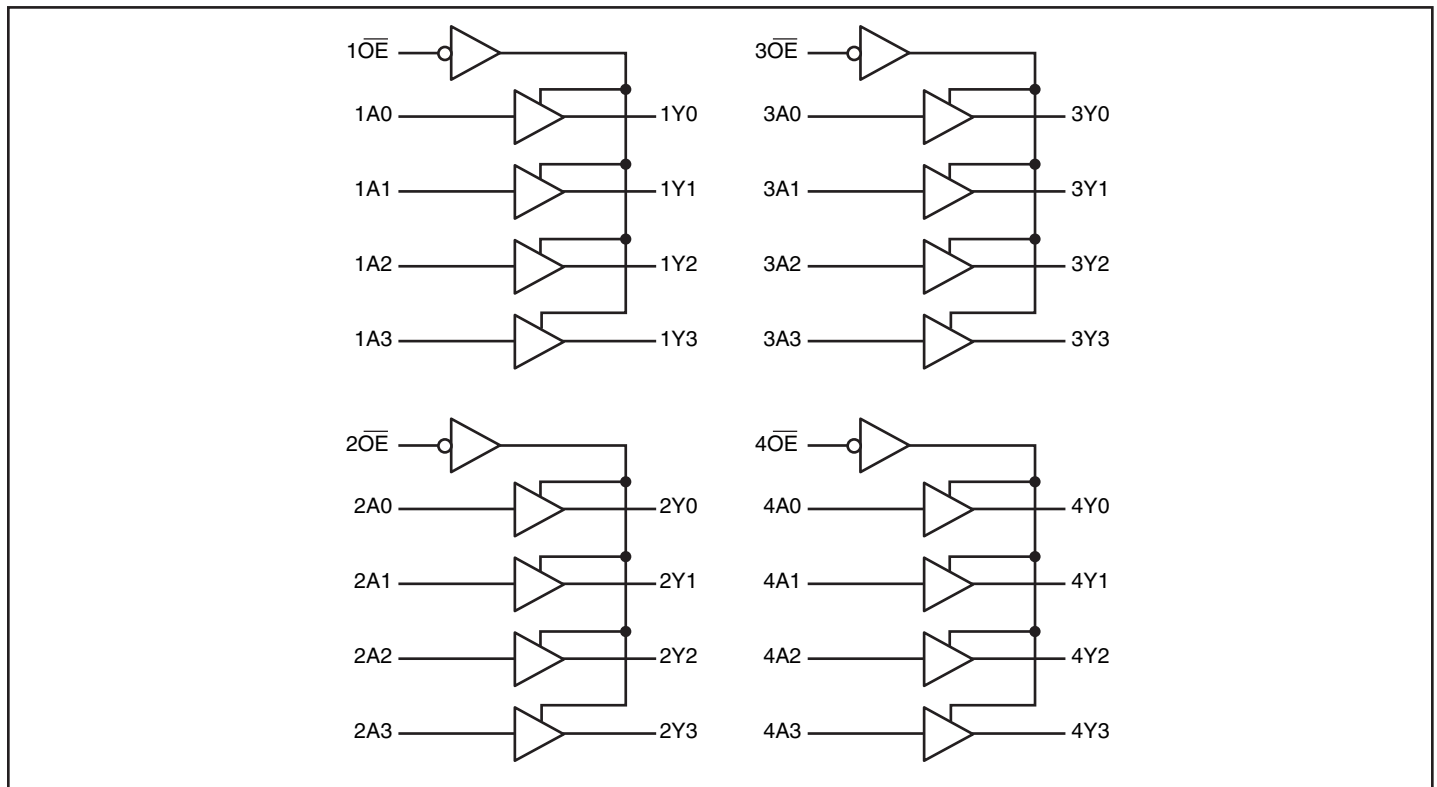
- Functionally compatible with FCT3, LVT, and 74 series 16244 families of products
- 3-State outputs
- 5V Tolerant inputs and outputs
- 2.0V – 3.6V V_{DD} supply operation
- Balanced sink and source output drives (24mA)
- Low ground bounce outputs
- Power Down High Impedance inputs and outputs
- Supports live insertion
- ESD Protection exceeds 2000V, Human Body Model
200V, Machine Model
- Packaging (Pb-free & Green Available):
 - 48-pin 300-mil wide plastic SSOP (V)
 - 48-pin 240-mil wide plastic TSSOP (A)

Description

Pericom Semiconductor’s PI74LCX16244 is a 16-bit buffer/line driver designed for driving memory loads. With its balanced-drive characteristics, this high-speed, low power device provides lower ground bounce, transmission line matching of signals, fewer line reflections and lower EMI and RFI effects. This makes it ideal for driving on-board buses and transmission lines. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The PI74LCX16244 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3V/5.0V system.

Block Diagram



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{DD} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) ...	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current.....	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Parameter	Description		Min.	Max.	Units
V _{DD}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V _I	Input Voltage		0	5.5	
V _O	Output Voltage	HIGH or LOW state	0	V _{DD}	
		3-state	0	5.5	
I _{OH} /I _{OL}	Output Current	V _{DD} = 3.0V - 3.6V		±24	mA
		V _{DD} = 2.7V		±12	
T _A	Operating Temperature		-40	85	°C
Δt/ΔV	Input Edge Rate	V = 0.8V - 2.0V, V _{DD} = 3.0V	0	10	ns/V

Pin Description

Pin Name	Description
\overline{xOE}	3-State Output Enable Inputs (Active LOW)
xAX	Inputs
xYX	3-State Outputs
GND	Ground
V_{DD}	Power

Truth Table⁽¹⁾

Inputs		Output
\overline{xOE}	xAX	xYX
L	L	L
L	H	H
H	X	Z

Notes:

- H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Pin Configuration

$\overline{1OE}$	1	48	$\overline{2OE}$
1Y0	2	47	1A0
1Y1	3	46	1A1
GND	4	45	GND
1Y2	5	44	1A2
1Y3	6	43	1A3
V_{DD}	7	42	V_{DD}
2Y0	8	41	2A0
2Y1	9	40	2A1
GND	10	39	GND
2Y2	11	38	2A2
2Y3	12	37	2A3
3Y0	13	36	3A0
3Y1	14	35	3A1
GND	15	34	GND
3Y2	16	33	3A2
3Y3	17	32	3A3
V_{DD}	18	31	V_{DD}
4Y0	19	30	4A0
4Y1	20	29	4A1
GND	21	28	GND
4Y2	22	27	4A2
4Y3	23	26	4A3
$\overline{4OE}$	24	25	$\overline{3OE}$

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 2.7\text{V}$ to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	
V_{OH}	Output HIGH Voltage	$V_{DD} = 2.7 - 3.6$	$I_{OH} = -0.1\text{mA}$	$V_{DD} - 0.2$			
		$V_{DD} = 2.7$	$I_{OH} = -12\text{mA}$	2.2			
		$V_{DD} = 3.0$	$I_{OH} = -18\text{mA}$	2.4			
			$I_{OH} = -24\text{mA}$	2.2			
V_{OL}	Output LOW Voltage	$V_{DD} = 2.7 - 3.6$	$I_{OL} = 0.1\text{mA}$			0.2	
		$V_{DD} = 2.7$	$I_{OL} = 12\text{mA}$			0.4	
		$V_{DD} = 3.0$	$I_{OL} = 16\text{mA}$			0.4	
			$I_{OL} = 24\text{mA}$			0.55	
V_{IK}	Clamp Diode Voltage	$V_{DD} = \text{Min.}, I_{IN} = -18\text{mA}$			-0.7	-1.2	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5\text{V}$	$V_{DD} = 2.7 - 3.6$			± 5	μA
I_{OZ}	Tri-State Output Leakage	$0 \leq V_O \leq 5.5\text{V}$ $V_I = V_{IH}$ or V_{IL}	$V_{DD} = 2.7 - 3.6$			± 5	
I_{OFF}	Power Down Disable	$V_{DD} = 0\text{V}, V_{IN}$ or $V_{OUT} \leq 5.5\text{V}$				10	
I_{DD}	Quiescent Power supply current	$V_{DD} = \text{Max.}$	$V_{IN} = \text{GND}$ or V_{DD}		0.1	10	
ΔI_{DD}	Quiescent Power supply current TTL Inputs High	$V_{DD} = \text{Max.}$	$V_{IN} = V_{DD} = 0.6\text{V}^{(3)}$			500	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{DD} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Per TTL driven input; all other inputs at V_{DD} or GND.

Capacitance

Parameters	Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	$V_{DD} = \text{Open}, V_I = 0\text{V}$ or V_{DD}	3	pF
C_{OUT}	Output Capacitance	$V_{DD} = 3.3\text{V}, V_I = 0\text{V}$ or V_{DD}	3	
C_{PD}	Power Dissipation Capacitance	$V_{DD} = 3.3\text{V}, V_I = 0\text{V}$ or $V_{DD}, F = 10\text{MHz}$	20	

Switching Characteristics over Operating Range

Parameters	Description	Test Conditions	V _{DD} = 3.3V±0.3		V _{DD} = 2.7V		Units
			Min.	Max.	Min.	Max.	
t _{PHL}	Propagation Delay, D _{XX} to O _{XX}	C _L = 50pF R _L = 500Ω	1.5	4.5	1.5	5.2	ns
t _{PZH}	Output Enable time		1.5	5.5	1.5	6.3	
t _{PHZ}	Output Disable time		1.5	5.4	1.5	5.7	
t _{sk(0)}	Output Skew ⁽¹⁾			1.0			

Notes:

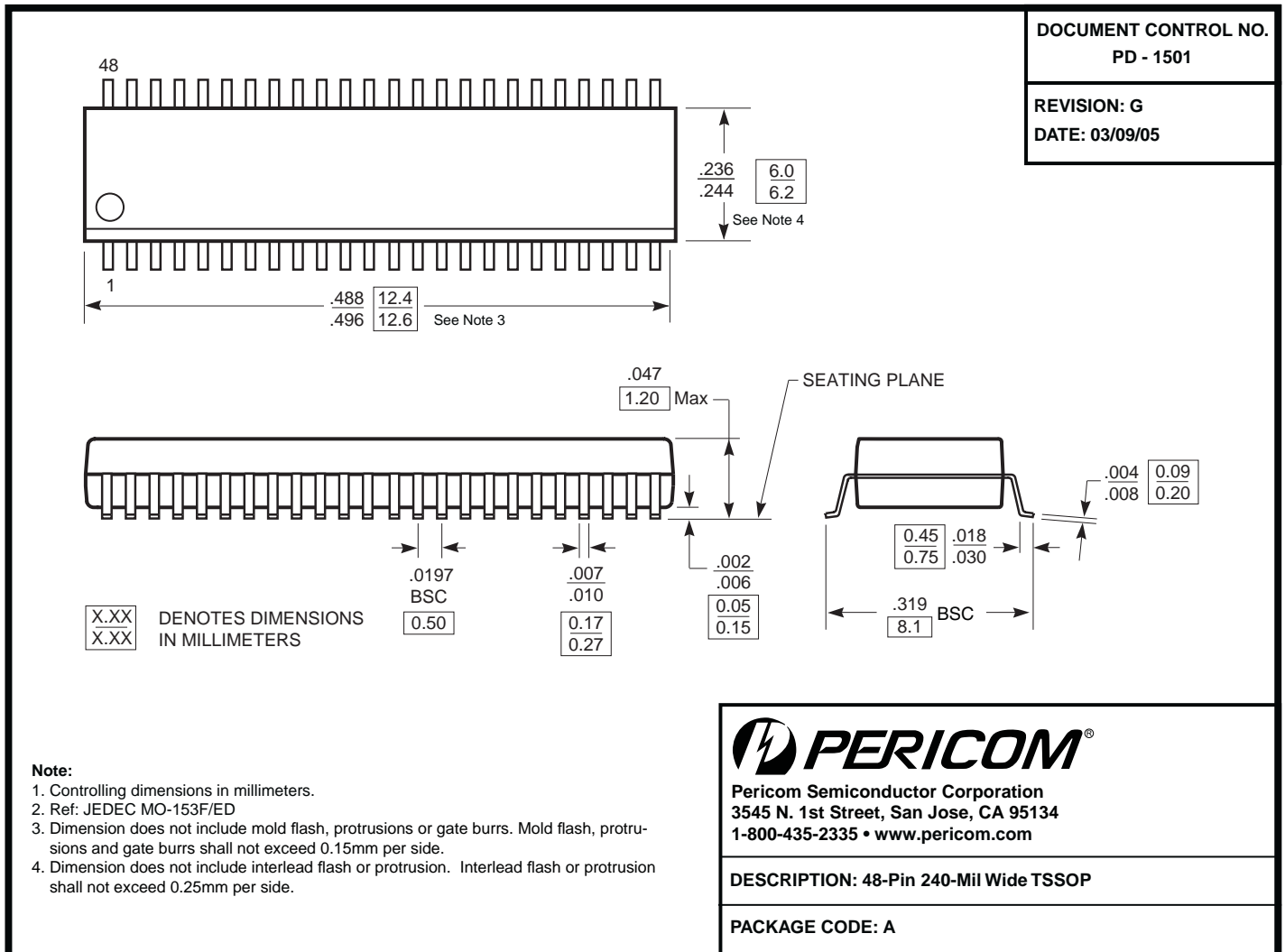
1. Skew between any two outputs, of the same package, switching in the same direction.

Dynamic Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions ⁽¹⁾	Typ.	Units
V _{OLP}	Dynamic LOW peak voltage	V _{DD} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V	0.8	V
V _{OLV}	Dynamic LOW valley voltage			

Notes:

1. Measured with 15 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.


Note:

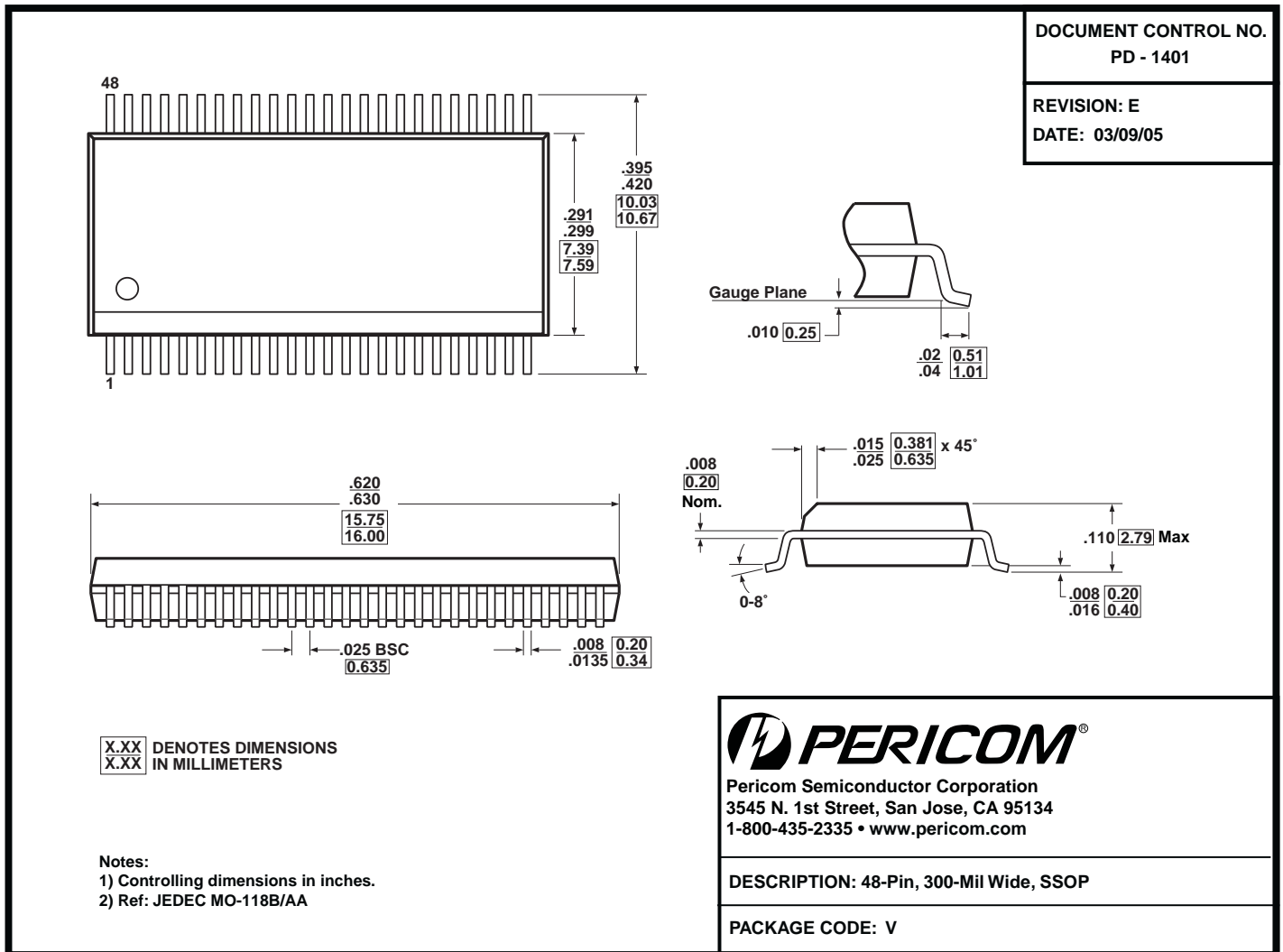
- Controlling dimensions in millimeters.
- Ref: JEDEC MO-153F/ED
- Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm per side.
- Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.



Pericom Semiconductor Corporation
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DESCRIPTION: 48-Pin 240-Mil Wide TSSOP

PACKAGE CODE: A


Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information

Ordering Code	Package Code	Package Description
PI74LCX16244AEX	A	Pb-free & Green, 48-pin 240 mil wide Plastic TSSOP
PI74LCX16244VEX	V	Pb-free & Green, 48-pin 300-mil wide plastic SSOP

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- Adding an X suffix = Tape/Reel