AMI SEMICONDUCTOR

Peripheral Imaging Corporation

PI616MC-AS

600DPI Image Sensor (CIS) PCB

Engineering Data Sheet

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PRODUCT SPECIFICATION

Reference: PI3039 Image Sensor Data Sheet

1. DESCRIPTION

This data sheet covers the PI616MC-AS specification and brief description of the PI616MC-AS CIS Module.

CIS stands for Contact Image Sensor. It is a one-dimension array of photosensitive elements, designed to image documents with a one-to-one magnification ratio. The sensors are sequentially cascaded to form a one dimensional variable-length line array in multiple integral numbers. Hence, providing the users desired lengths.

The PI616MC-AS is one of these special length line-image arrays. It is configured with a total of 8 sub sections, each section containing a sequential line of 5 array sensors with its individual video output line. These 8 video outputs, are also referred to as tapped outputs. They are all readout in parallel. See Figure 1, Simplified Circuit Block Diagram. The 8 sub sections are all sequentially cascaded to form the one-dimensional array. It is fabricated on two PCB (Printed Circuit Board) referred to as sensor boards. Each sensor board contains 4 sub sections. The two sensor boards are cascaded in series to form a complete line image sensor of 8 sub sections with a total read length of $\cong$ 325mm. Accordingly, each sensor board contains 20 each of PI3039 image sensors, also a product of PIC. Hence, for both boards there are a total of 8 parallel tapped outputs and 40 each of the PI3039 image array sensors. Each chip has 192 photo sensing cells, hence, on one board there are 3840 cell sites and a total of 7680 cell sites for both board. Each cell site is a photo-detector that possesses its own independent processing circuit. An associated on-chip digital shift register scans and reads each photo detector's video signal on to a common output video line. In section of 5 sensors these common output video lines are individually brought out to the sensor boards' I/O connectors. There are two connectors, one on each board, each with four video outputs. These connectors are connected via a cable to their respective amplifier boards. See Figure 2, System Configuration Block Diagram. PI616MC-AS's schematic and its PCB mechanical outline drawing are attached to this data sheet.

2. OVERVIEW

The PI616MC-AS has $\approx$ 324.2 mm read width. Its recommended line rate is 192μs/line @ 5.0MHz clock rate, but its minimum can be low as 160μs/line @ it's maximum clocking speed of 6.0 MHz. Its sensor photo-site density is 23.25 elements/mm. See Peripheral Imaging Corporation's PI3039 data sheet that covers the specifications on the imaging array sensor. Operationally, it requires only the power supplies, +5V and –5V and two input clocks, one is the clock, CP, to operate the internal shift registers, second is the start pulse, SP, to initiate the output scan.

3. SCAN OUTLINE

TABLE 3.1 SCANNING OUTLINE

ITEM	SPECIFICATION	NOTE
READABLE WIDTH	324.2 mm	
SENSOR PHOTO-SITE DENSITY	23.25 elements/mm	
NUMBER OF TOTAL ACTIVE SENSOR PHOTO-SITES	7680 elements	

NUMBER OF PHOTO-SITE PER TAP	960	
TOTAL LINE READ TIME = READ TIME PER SECTION	192μs/line 160μs/line	Typical, Tested @ 5.0 MHz Clock Minimum, Tested @ 6.0 MHz Clock
CLOCK FREQUENCY	5.0 MHz 6.0 MHz	Typical Maximum

4. PHYSICAL OUTLINE

TABLE 4.1 PHYSICAL OUTLINE

ITEM	SPECIFICATION	NOTE
IMAGE SENSORS	PERIPHERAL IMAGING CORP. PI3039	SEE REFERENCED IMAGE SENSOR DATA SHEET
PCB STIFFNER BOARD	PCB STIFFNER BOARD SIZE ≅355.6 mm X 41.3 mm X 6.35 mm	
SENSOR PCB	SIZE ≈165.1mm X 21.4mm X 1.62mm	2 PCB MOUNTED ON THE STIFFENER
DATA OUTPUT	8 ANALOG VIDEO OUTPUTS	
SENSOR BOARD CONNECTORS	TWO I/O CONNECTOR MOLEX 52610-1590	USED TO CONNECT TO THEIR RESPECTIVE OUTPUT AMPLIFIERS
AMPLIFIER PCB BOARD	SIZE ≈ 291.3 mm X 76.2 mm X 1.6 mm	
AMPIFIER BOARD'S FOUR CONNECTORS	TWO INPUTS: MOLEX 52207-1950 TWO OUTPUTS: ERNI-594083	MOUNTED ARE 8 OUTPUT AMPLIFIERS FOR EACH OF THE VIDEO LINES FROM THE SENSOR BOARDS

5. RECOMMENDED OPERATING CONDITIONS

TABLE 5.1 RECOMMENDED OPERATING CONDITIONS (25 °C)

ITEM	SYMBOL	MIN	TYPICAL	MAX	UNITS
	VDD	4.5	5.0	5.5	V
	IDD	135	150	165	ma
	VSS		|-5.0|	|-5.5|	V

INPUT VOLTAGE AT DIGITAL LOW (INPUT CLOCKS SP AND CP)	VIL	0		0.8	V
CLOCK FREQUENCY	FREQ (3)		5.0	6.0	MHz
CLOCK PULSE HIGH DUTY CYCLE	DUTY (4)	25		75	%
CLOCK HIGH DURATION	TPW (3)(5)	83.3	100		ns, at 50%Duty
INTEGRATION TIME	TINT	192μs/line 160μs/line			Typical, Tested @ 5.0 MHz Clock Minimum, Tested @ 6.0 MHz Clock
OPERATING TEMPERATURE	TOP (6)		25	50	^{0}C

Notes:

Note (1) Vpavg is a symbol representing the average value of every pixel in the complete line scan. Vp(n) is the pixel amplitude of nth pixel in a line scan. This measurement is taken with the image array under a uniform light exposure. The typical output is specified with a uniform input light exposure of 0.5μJ/cm^2 from a blue Led light source.

Note (2) Two saturated video output levels are specified. One is at the video signal's output amplifier, VSATA, and the other is at the input of the amplifier. In almost all applications, because the integration time is usually too short, there is not enough exposure time to saturate the array sensors. Accordingly, each output amplifier is fixed with a gain of ≅ 4.5.

Note (3) FREQ is generally fixed for any application for the following reasons: One is the exposure time. With a given light power, the exposure time of the sensor depends on integration time, TINT, and in many of the applications it uses a clock count down circuits to generate the SP, shift register start pulse, hence, it will be related to the clock frequency. The second is the shape of the video output pulse. Because of the output video is in pulse charge packets, the signals are processed on the output video line of the sensors. Hence, the signal shape depends greatly upon the amplifier configurations. Please refer to the referenced PI3039 Data Sheet. It has some brief outline application notes. Under Note 6 in page 6 there is a discussion on video pulse shapes. On page 8, 9 and 10 there are discussions on the three types of signal output stages.

Note (4) DUTY is the ratio of the clock's pulse width over its pulse period. Because the video pixel output resets during the clock pulse's high period and because the reset requires a finite resetting time, the clock duty cycle is recommended to operate within the following limits. See referenced data sheet in above note 3. Noting that the larger the DUTY, the less the signal amplitude, while too short of clock pulse will not provide enough video reset time and leaves residual charges, the recommended DUTY is 25% for frequencies < 5MHz and 50% for frequencies > 5MHz.

Note (5) TINT is determined by time interval between two start pulses, SP. Hence, if SP is generated from a clock count down circuit, it will be directly proportional to clock frequency. And it will be synchronous with the clock frequency. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system. A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion and determine the desired tolerance level for the given system.

Note (6) TOP is a conservative engineering estimate. It is based on measurements of similar CIS modules and simple bench top tests using heat guns and freeze sprays. These will be re-measured during the pilot production under the standard QA practices that is under control of ISO 9000.

6.0 ELECTRO-OPTICAL CHARACTERISTICS

TABLE 6.1 ELECTRO-OPTICAL CHARACTERISTICS (25^{O} C)

PARAMETER	SYMBOL	PARAMETER	UNITS	NOTE
NUMBER OF ACTIVE PHOTO DETECTORS		7680	elements	
PIXEL-TO-PIXEL SPACING		43.25	μm	
LINE SCANNING RATE	TINT (1)	192	μs/line	@ 5.0 MHz clock frequency, see note 1.
CLOCK FREQUENCY	FREQ (2)	6.0	MHz	Maximum clock frequency, see note 2.
RED RESPONSIVITY	ExpR (3)	70	V/μJ/cm2	See Note 3 for definition
GREEN RESPONSIVITY	ExpG (3)	55	V/μJ/cm2	See Note 3 for definition
BLUE RESPONSIVITY	ExpB (3)	35	V/μJ/cm2	See Note 3 for definition
BRIGHT OUTPUT VOLTAGE	Vpavg (4)	3.0	Volts	Green light, Exposure=X XXXXμJ/cm^2
BRIGHT OUTPUT NON-UNIFORMITY	Up (5)	<7	%	Depends on optical System. See note 5
ADJACENT PIXEL NONUNIFORMITY	Uadj (6)	<10	%	
BRIGHT OUTPUT NONUNIFORMITY TOTAL	Uptotal (7)	<10	%	Depends on the optical system, see note 5
DARK NONUNIFORMITY	Ud (8)	<25	mV	
DARK VIDEO OFFSET	Vd (9)	-2.0	Volts	
RANDOM NOISE	RNL (10)	<11.8 <3.0	p-p mV rms mV	
MODULATION TRANSFER FUNCTION	MTF (11)	>70	%	Sensor only see note 11

Notes:

1. TINT is the line-scan rate or integration time. It is determined by time interval between two start pulses, SP. Hence, if SP is generated from a clock count down circuit, it will be directly proportional to clock frequency. And it will be synchronous with the clock frequency. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system. A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion and determine the desired tolerance level for the given system.
2. FREQ is clock frequency, also equal to the signal data rate. It is generally fixed for many applications for following reasons: One is the exposure time. With a give light power, the exposure time of the sensor depends on integration time and in most applications it uses clock count down circuits to generate the SP, shift register start pulse. The second is the shape of the video output pulse. Because of the output is in pulse packets of video charges, the signal are processed on the output video line of the sensors. The signal shape depends greatly upon the amplifier configurations. Please refer to the referenced PI3039 Data Sheet. It has some brief outline application notes. Under Note 6 in page 6 there is a discussion on video pulse shapes. On page 8, 9 and 10 there are discussions on the three types of signal output stages.
3. The RESPONSIVITY is the ratio of video signal in volts divided by the unit exposure (Volts/micro-Joules/cm ^{2}). This exposure was measured with the output level adjusted to 1.27V. The spread of the measured exposure R-RSP, G-RSP and B-RSP can be used to compute the user's desired signal voltage level.

Since this is prototype module, all of the following notes 4, 5, 6, 7 and 8, are on data, based on engineering scope measurements, the data will be re-measured during pilot production using all the standard QA practices under the control of ISO 9000 regulations. Furthermore, they will be taken on fully computerized test systems. If required, these prototype data may be revised.

4. Vpmax = maximum pixel value of Vp(n); Vpmin = minimum pixel value of Vp(n); Vpavg = $\sum$ Vp(n)/7680; where Vp(n) is the n^{th} pixel in a line scan with the module scanning a uniform white target. Vp values are measured with a uniform exposure.
5. BRIGHT OUTPUT NONUNIFORMITY: Up(+) = [(Vpmax - Vpavg) / Vpavg] x 100% or Up(-)= [(Vpavg - Vpmin) / Vpavg] x 100%, whichever polarity with the highest value is selected. Two further notes, one is that the PI616MC-AS has no requirement for an optical system, or a light system. The second is that the non-uniformity is dominated by the LED light bar's non-uniformity so only the sensor non-uniformity is specified. The normal standard CIS modules are enclosed in a self-contained module with the complete optical and LED lighting system. So the light system, usually LED bar, is included in making the measurement of the optical characteristics. This fixes the optical geometry for the module and the light source. So the module's optical characteristics are simply measured with the module placed on a uniform reflecting target with a know reflection density. However, the PI616MC-AS is not enclosed with its optical and light source system. So Up is measured with uniform light source that directly illuminates the image sensors' photosite.
6. ADJACENT PIXEL NONUNIFORMITY: Upadj = MAX[| (Vp(n) - Vp(n+l) | / Vp(n)] x 100%. Upadj is non-uniformity in percentage of Vpavg. It is the maximum difference amplitude between two neighboring pixels.
7. BRIGHT OUTPUT TOTAL NONUNIFORMITY: Uptotal = [Vpmax -Vpmin]/Vpavg
8. DARK NONUNIFORMITY: Ud = Vdmax – Vdmin: It is measured over the full length of the array with the light source off and the sensors are placed in the dark. Vdmax is the maximum pixel value of the video pixel with the exposure off. Vdmin is the minimum

pixel value of the video pixel with exposure off. The references for these levels are the dark level, VDL.

9. DARK OUTPUT VOLTAGE, VDL is the level between the out video pixel dark level and the ground.
10. RANDOM NOISE, RNL, is measured using two methods, one is tangentially on the scope. This measures an approximate peak-to-peak, p-p, random thermal noise. The other is in terms of rms. It is estimated by using the Gaussian Statistical Methods. One pixel is selected out of a line scan and its peak values are recorded for a multiple line scans. These random peak values are used to estimate the rms values.
11. MODULATION TRANSFER FUNCTION depends on the optical system. Since this system relies on the users optical system it was not measured. Refer back to note 5, measurements on Up, all notes that references the optical measurements applies to MTF measurements as well. Using a conservative engineering estimate, the sensor's MTF is in excess of 70% at the Optical Nyquest Frequency.

7.0 ELECTRICAL CLOCKING CHARACTERISTICS.

TABLE 7.1 CLOCK AMPLITUDE AND DUTY CHARACTERISTICS (Ta =25^{O}C)

ITEM	SYMBOL	CONDITION	SPECIFICATION			UNITS
			MIN	TYP	MAX	
CLOCK INPUT VOLTAGE	VIH (1)	For values see the notes		See note (1) for values		
	VIL (1)					
CLOCK INPUT CURRENT	IIH (1)			See note (1) for values		
	IIL (1)					
CLOCK FREQUENCY	FREQ (2)		0.100	5.0	6.0	MHz
LINE READ TIME	TINT (3)		160	192	1000	μs
CLOCK PULSE DUTY CYCLE	RATIO= tw/ to (4)		25	50	75	%

Note 1. These clock, CP, and start pulse, SP, values are compatible with CMOS 74HCXX series logic devices.

Note 2. FREQ is not only the clock frequency, but is also equal to the pixel sample rate. See not 2 under Table 6.1.

Note 3. TINT is the Line scan read time that depends on the interval between the start pulse entries. See note 1 under Table 6.1. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system. A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion and determine the desired tolerance level for the given system.

Note 4. The definition for the symbols used in the RATIO is defined under the 7.2 Timing Diagram.

7.2 TIMING DIAGRAM

TABLE 7.2 CLOCK TIMING CHARACTERISTICS, SEE FIGURE 3. TIMING DIAGRAM

This table is defines the symbols used in the timing diagram, Figure 3. Timing Diagram. It is for a single video section. However it applies to all eight video sections. Accordingly, the system-timing diagram is a composition of this timing diagram repeated eight times with all waveforms in parallel, so electrically the system produces pixels from all eight video section simultaneously.

ITEM	SYMBOL	MIN.	TYPICAL	MAX.	UNITS
CLOCK CYCLE TIME (2)	to	0.1666	0.200	10	μs
CLOCK PULSE WIDTH (2)	tw		0.100		ns
CLOCK DUTY CYCLE (2)	duty	25	50	75	%
PROHIBIT CROSSING TIME OF START PULSE	tprh	30			ns
DATA SETUP TIME	tds	30			ns
DATA HOLD TIME	tdh	25			ns
SIGNAL DELAY TIME	tdl			75	ns
SIGNAL SAMPLE TIME	tsmp (3)	125			ns
SIGNAL FALL TIME	tsigf			75	ns
RECOMMEND SP GENERATION	Tonoff (4)				

1. Applies to whole chart. All of the symbol definitions in above table are used in Figure 3, TIMING DIAGRAM. For the complete system, there are only two clocks, CP, and start pulse, SP and there logic levels are compatible with CMOS 74HCXX series logic devices.
2. See the notes on clock periods (the inverse of FREQ) and their duty cycle under Table 5.1 notes 3 and 4.
3. See PI3039 DATA SHEET page 6, Table 6A, note 6.
4. Recommend method for SP generation because the shift register loads only on the falling edge.

8.0 MAXIMUM RATINGS

TABLE 8.1 MAXIMUM RATINGS (Not to be used for continuous operation)

ITEM	SYMBOL	SPECIFICATION	NOTE
DC SUPPLY VOLTAGE	VDD	7 V	
INPUT VOLTAGE	VIN	0 TO VDD+0.3	SP & CP
AMBIENT TEMPERATURE (1)	TA (PCB Surface)	0 TO 70^{O}C (See note, below.) -10^{O} to +75^{O}C (See note, below.)	Operational Storage
AMBIENT HUMIDITY (1)	HA	0 to 80% (See note)	Non Condensing
MAXIMUM OPERATING CASE TEMPERATURE (1)	PCB Temperature	70^{O}C (See note, below.)	

Note (1) All referenced parameters are conservative engineering estimate based on few of the prototype PCB. They are based on measurements of similar CIS modules and/or simple bench top tests using heat guns and freeze sprays. However these parameters will be re-measured during the pilot production using standard QA practices that is under the control of ISO 9000 regulations.

9.0 I/O CONNECTOR PIN CONFIGURATION

There are two I/0 connectors on the stiffener plate with the two sensor boards. They are MOLEX 52610-1590. They serve to interconnect the sensor boards to the amplifier boards. See the outline drawing of the system, Figure 2, System Configuration Block Diagram. Two 15 conductors strip lines serve as the interfacing harness. It is depicted with harnesses coming from under the stiffener plate and crossing to the top of the amplifier board and connecting to the two input connectors MOLEX 52207-1950. The final connectors are the two ERNI-594083. They are the SYSTEM I/Os.

TABLE 9.1A SENSOR BOARD CONNECTORS AND INPUT CONNECTORS FOR AMPLIFIER BOARD PIN OUTS

Only one of the two connectors on the stiffener board is specified because both connectors have identical pin out definitions. There are 8 video taps, 4 from each sensor board. They are sequential renumbered. The first sensor board video outputs are, 1, 2, 3 and 4. The second sensor board's videos are 5, 6, 7 and 8.

TWO MOLEX 52610-I590 AND ITS MATE TO AMPLIFIER BOARDS MOLEX 52207-1590

PIN NUMBERS	PIN NAMES	SYSMBOL	I/0	NAMES AND FUNCTIONS
1	CLOCK PULSE	CP	I	
2	START PULSE	SP	I	
3	GROUND	GRD	I	GROUND; 0V
4	POWER SUPPLY	VDD	I	POSITIVE POWER SUPPLY
5	GROUND	GRD	I	GROUND; 0V
6	GROUND	GRD	I	GROUND; 0V
7	GROUND	GRD	I	GROUND; 0V
8	VIDEO OUTPUT	VSEC1	O	TAPPED 1 VIDEO OUTPUT, SECTION 1 ON BOARD 1. IT IS SECTION 5 ON BOARD 2
9	ANALOG GROUND	AGRD	I	ANALOG VIDEO RETURN LINE, GROUND; 0V
10	VIDEO OUTPUT	VSEC2	O	TAPPED 2 VIDEO OUTPUT, SECTION 2 ON BOARD 1. IT IS SECTION 6 ON BOARD 2
11	ANALOG GROUND	AGRD	I	ANALOG VIDEO RETURN LINE, GROUND; 0V
12	VIDEO OUTPUT	VSEC3	O	TAPPED 3 VIDEO OUTPUT, SECTION 3 ON BOARD 1. IT IS SECTION 7 ON BOARD 2
13	ANALOG GROUND	AGRD	I	ANALOG VIDEO RETURN LINE,

				GROUND; 0V
14	VIDEO OUTPUT	VSEC4	O	TAPPED 4 VIDEO OUTPUT, SECTION 4 ON BOARD 1. IT IS SECTION 8 ON BOARD 2
15	ANALOG GROUND	AGRD	I	ANALOG VIDEO RETURN LINE, GROUND; 0V

TABLE 9.1B AMPLIFIER BOARD OUTPUT CONNECTORS, ERNI-594083

There are four connectors on the amplifier board. Two are inputs, which are described above, and two are outputs, which are described below. There is only one table shown for both connectors. They are both identical in there connections except one is for sensor board 1's outputs and the other is for sensor board 2's outputs. Accordingly each of the video outputs, after amplification, for both sensor boards are labeled VOUT1, VOUT2, VOUT3 and VOUT4. Videos from sensor board 1, VSEC1's corresponding output is VOUT1, VSEC2's corresponding output is VOUT2, VSEC3's corresponding output is VOUT3 and VSEC4's corresponding output is VOUT4. Then the videos from sensor board 2 will have their corresponding outputs on the second connector VOUT1, VOUT2, VOUT3 and VOUT4, except they are outputs VOUT5, VOUT6. VOUT7 and VOUT8 because their video signals originate from section 5, section 6, section 7 and section 8 of the sensor board 2.

ERNI CONNECTOR ERNI-594083

PIN NUMBERS	DESCRIPTION ROW A	DESCRIPTION ROW B	DESCRIPTION ROW C
1	VDD	VDD	AGND
2	VDD	VDD	VOUT1
3	NO CONNECT	NO CONNECT	AGND
4	GROUND	GROUND	AGND
5	SP	GND	AGND
6	NO CONNECT	GND	VOUT2
7	NO CONNECT	GND	AGND
8	NO CONNECT	GND	AGND
9	CLK	GND	AGND
10	GND	GND	VOUT3
11	NO CONNECT	GND	AGND
12	NO CONNECT	GND	AGND
13	NO CONNECT	GND	AGND
14	GND	GND	VOUT4
15	NO CONNECT	NO CONNECT	AGND
16	VSS	VSS	AGND

Note: The functional description for the symbols used in the table below are same as described for the input connector. The two new symbols VSS and CLK are as follows:
VSS is negative supply input. CLK is CP.
The locations of pin 1 on all the connectors are facing the same end. See Figure 2, System Configuration Block Diagram.

10.0 SCHEMATIC DIAGRAM

Two reference schematic diagrams are attached. Only one schematic, CKT 1, Sensor Board Schematic, is required to represent both the sensor board 1 and 2 because the circuits are identical. The second one is for the amplifier board it contains all eight of the amplifiers on one schematic. The circuit description of its structure and operation has been briefly discussed in section 1, DISCRIPTION, page 2. Its operation follows from the discussion of the simplified block diagram. There are only two input control clocks for the circuits, the clock, CP, and the start pulse, SP. SP starts the shift register scanning while CP clocks the register and produces the video pixels at its same rate. The clocks are entered through the I/O connectors on both sensor boards. They are both externally buffered with the 74HC00 hexes and applied to inputs of the image sensors. On each of the two-image array sensor boards there are four sequential video sections. Each video section contains a row of 5 sequential image array sensors, PI3039. These are all clock in parallel with CP. The four sections on both boards are clocked with SP in parallel to initiate all eight video sections and simultaneously begin the eight sequential readouts. All eight lines, four in each sensor board, have reset switches, BU4S66, that parallel resets the video pixel charges after they are readout. These pixels, readout in parallel, are applied to their respective output amplifiers on the amplifier board.

The second schematic, CKT 2, Amplifier Board Schematic, is the amplifier board. There are eight amplifiers for processing the output videos from both sensor boards. The amplifier board receives the inputs from sensor board output connector, J1, through two harnesses. They are connected into the input I/O connectors, J1 and J2, of the amplifier board. Since there are two sensor boards using the same schematic representation, the connector on sensor board 1, J1, becomes J2 for the second board. They are physically differentiated and marked as J1 and J2 on the Stiffener Board. Since all eight sections process their video signals through identical amplifiers, only one amplifier circuit is discussed. The AD8051 is an operational amplifier that is configured into non-inverting buffer amplifier with again of $\cong 4.5$. It is used to isolate the video line from its external circuits. The isolated video line then serves as a storage capacitance for the pixels outputs. The pixel charges are read out onto the video line capacitance and integrated. This integrated pixel charges, converted to a voltage pulse, is amplified and produced at the output I/O. The reset switch on the video line, which is located on the sensor board schematic, resets the pixel signal charge prior to the readout of following pixel.

11.0 DRAWING ON MECHANICAL STRUCTURE

Attached are 6 mechanical drawings. The first one, Top Assemble Outline, sheet 1of 1, shows an outline drawing of the complete CIS system, consisting of the Stiffener Plate, the interconnecting harness and the Amplifier Board. There are two connector Pin Configuration Tables, one for the two sensor boards and the input for the amplifier board. The other is for the two output connectors on the amplifier boards. These two tables show the pin numbering and names for the 6 connectors that are seen in the drawing. For detail descriptions of the interconnection and their functions, see section 9.0 CONNECTORS PIN CONFIGURATION, page 9.

The second one, Stiffener Plate, is the view of the stiffener board. Stiffener board is ¼" aluminum backing plate on which the two image sensor boards are mounted. It provides the dimensions of the plate, its access holes for the two-sensor board's connectors, along with all of the required dimensions.

The third one, Two Sensor Board on the Stiffener, is a view of the two sensor boards mounted on the stiffener board. It shows the direction of the scan, its first pixel location and

its video read line location. It provides the dimensions on the connector height, the thickness of PCB board and its component height.

The fourth one, Connectors on Stiffener, is a backside view of the stiffener plate. It shows the location of the connectors and its pin order and direction.

The fifth one, Amplifier Board, is a view of the PCB outline. The three views of the board provide the outline dimensions, its length, its width and its thickness. It also depicts the mounting holes and their dimensions and locations.

The six one, Amplifier Board and Its Connectors, is view of the PCB with its connectors.

11.0 BLOCK DIAGRAMS; FIGURES 1, 2, AND 3

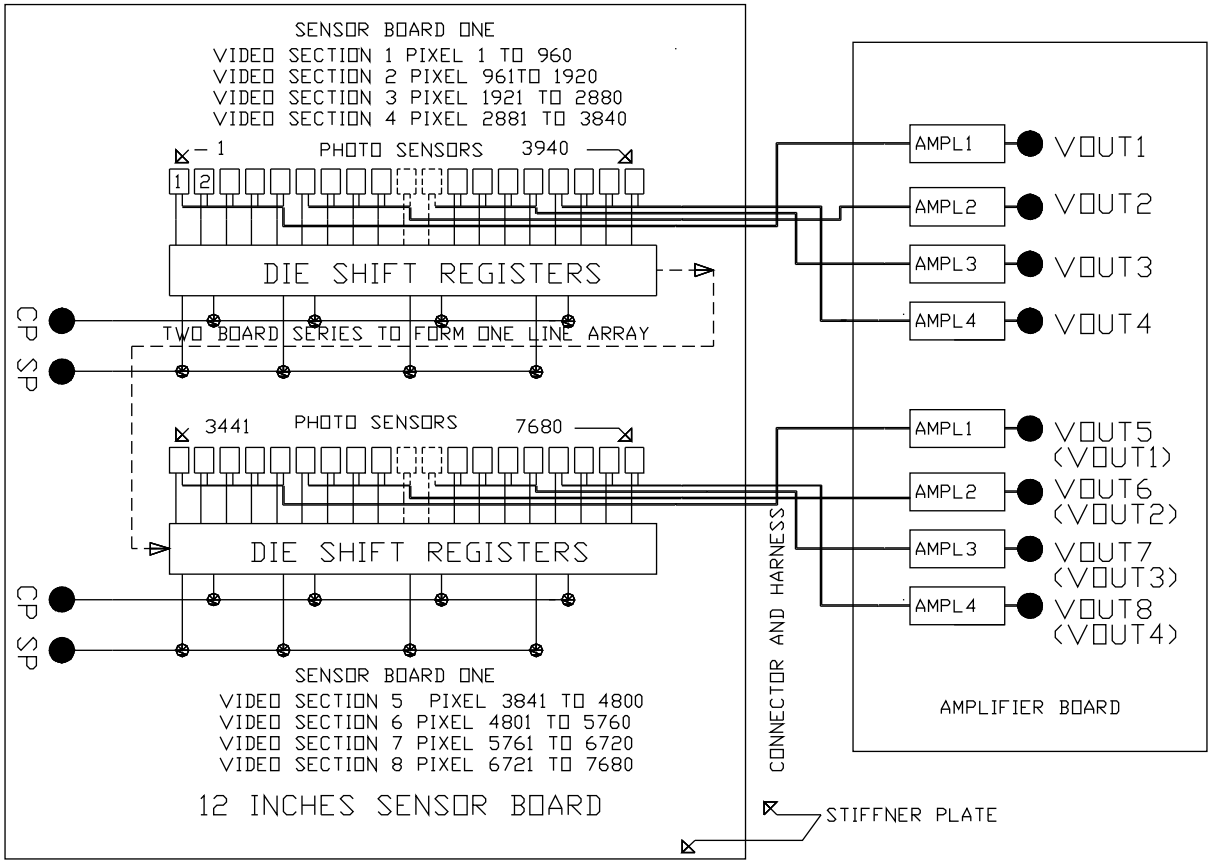


FIGURE 1. SIMPLIFIED CIRCUIT BLOCK DIAGRAM

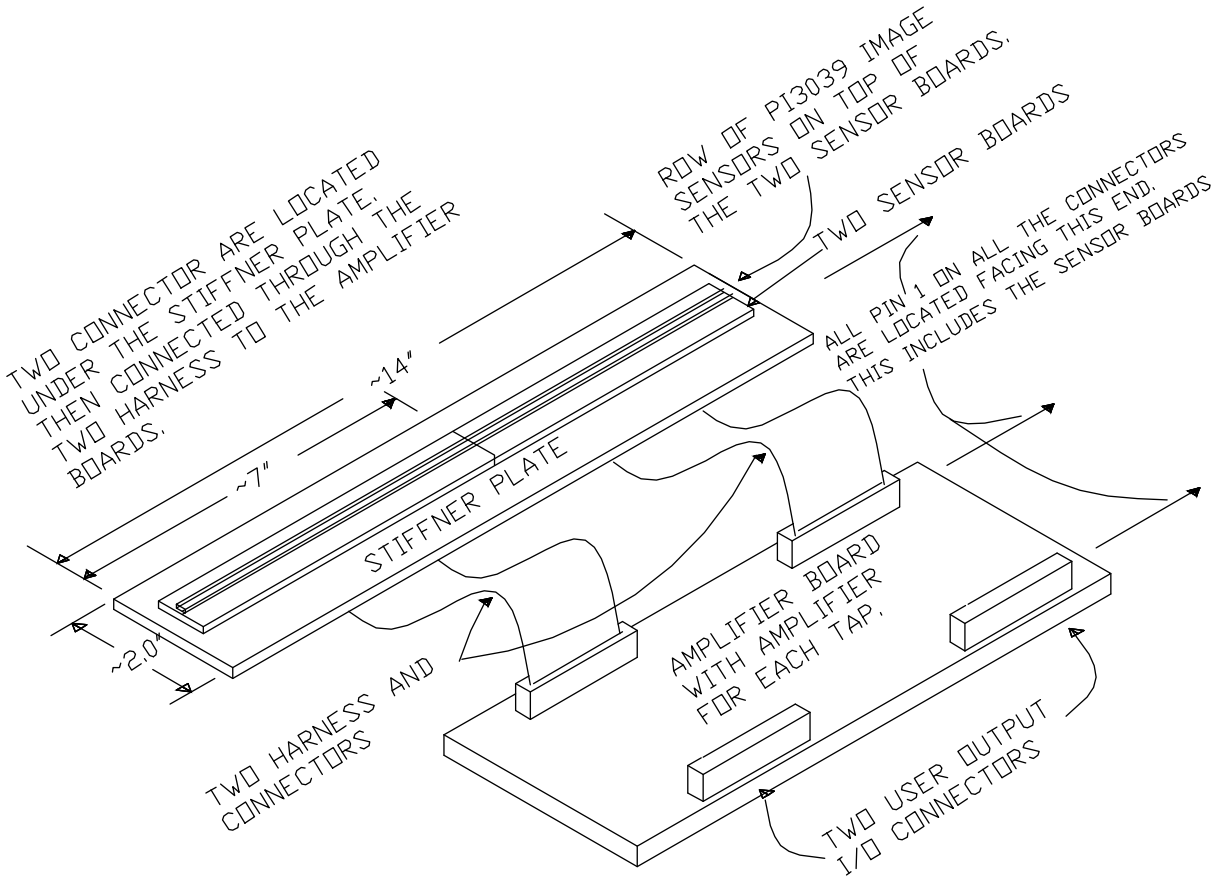


FIGURE 2, SYSTEM CONFIGURATION BLOCK DIAGRAM

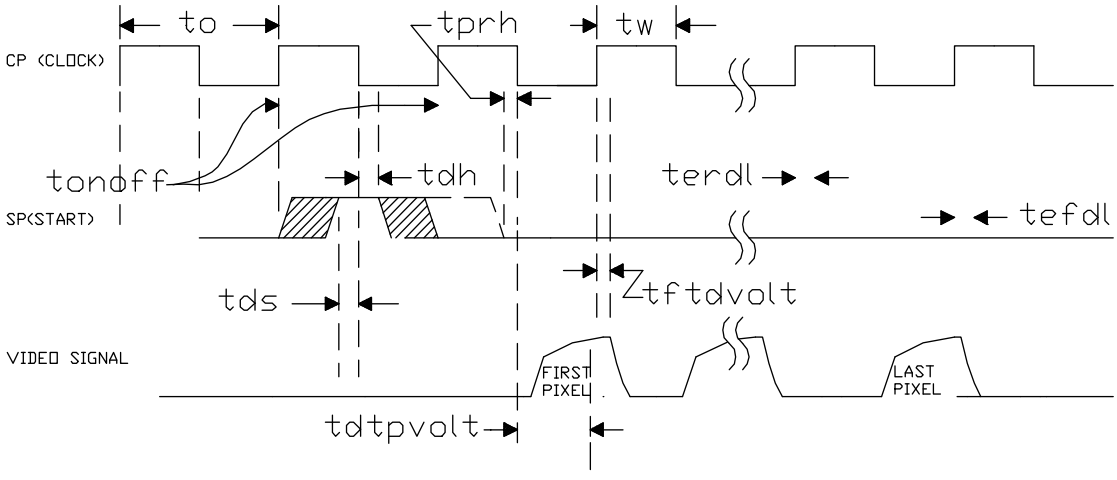
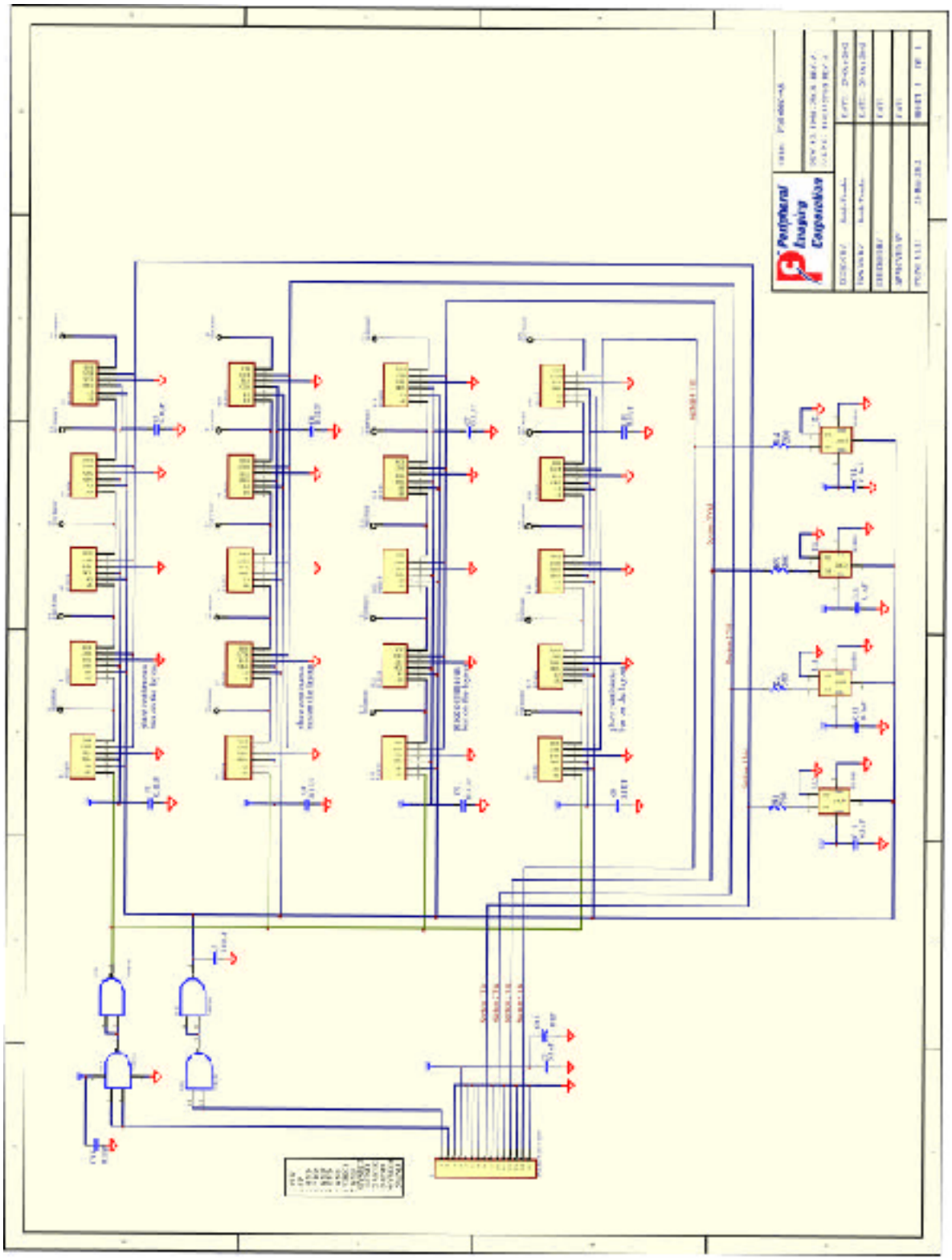
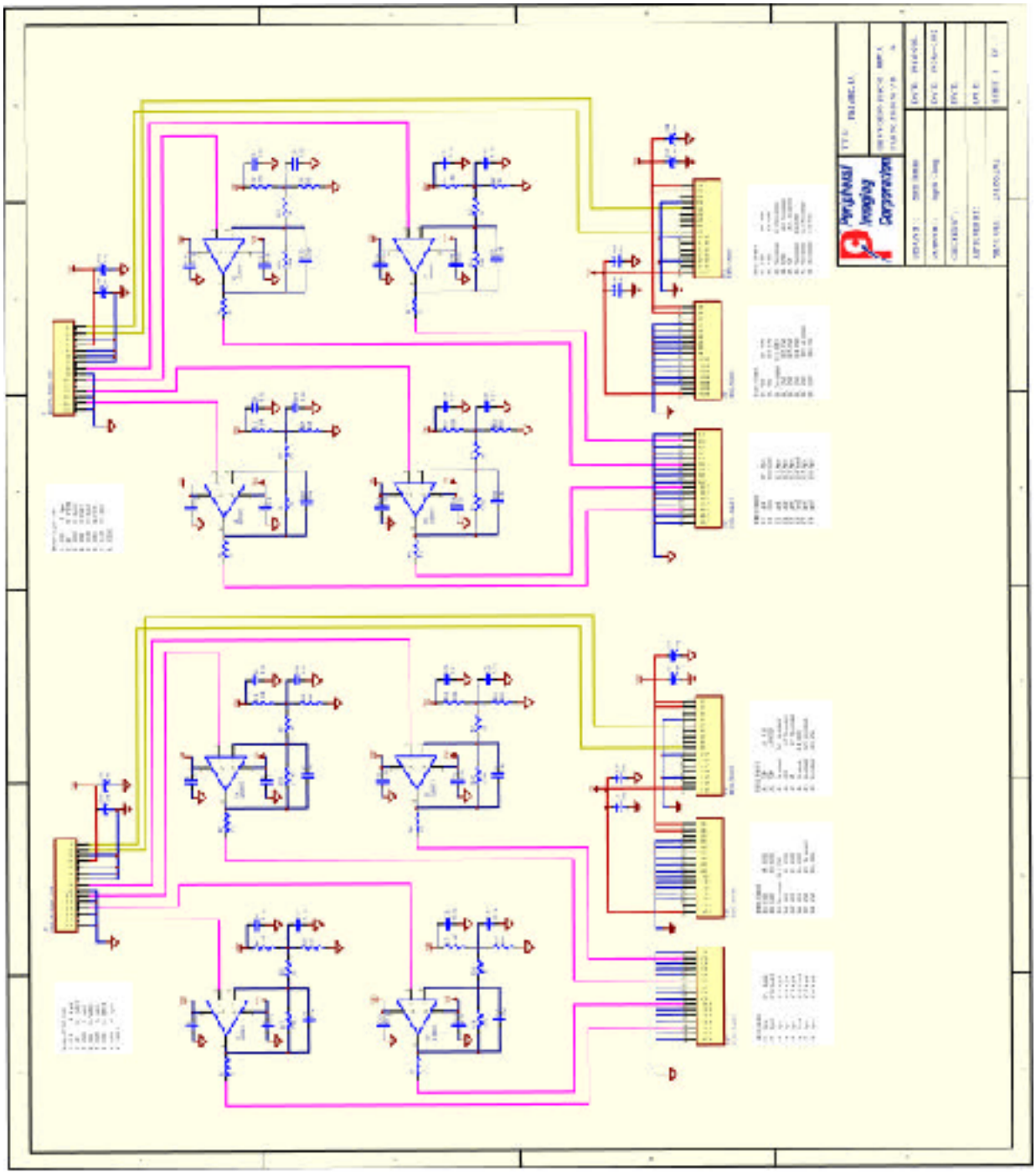


FIGURE 3. TIMING DIAGRAM

12.0 SCHEMATIC DRAWINGS; CKT 1 AND CKT 2

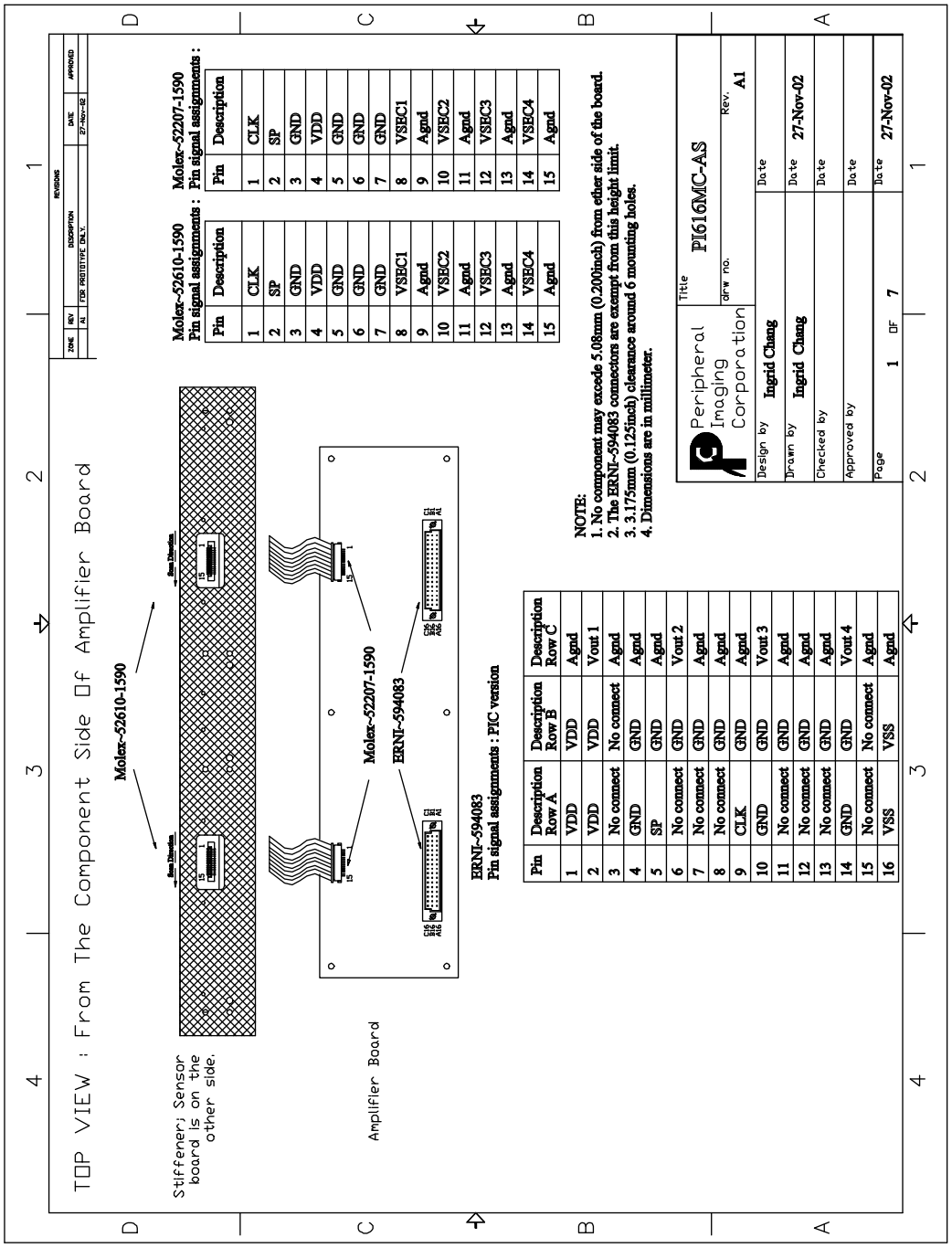


CKT 1. SENSOR BOARD SCHEMATIC



CKT 2. AMPLIFIER BOARD SCHEMATIC

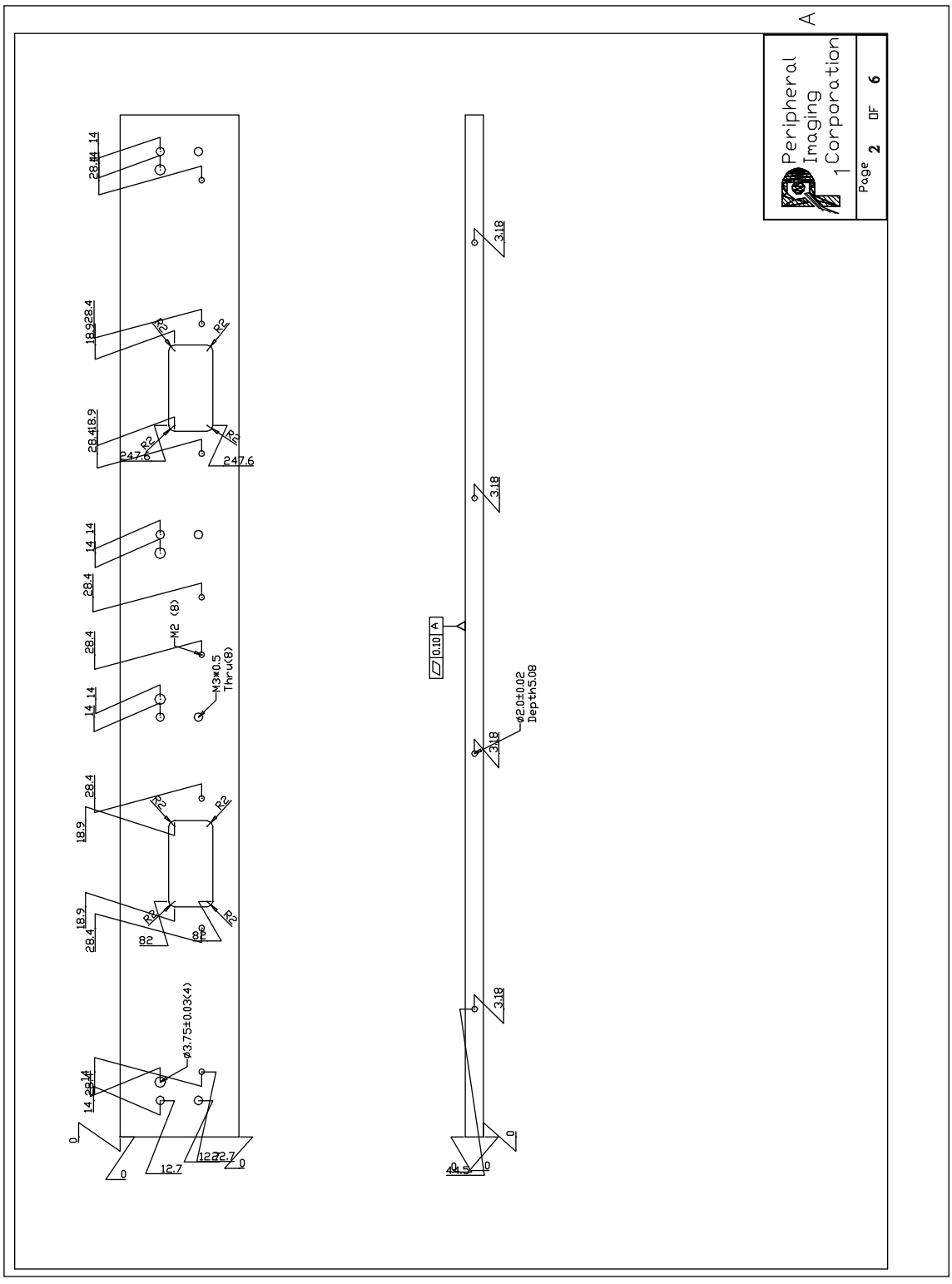
13.0 MECHANICAL DRAWINGS; DRW 1. 2. 3, 4, 5 AND 6



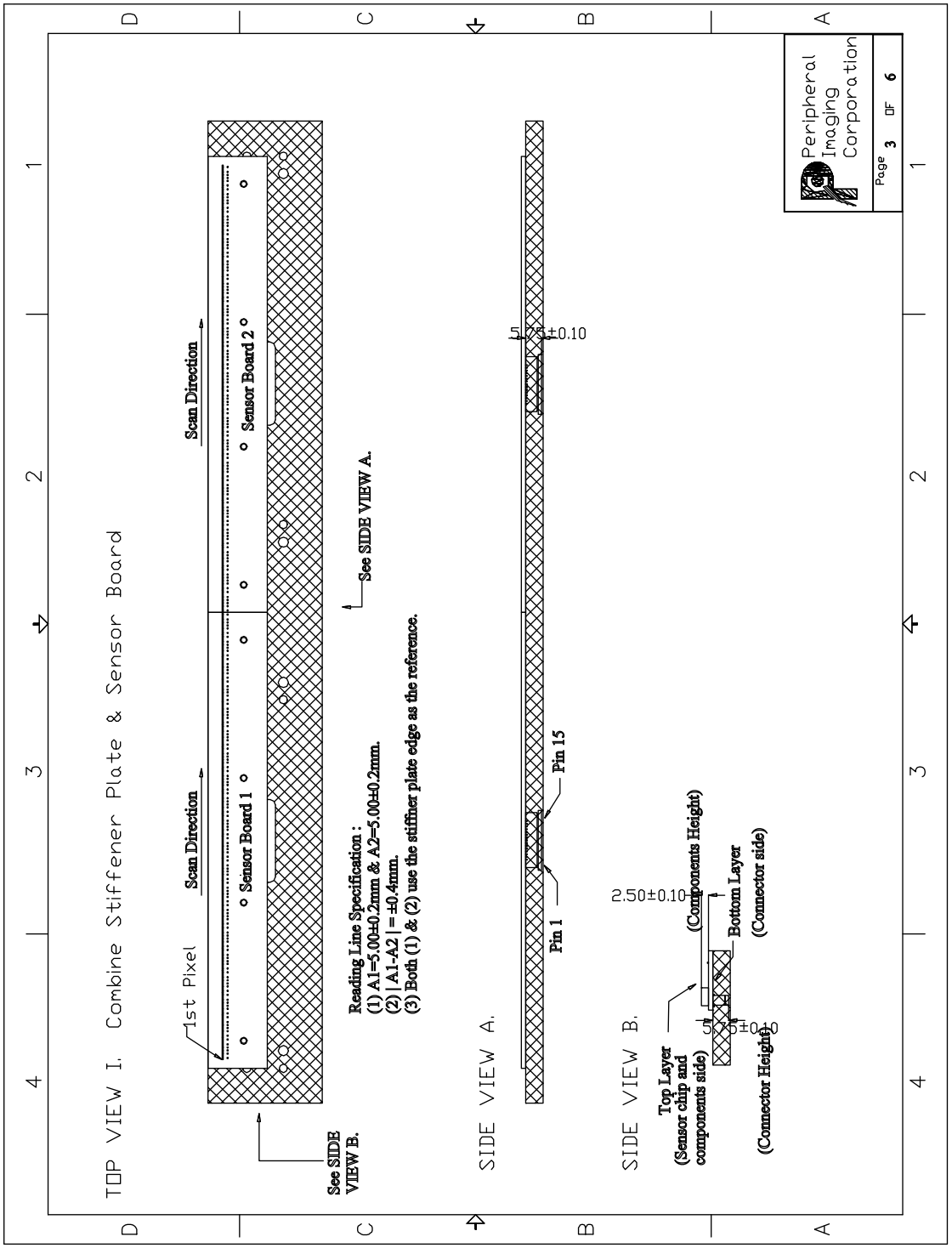
Pin	Description
1	CLK
2	SP
3	GND
4	VDD
5	GND
6	GND
7	GND
8	VSEC1
9	Agnd
10	VSEC2
11	Agnd
12	VSEC3
13	Agnd
14	VSEC4
15	Agnd

Pin	Description Row A	Description Row B	Description Row C
1	VDD	VDD	Agnd
2	VDD	VDD	Vout 1
3	No connect	No connect	Agnd
4	GND	GND	Agnd
5	SP	GND	Agnd
6	No connect	GND	Vout 2
7	No connect	GND	Agnd
8	No connect	GND	Agnd
9	CLK	GND	Agnd
10	GND	GND	Vout 3
11	No connect	GND	Agnd
12	No connect	GND	Agnd
13	No connect	GND	Agnd
14	GND	GND	Vout 4
15	No connect	No connect	Agnd
16	VSS	VSS	Agnd

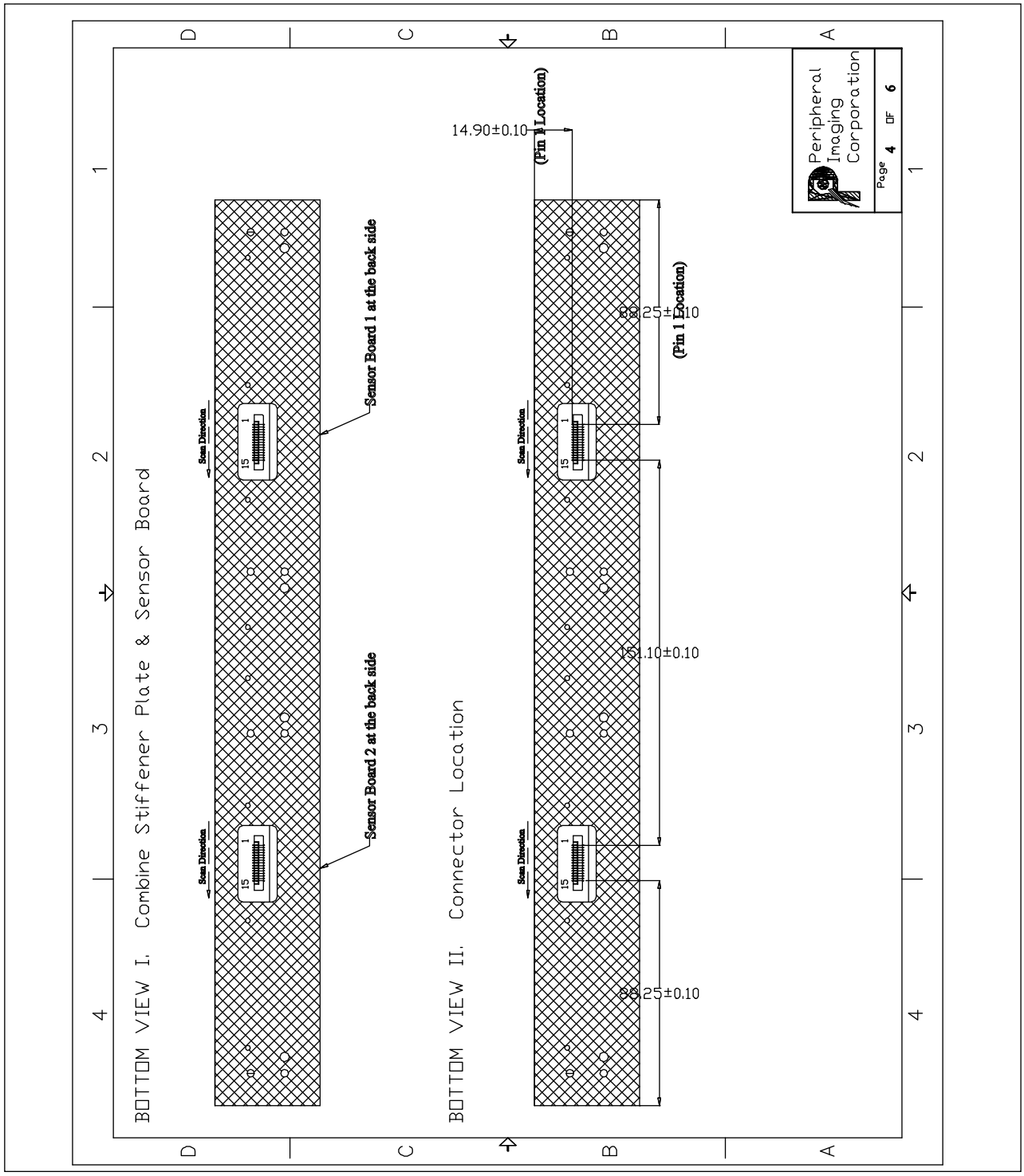
DRW 1. TOP ASSEMBLE OUTLINE



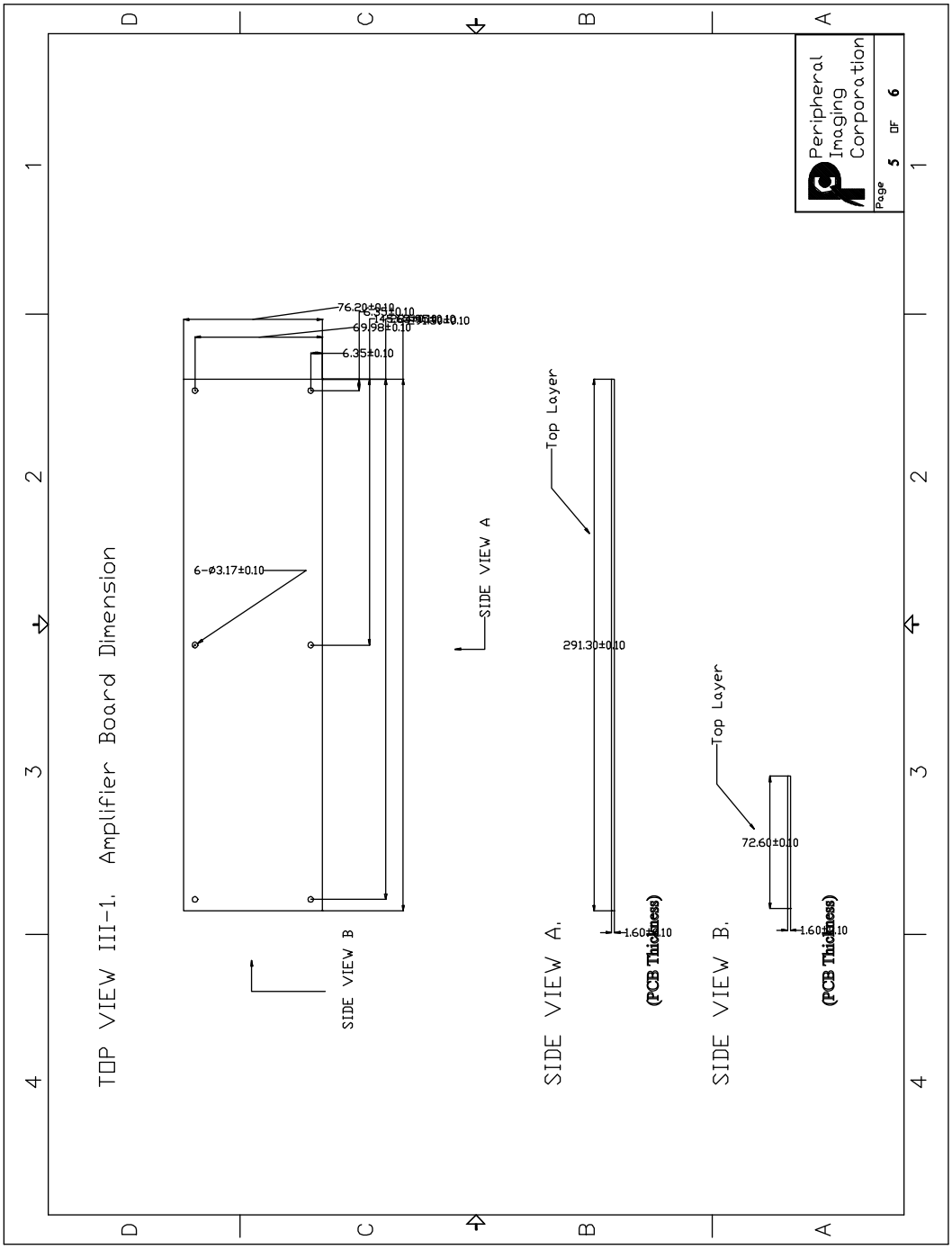
DRW 2. STIFFENER PLATE



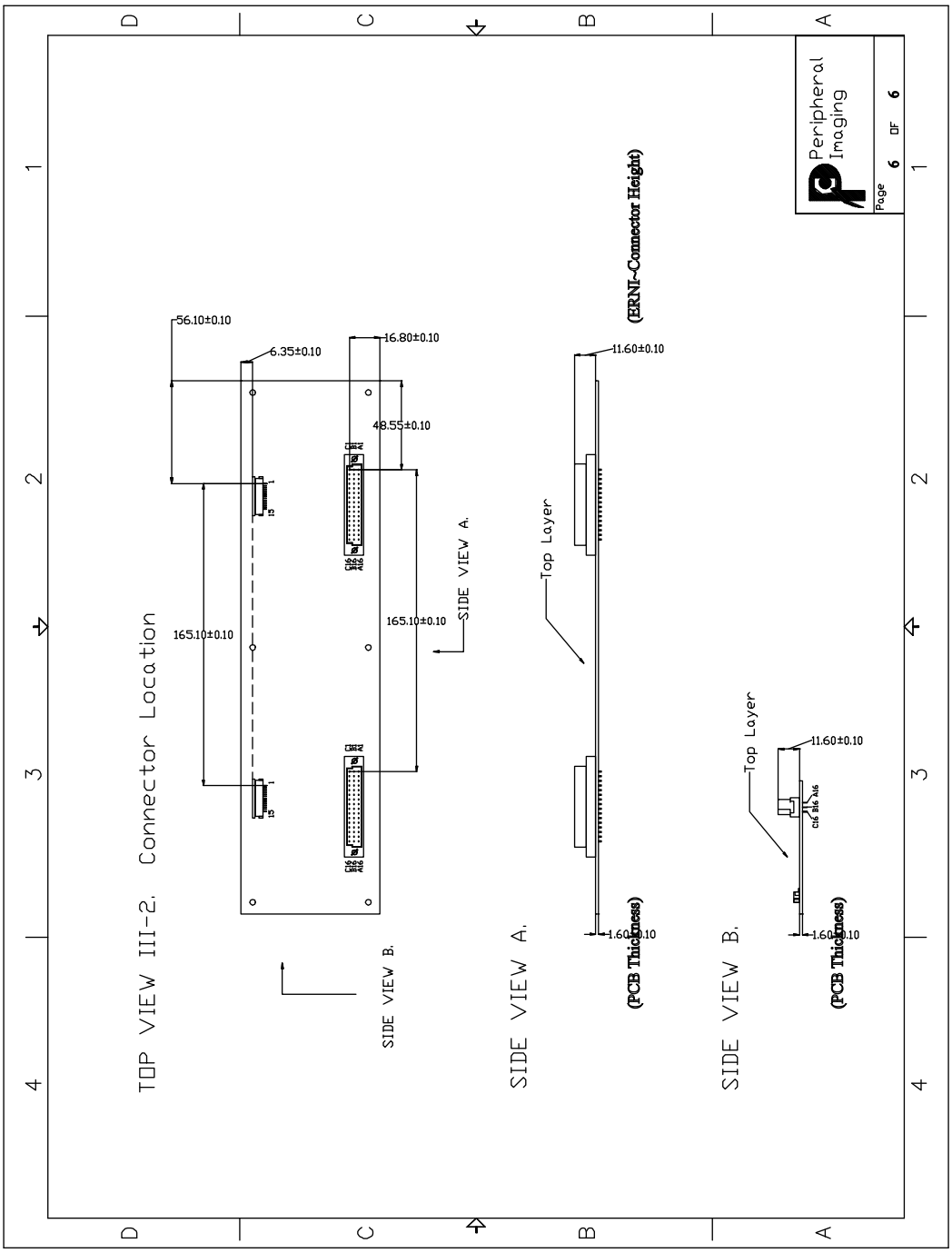
DRW 3. TWO SENSOR BOARD



DRW 4. CONNECTORS ON STIFFENER



DRW 5. AMPLIFIER BOARD



DRW 6. AMPLIFIER BOARD WITH CONNECTORS