

#### Features

- High-density 8 megabit Static RAM module
- Low profile 64-pin ZIP, 64 -pin SIMM (Single In-line Memory Module) or Angled SIMM.
- Ultra fast access time: 10 ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V ( $\pm 10\%$ ) power supply
- Multiple  $V_{SS}$  pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

#### Description

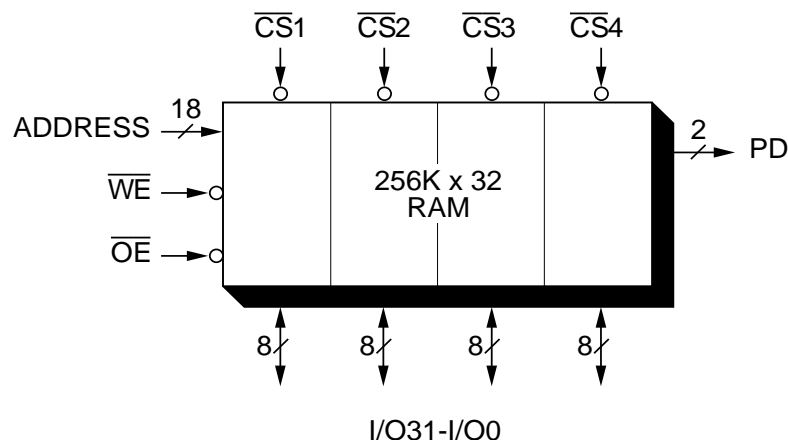
The PDM4M4050 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using eight 256K x 4 static RAMs in plastic SOJ packages. Availability of four chips select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 1 megabit static RAMs fabricated in Paradigm's high-performance, high-reliability technology. The PDM4M4050 is available with access time as fast as 10 ns with minimal power consumption.

The PDM4M4050 is packaged in a 64-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64-pin SIMM (Single In-line Memory Module). The Angled SIMM configuration allows 64 pins to be placed on a package 3.50" long and 0.35" wide and 0.68" high. The SIMM configuration also allows use of edge mounted sockets to secure the module.

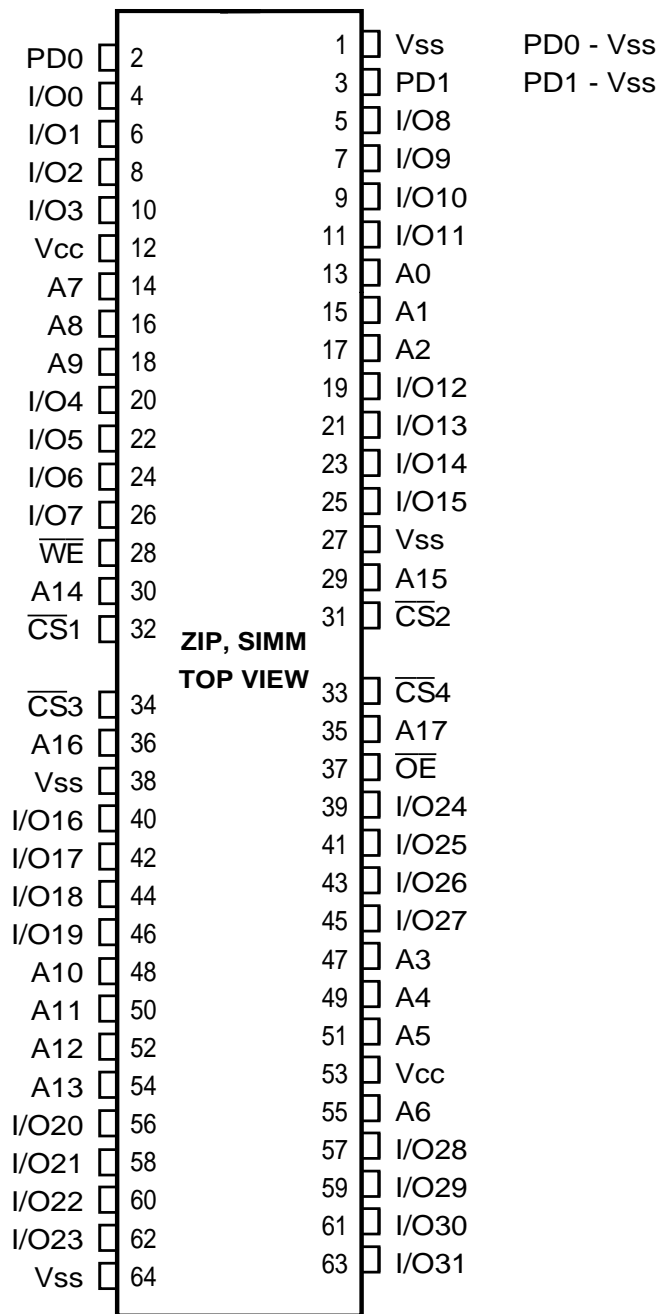
All inputs and outputs of the PDM4M4050 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 256K depth.

#### Functional Block Diagram



**Pin Configuration<sup>(1)</sup>**



**Pin Assignment**

Pin	Signal
I/O31-I/O0	Data Inputs/Outputs
A17-A0	Addresses
CS4-CS1	Chip Selects
WE	Write Enable
OE	Output Enable
PD1-PD0	Depth Identification
Vcc	Power
Vss	Ground

NOTE: 1. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the density of the module. If PD0 reads V<sub>SS</sub> and PD1 reads V<sub>SS</sub> then the module has a 256K depth.

**Truth Table**

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Deselect/ Power-down	H	X	X	High-Z	Standby
Read	L	L	H	DATA <sub>OUT</sub>	Active
Write	L	X	L	DATA <sub>IN</sub>	Active
Deselect	L	H	H	High-Z	Active

**Absolute Maximum Ratings<sup>(1)</sup>**

Symbol	Rating	Com'l.	Ind.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to V <sub>SS</sub>	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-10 to +85	-10 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
T <sub>A</sub>	Operating Temperature	0 to +70	0 to +70	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Recommended DC Operating Conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C

**DC Electrical Characteristics** ( $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ )

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$I_{LI}$	Input Leakage Current (Address)	$V_{CC} = \text{Max.}, V_{IN} = V_{SS} \text{ to } V_{CC}$	—	80	$\mu A$
$I_{LI}$	Input Leakage Current (Data)	$V_{CC} = \text{Max.}, V_{IN} = V_{SS} \text{ to } V_{CC}$	—	10	$\mu A$
$I_{LO}$	Output Leakage Current	$V_{OUT} = V_{SS} \text{ to } V_{CC}, V_{CC} = \text{Max.}, \overline{CS} = V_{IH}$	—	10	$\mu A$
$V_{OL}$	Output Low Voltage	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min.}$	—	0.4	V
$V_{OH}$	Output High Voltage	$I_{OL} = -4 \text{ mA}, V_{CC} = \text{Min.}$	2.4	—	V
$V_{IH}$	Input High Voltage		2.2	6.0	V
$V_{IL}$	Input Low Voltage		-0.5 <sup>(1)</sup>	0.8	V

NOTE 1.  $V_{IL} = -1.5V$  for pulse widths less than 10 ns, once per cycle.

**Power Supply Characteristics**

Symbol	Parameter	10 ns - 15 ns <sup>(1)</sup> Max	20 ns - 25 ns <sup>(1)</sup> Max	Unit
$I_{CC}$	Operating Current $\overline{CS} = V_{IL}, V_{CC} = \text{Max.}, f = f_{MAX}, \text{Outputs Open}$	1600	1360	mA
$I_{SB}$	Standby Current $\overline{CS} \geq V_{IH}, V_{CC} = \text{Max.}, f = f_{MAX}, \text{Outputs Open}$	480	480	mA
$I_{SB1}$	Full Standby Current $\overline{CS} \geq V_{CC} - 0.2V,$ $f = 0, V_{IN} > V_{CC} - 0.2V \text{ or } < 0.2V, \text{Outputs Open}$	320	120	mA

NOTE 1. Preliminary specification only.

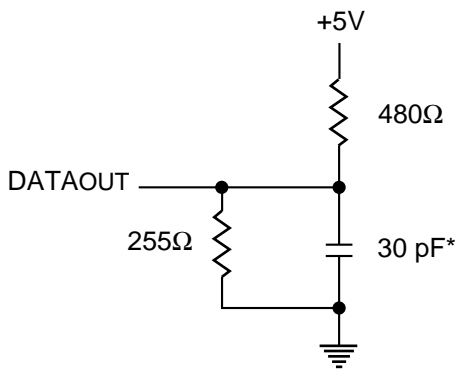
**Capacitance<sup>(1)</sup>** ( $T_A = +25^\circ C, f = 1.0 \text{ MHz}$ )

Symbol	Parameter	Max.	Unit
$C_{IN(C)}$	Input Capacitance, ( $\overline{CS}$ ) $V_{IN} = 0V$	20	pF
$C_{IN(A)}$	Input Capacitance, (Address and Control) $V_{IN} = 0V$	70	pF
$C_{I/O}$	I/O Capacitance $V_{OUT} = 0V$	12	pF

NOTE 1. This parameter is determined by device characteristics but is not production tested.

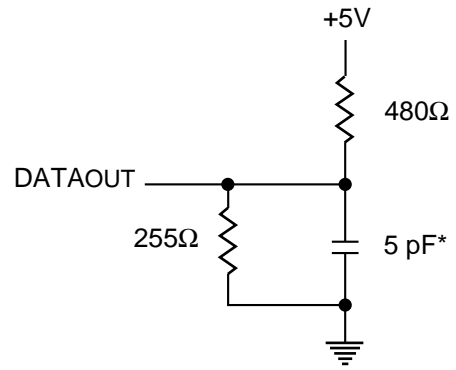
**AC Test Conditions**

Input Pulse Levels	$V_{SS}$ to 3.0V
Input Rise/Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 - 4



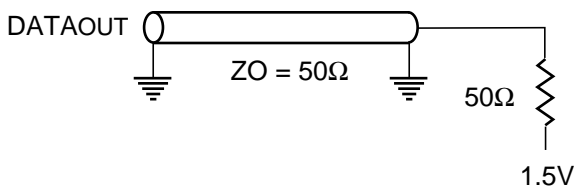
\* Including scope and jig capacitances

**Figure 1. Output Load**

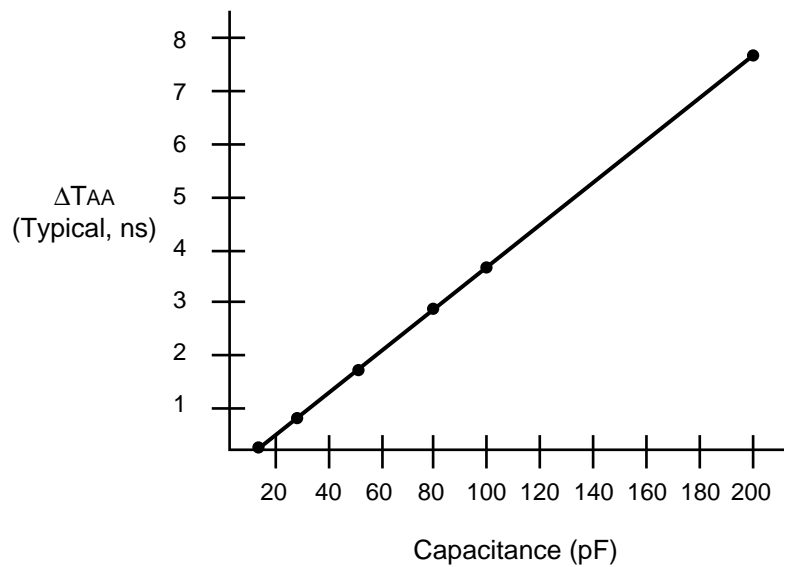


\* Including scope and jig capacitances

**Figure 2. Output Load**  
(for tOHZ, tCHZ, tOLZ, and tCLZ)



**Figure 3. Alternate Output Load**



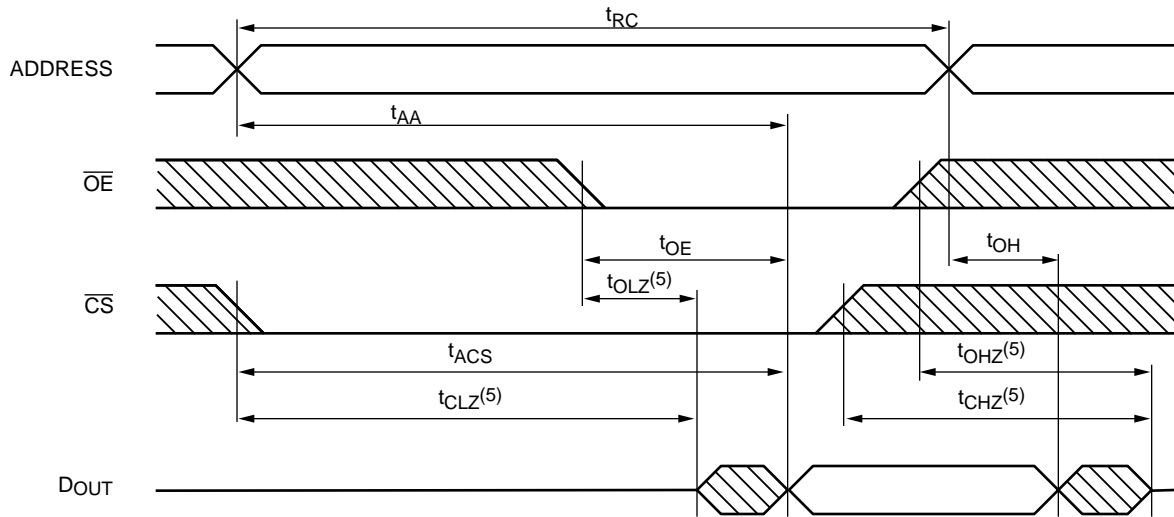
**Figure 4. Alternate Lumped Capacitive Load, Typical Derating**

**AC Electrical Characteristics** ( $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ )

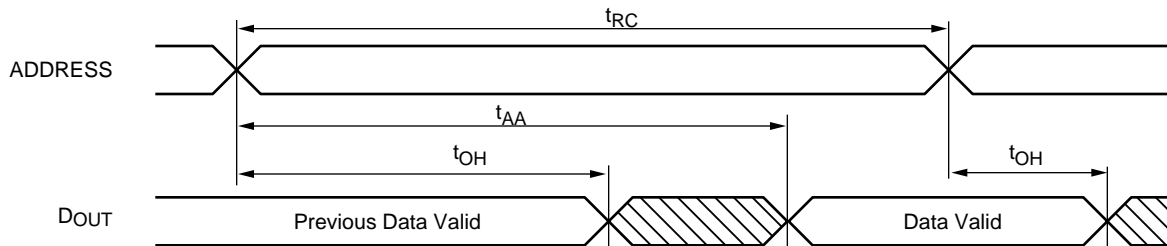
Symbol	Parameter	PDM4M4050SXXZ, PDM4M4050SXXM										Unit
		-10 ns <sup>(2)</sup>		-12 ns <sup>(2)</sup>		-15 ns <sup>(2)</sup>		-20 ns		-25 ns		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>												
t <sub>RC</sub>	Read Cycle Time	10	—	12	—	15	—	20	—	25	—	ns
t <sub>AA</sub>	Address Access Time	—	10	—	12	—	15	—	20	—	25	ns
t <sub>ACS</sub>	Chip Select Access Time	—	10	—	12	—	15	—	20	—	25	ns
t <sub>CLZ</sub> <sup>(1)</sup>	Chip Select to Output in Low-Z	2	—	2	—	2	—	5	—	5	—	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	5	—	7	—	8	—	10	—	12	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t <sub>CHZ</sub> <sup>(1)</sup>	Chip Deselect to Output in High-Z	—	6	—	7	—	8	—	10	—	12	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Disable to Output in High-Z	—	6	—	7	—	8	—	10	—	10	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
<b>Write Cycle</b>												
t <sub>WC</sub>	Write Cycle Time	10	—	12	—	15	—	—	20	—	25	ns
t <sub>CW</sub>	Chip Select to End of Write	8	—	10	—	12	—					ns
t <sub>AW</sub>	Address Valid to End of Write	8	—	10	—	12	—	20	—	25	—	ns
t <sub>AS</sub>	Address Setup Time	0	—	0	—	0	—	15	—	20	—	ns
t <sub>WP</sub>	Write Pulse Width	8	—	10	—	12	—	15	—	20	—	ns
t <sub>WR</sub>	Write Recovery Time	1	—	1	—	1	—	0	—	0	—	ns
t <sub>WHZ</sub> <sup>(1)</sup>	Write Enable to Output in High-Z	—	5	—	6	—	7	15	—	20	—	ns
t <sub>DW</sub>	Data to Write Time Overlap	6	—	7	—	8	—	0	—	0	—	ns
t <sub>DH</sub>	Data Hold from Write Time	1	—	1	—	1	—	—	13	—	15	ns
t <sub>OW</sub> <sup>(1)</sup>	Output Active from End of Write	1	—	1	—	1	—	12	—	15	—	ns

- NOTES 1. This parameter is determined by device characteristics but is not production tested.  
 2. Preliminary specifications only.

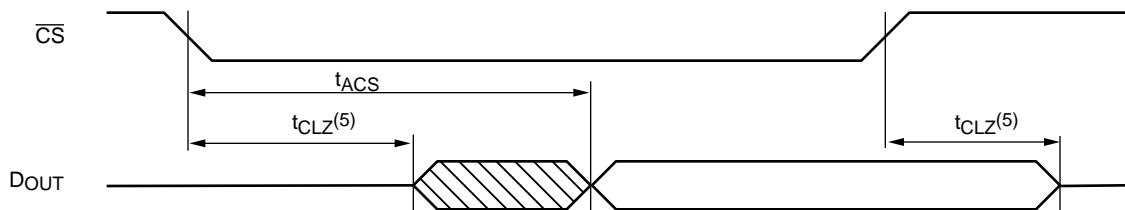
**Timing Waveforms of Read Cycle No.1<sup>(1)</sup>**



**Timing Waveforms of Read Cycle No.2<sup>(1,2,4)</sup>**

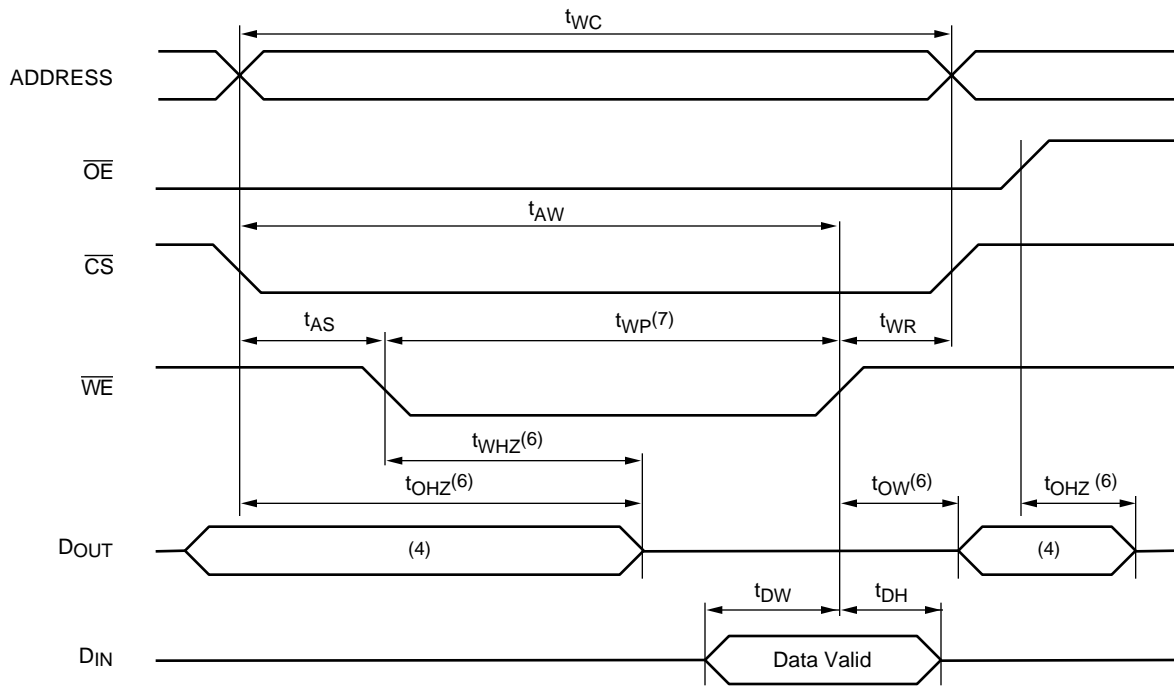


**Timing Waveforms of Read Cycle No.3<sup>(1,3,4)</sup>**

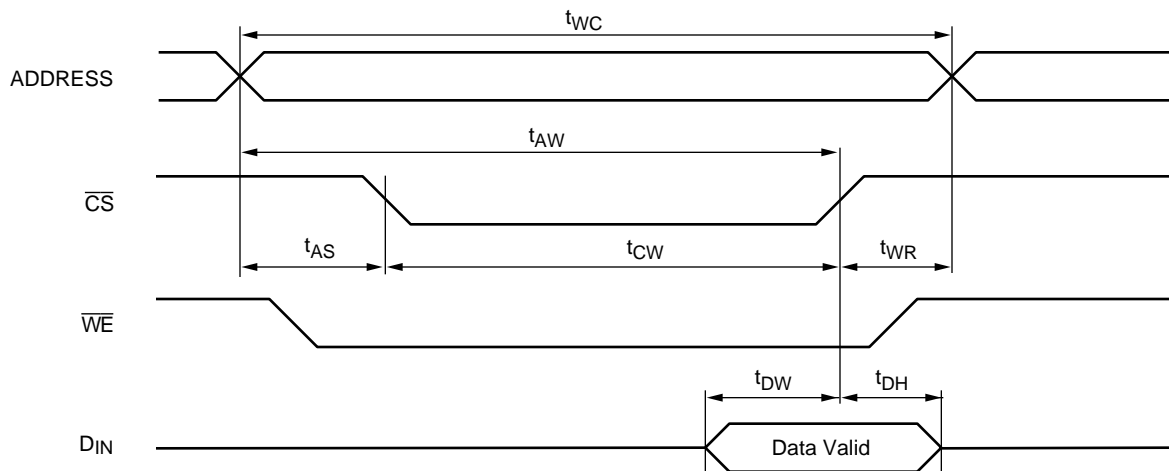


- NOTES
1.  $\overline{WE}$  is HIGH for Read Cycle.
  2. Device is continuously selected.  $\overline{CS} = V_{IL}$ .
  3. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
  4.  $\overline{OE} = V_{IL}$ .
  5. Transition is measured  $\pm 200$  mV for steady state. This parameter is determined by device characteristics but is not production tested.

Timing Waveforms of Write Cycle No.1 ( $\overline{WE}$  Controlled)<sup>(1,2,3,7)</sup>



Timing Waveforms of Write Cycle No.2 ( $\overline{CS}$  Controlled)<sup>(1,2,3,5)</sup>

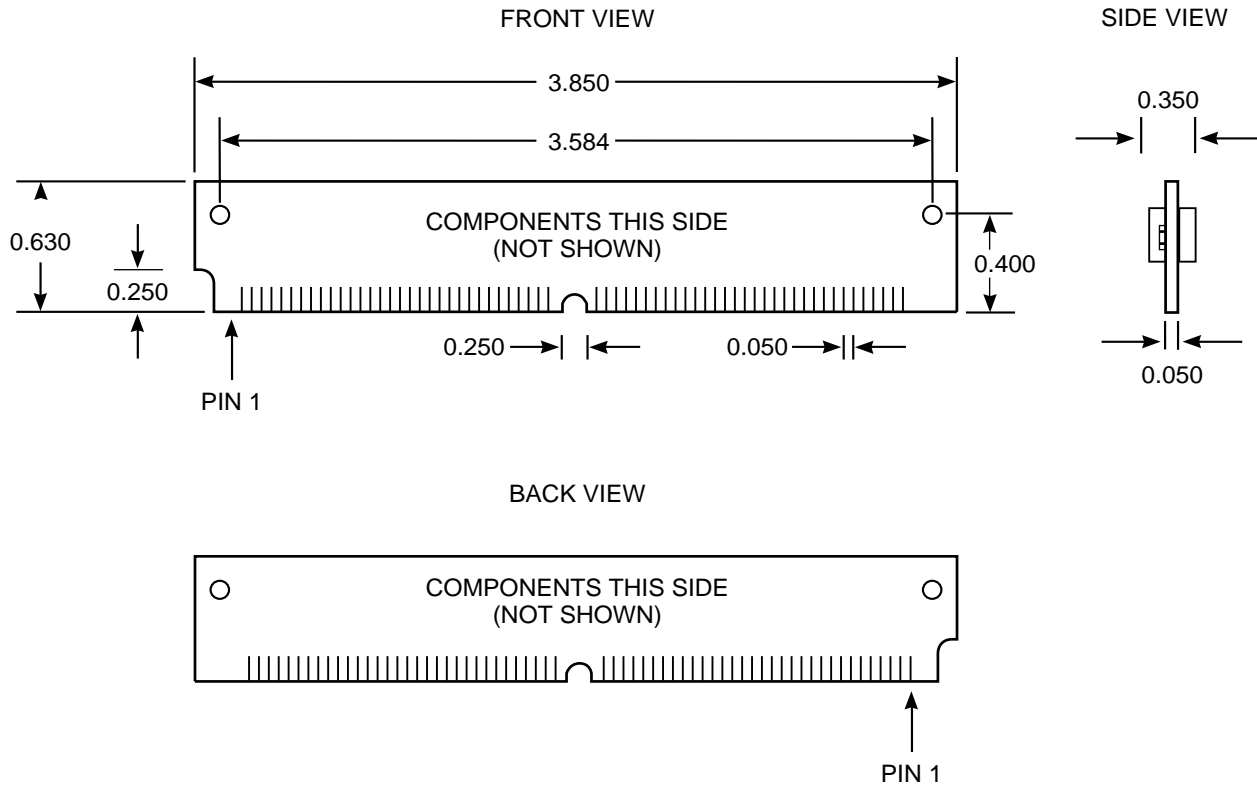


- NOTES
- $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
  - A write occurs during the overlap ( $t_{WP}$ ) of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
  - $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to end the write cycle.
  - During this period, I/O pins are in the output state, and input signals must be applied.
  - If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
  - Transition is measured  $\pm 200$  mV for steady state with a 5 pF load (including scope and jig). This parameter is determined by device characteristics but is not production tested.
  - If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WHZ} + t_{DW}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse width can be as short as the specified  $t_{WP}$ .

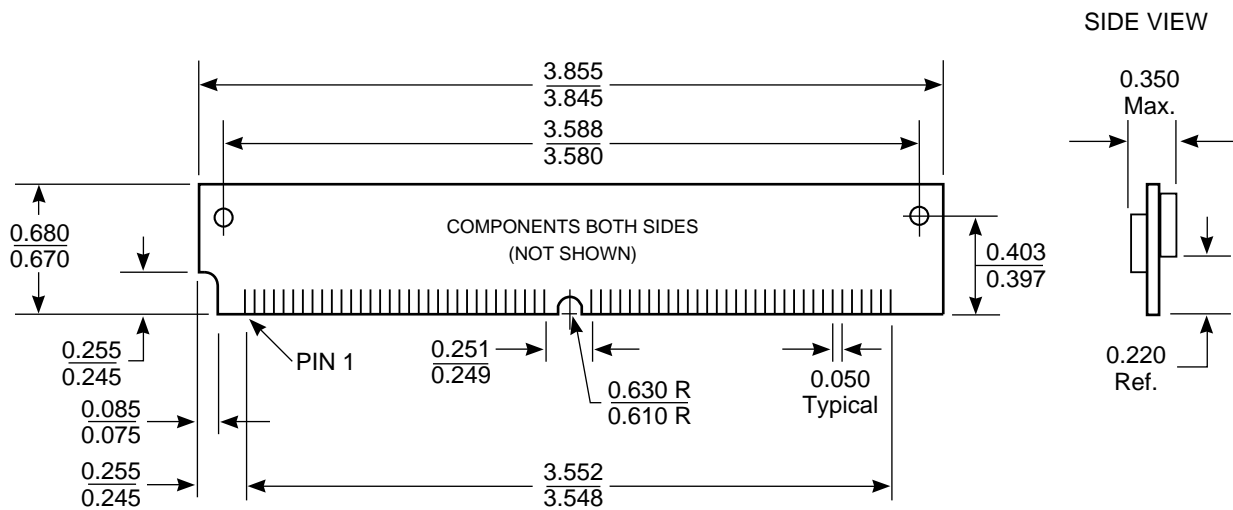


Package Dimensions

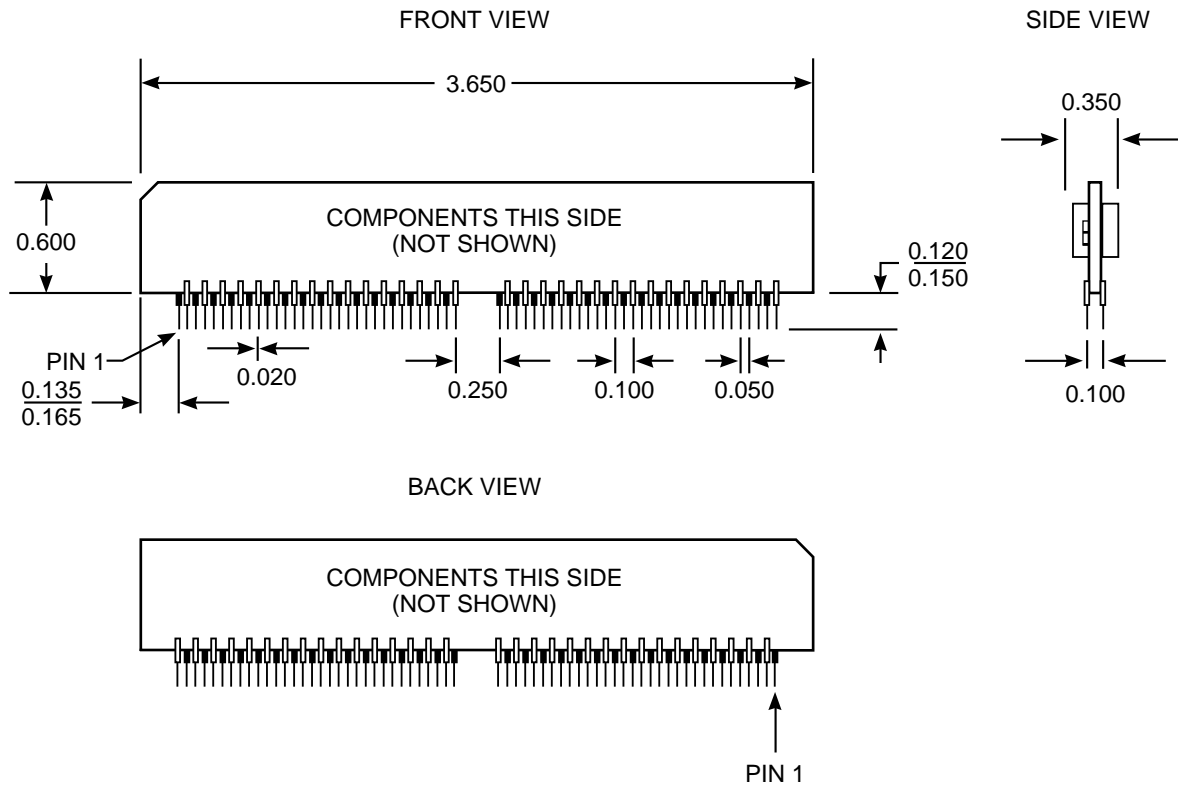
SIMM Version



Angled SIMM Version



ZIP Version



Ordering Information

