DATA SHEET

PDI1394P25

1-port 400 Mbps physical layer interface

Preliminary data
Supersedes data of 2001 Jul 18

2001 Sep 06

Philips
Semiconductors

PHILIPS

1-port 400 Mbps physical layer interface PDI1394P25

1.0 FEATURES

- Fully supports provisions of IEEE 1394–1995 Standard for high performance serial bus and the P1394a–2000 Standard[1]
- Fully interoperable with Firewire™ and i.LINK™ implementations of the IEEE 1394 Standard.[2]
- Full P1394a support includes:
  - Connection debounce
  - Arbitrated short reset
  - Multispeed concatenation
  - Arbitration acceleration
  - Fly-by concatenation
  - Port disable/suspend/resume
- Provides one 1394a fully-compliant cable port at 100/200/400 Mbps. Can be used as a one port PHY without the use of any extra external components
- Fully compliant with Open HCI requirements
- Cable ports monitor line conditions for active connection to remote node.
- Power down features to conserve energy in battery-powered applications include:
  - Automatic device power down during suspend
  - Device power down terminal
  - Link interface disable via LPS
  - Inactive ports powered-down
- Logic performs system initialization and arbitration functions
- Encode and decode functions included for data-strobe bit level encoding
- Incoming data resynchronized to local clock
- Single 3.3 volt supply operation
- Minimum V_{DD} of 2.7 V for end-of-wire power-consuming devices
- While unpowered and connected to the bus, will not drive TPBIAS on a connected port, even if receiving incoming bias voltage on that port
- Supports extended bias-handshake time for enhanced interoperability with camcorders
- Interface to link-layer controller supports both low-cost bus-holder isolation and optional Annex J electrical isolation
- Data interface to link-layer controller through 2/4/8 parallel lines at 49.152 MHz
- Low-cost 24.576 MHz crystal provides transmit, receive data at 100/200/400 Mbps, and link-layer controller clock at 49.152 MHz
- Does not require external filter capacitors for PLL
- Interoperable with link-layer controllers using 3.3 V and 5 V supplies
- Interoperable with other Physical Layers (PHYs) using 3.3 V and 5 V supplies
- Node power class information signaling for system power management
- Cable power presence monitoring
- Separate cable bias (TPBIAS) for each port
- Register bits give software control of contender bit, power class bits, link active bit, and 1394a features
- LQFP package is function and pin compatible with the Texas Instruments TSB41LV01E™ and TSB41AB1™ (PAP package) 400 Mbps PHYs.

2.0 DESCRIPTION

The PDI1394P25 provides the digital and analog transceiver functions needed to implement a one port node in a cable-based IEEE 1394–1995 and/or 1394a network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The PDI1394P25 is designed to interface with a Link Layer Controller (LLC), such as the PDI1394L40 or PDI1394L41.

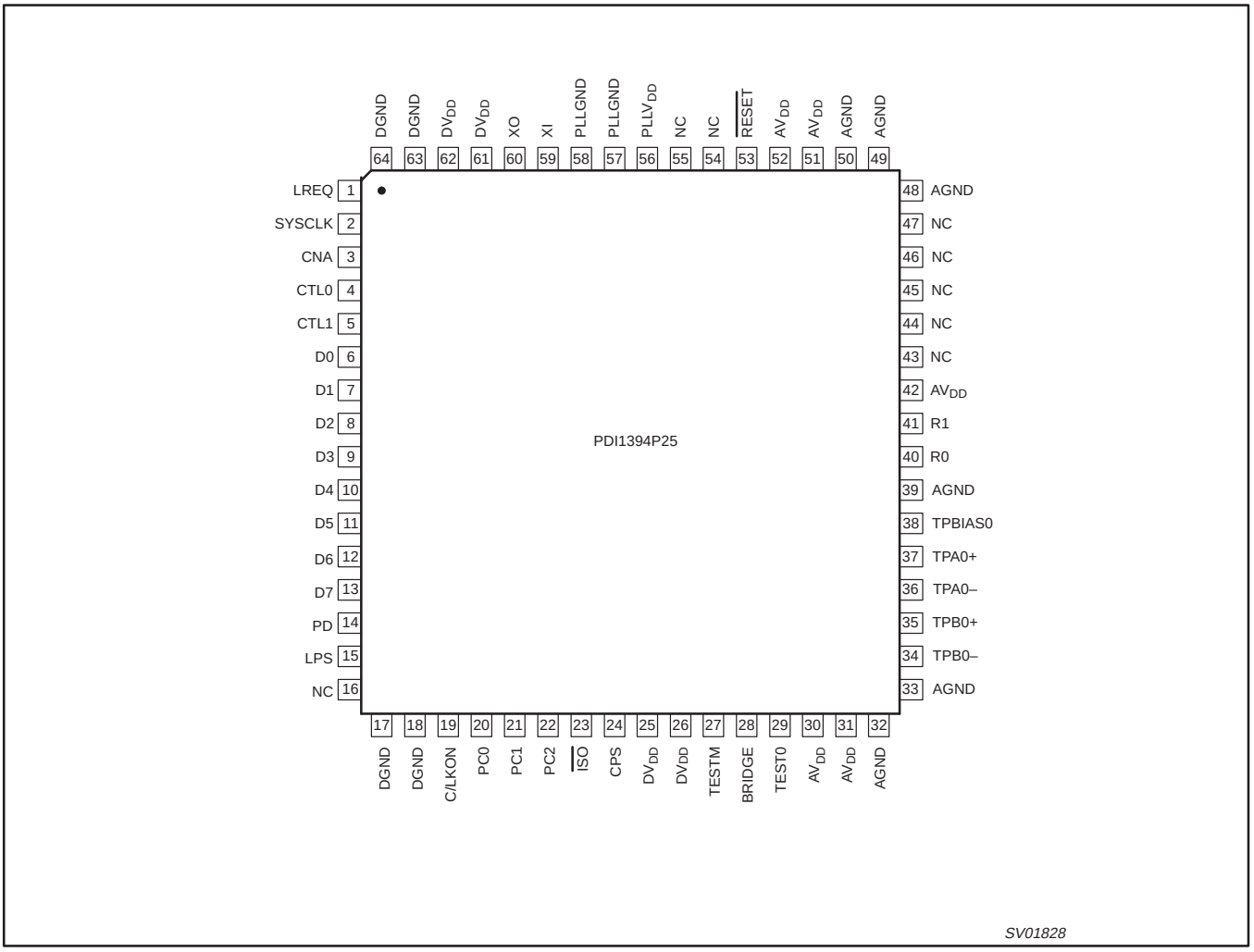
3.0 ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDER CODE	PKG. DWG. #
64-pin plastic LQFP	0 to +70°C	PDI1394P25BD	SOT314-2
64-ball plastic LFBGA	0 to +70°C	PDI1394P25EC	SOT534-1

1. Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thompson, Limited.
2. Firewire is a trademark of Apple Computer Inc. i.LINK is a trademark of Sony.

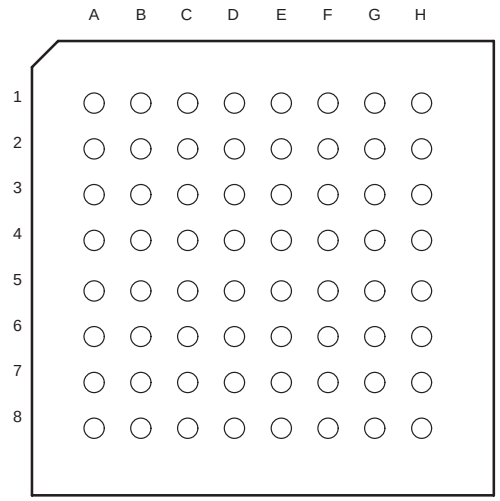
4.0 PIN AND BALL CONFIGURATION

4.1 LQFP CONFIGURATION



4.2 LFBGA CONFIGURATION

BOTTOM (BALL) VIEW



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Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A1	AGND	C1	$\overline{\text{RESET}}$	E1	PLLGND	G1	DGND
A2	NC	C2	AV_{DD}	E2	XI	G2	DGND
A3	NC	C3	AV_{DD}	E3	XO	G3	CTL0
A4	R1	C4	NC	E4	D2	G4	CTL1
A5	AGND	C5	AV_{DD}	E5	CPS	G5	D5
A6	TPBIAS0	C6	TPB0+	E6	DV_{DD}	G6	PD
A7	TPB0–	C7	AV_{DD}	E7	PC1	G7	DGND
A8	AGND	C8	TEST0	E8	$\overline{\text{ISO}}$	G8	DGND
B1	AGND	D1	$PLLV_{DD}$	F1	DV_{DD}	H1	LREQ
B2	AGND	D2	AV_{DD}	F2	DV_{DD}	H2	SYSCLK
B3	NC	D3	PLLGND	F3	CNA	H3	D0
B4	NC	D4	$PLLV_{DD}$	F4	D4	H4	D1
B5	TPA0+	D5	R0	F5	D6	H5	D3
B6	TPA0–	D6	BRIDGE	F6	C/LKON	H6	D7
B7	AGND	D7	TESTM	F7	PC0	H7	LPS
B8	AV_{DD}	D8	DV_{DD}	F8	PC2	H8	DGND

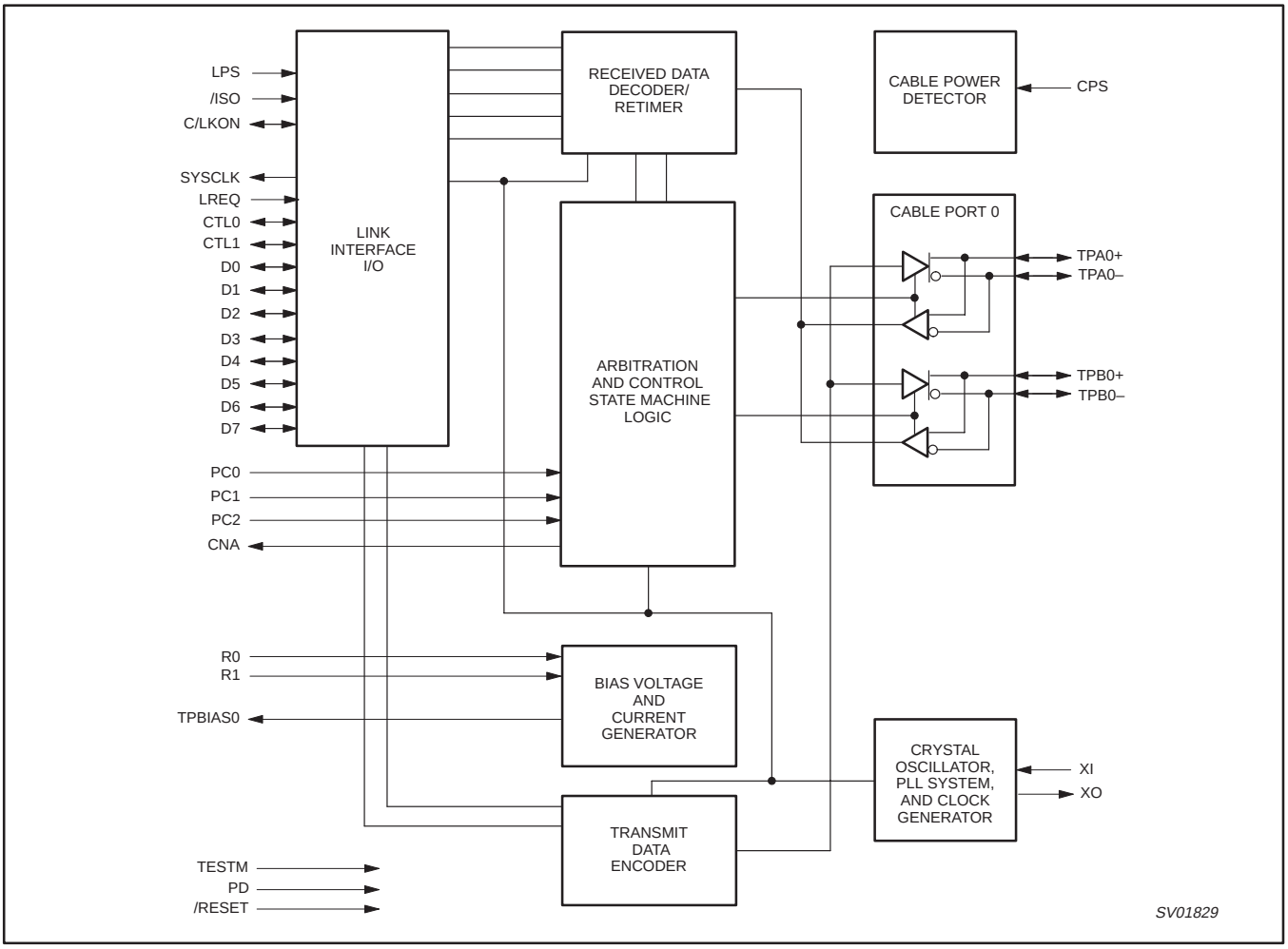
5.0 PIN DESCRIPTION

Name	Pin Type	LQFP Pin Numbers	LFBGA Ball Numbers	I/O	Description
AGND	Supply	32, 33, 39, 48, 49, 50	A1, A5, A8, B1, B2, B7	—	Analog circuit ground terminals. These terminals should be tied together to the low impedance circuit board ground plane.
AV_{DD}	Supply	30, 31, 42, 51, 52	B8, C2, C3, C5, C7, D2	—	Analog circuit power terminals. A combination of high frequency decoupling capacitors on each side are suggested, such as paralleled 0.1 µF and 0.001 µF. These supply terminals are separated from $PLLV_{DD}$ and DV_{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
BRIDGE	CMOS	28	D6	I	BRIDGE input. This input is used to set the Bridge_Aware bits located in the Vendor-Dependent register Page 7, base address 1001_b, bit positions 6 and 7. This pin is sampled during a hardware reset ($\overline{\text{RESET}}$ low). When the BRIDGE pin is tied low (or through a 1 kΩ resistor to accommodate other vendor's pin-compatible chips), the Bridge_Aware bits are set to "00" indicating a "non-bridge device." When the BRIDGE pin is tied high, the Bridge_Aware bits are set to "11" indicating a "1394.1 bridge compliant" device. The default setting of the Bridge_Aware bits can be overridden by writing to the register. The Bridge_Aware bits are reported in the self-ID packet at bit positions 18 and 19.
C/LKON	CMOS 5 V tol	19	F6	I/O	Bus Manager Contender programming input and link-on output. On hardware reset, this terminal is used to set the default value of the contender status indicated during self-ID. Programming is done by tying the terminal through a 10-kΩ resistor to a high (contender) or low (not contender). The resistor allows the link-on output to override the input. If this pin is connected to a LLC driver pin for setting Bus Manager/IRM contender status, then a 10-kΩ series resistor should be placed on this line between the PHY and the LLC to prevent possible contention. In this case. the pull-high or pull-low resistors mentioned in the previous paragraph should not be used. Refer to Figure 9. Following hardware reset, this terminal is the link-on output, which is used to notify the LLC to power-up and become active. The link-on output is a square-wave signal with a period of approximately 163 ns (8 SYSCLK cycles) when active. The link-on output is otherwise driven low, except during hardware reset when it is high impedance. The link-on output is activated if the LLC is inactive (LPS inactive or the LCtrl bit cleared) and when: a) the PHY receives a link-on PHY packet addressed to this node, b) the PEI (port-event interrupt) register bit is 1, or c) any of the CTOI (configuration-timeout interrupt), CPSI (cable-power-status interrupt), or STOI (state-timeout interrupt) register bits are 1 and the RPIE (resuming-port interrupt enable) register bit is also 1. Once activated, the link-on output will continue active until the LLC becomes active (both LPS active and the LCtrl bit set). The PHY also deasserts the link-on output when a bus-reset occurs unless the link-on output would otherwise be active because one of the interrupt bits is set (i.e., the link-on output is active due solely to the reception of a link-on PHY packet). NOTE: If an interrupt condition exists which would otherwise cause the link-on output to be activated if the LLC were inactive, the link-on output will be activated when the LLC subsequently becomes inactive.
CNA	CMOS	3	F3	O	Cable Not Active output. This terminal is asserted high when there are no ports receiving incoming bias voltage.
CPS	CMOS	24	E5	I	Cable Power Status input. This terminal is normally connected to cable power through a 390 kΩ resistor. This circuit drives an internal comparator that is used to detect the presence of cable power.
CTL0, CTL1	CMOS 5 V tol	4 5	G3 G4	I/O	Control I/Os. These bi-directional signals control communication between the PDI1394P25 and the LLC. Bus holders are built into these terminals.

Name	Pin Type	LQFP Pin Numbers	LFBGA Ball Numbers	I/O	Description
D0–D7	CMOS 5 V tol	6, 7, 8, 9, 10, 11, 12, 13	H3, H4, E4, H5, F4, G5, F5, H6	I/O	Data I/Os. These are bi-directional data signals between the PDI1394P25 and the LLC. Bus holders are built into these terminals. Unused Dn pins should be pulled to ground through 10 kΩ resistors.
DGND	Supply	17, 18, 63, 64	G1, G2, G7, G8, H8	—	Digital circuit ground terminals. These terminals should be tied together to the low impedance circuit board ground plane.
DV_{DD}	Supply	25, 26, 61, 62	D8, E6, F1, F2	—	Digital circuit power terminals. A combination of high frequency decoupling capacitors near each side of the IC package are suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply terminals are separated from $PLLV_{DD}$ and AV_{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
$\overline{ISO}$	CMOS	23	E8	I	Link interface isolation control input. This terminal controls the operation of output differentiation logic on the CTL and D terminals. If an optional isolation barrier of the type described in Annex J of IEEE Std 1394–1995 is implemented between the PDI1394P25 and LLC, the $\overline{ISO}$ terminal should be tied low to enable the differentiation logic. If no isolation barrier is implemented (direct connection), or bus holder isolation is implemented, the $\overline{ISO}$ terminal should be tied high to disable the differentiation logic.
LPS	CMOS 5 V tol	15	H7	I	Link Power Status input. This terminal is used to monitor the active/power status of the link layer controller and to control the state of the PHY-LLC interface. This terminal should be connected to either the V_{DD} supplying the LLC through a 10 kΩ resistor, or to a pulsed output which is active when the LLC is powered. A pulsed signal should be used when an isolation barrier exists between the LLC and PHY. (See Figure 8) The LPS input is considered inactive if it is sampled low by the PHY for more than 2.6 μs (128 SYSCLK cycles), and is considered active otherwise (i.e., asserted steady high or an oscillating signal with a low time less than 2.6 μs). The LPS input must be high for at least 21 ns in order to be guaranteed to be observed as high by the PHY. When the PDI1394P25 detects that LPS is inactive, it will place the PHY-LLC interface into a low-power reset state. In the reset state, the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 μs (1280 SYSCLK cycles), the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is placed into the disabled state upon hardware reset. The LLC is considered active only if both the LPS input is active and the LCtrl register bit is set to 1, and is considered inactive if either the LPS input is inactive or the LCtrl register bit is cleared to 0.
LREQ	CMOS 5 V tol	1	H1	I	LLC Request input. The LLC uses this input to initiate a service request to the PDI1394P25. Bus holder is built into this terminal.
NC	No connect	54, 55		—	These pins are not internally connected and consequently are “don’t cares”. **Other vendors’ pin compatible chips may require connections and external circuitry on these pins.**
NC	No connect	16, 43, 44, 45, 46, 47	A2, A3, B3, B4, C4	—	No connect.
PC0 PC1 PC2	CMOS 5 V tol	20 21 22	F7 E7 F8	I	Power Class programming inputs. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying the terminals high or low. Refer to Table 21 for encoding.
PD	CMOS 5 V tol	14	G6	I	Power Down input. A logic high on this terminal turns off all internal circuitry except the cable-active monitor circuits which control the CNA output. For more information, refer to Section 17.2

Name	Pin Type	LQFP Pin Numbers	LFBGA Ball Numbers	I/O	Description
PLLGND	Supply	57, 58	D3, E1	—	PLL circuit ground terminals. These terminals should be tied together to the low impedance circuit board ground plane.
$PLLV_{DD}$	Supply	56	D1, D4	—	PLL circuit power terminals. A combination of high frequency decoupling capacitors near each terminal are suggested, such as paralleled 0.1 μF and 0.001 μF. These supply terminals are separated from DV_{DD} and AV_{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
$\overline{RESET}$	CMOS 5 V tol	53	C1	I	Logic reset input. Asserting this terminal low resets the internal logic. An internal pull-up resistor to V_{DD} is provided so only an external delay capacitor is required for proper power-up operation. For more information, refer to Section 17.2. This input is otherwise a standard Schmitt logic input, and can also be driven by an open-drain type driver.
R0 R1	Bias	40 41	D5 A4	—	Current setting resistor pins These pins are connected to an external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ ±1% is required to meet the IEEE 1394–1995 Std. output voltage limits.
SYSCLK	CMOS	2	H2	O	System clock output. Provides a 49.152 MHz clock signal, synchronized with data transfers, to the LLC.
TEST0	CMOS	29	C8	I	Test control input. This input is used in manufacturing tests of the PDI1394P25. For normal use, this terminal should be tied to GND.
TESTM	CMOS	27	D7	I	Test control input. This input is used in manufacturing tests of the PDI1394P25. For normal use, this input may be tied to V_{DD} (for compatibility with other vendors' pin-compatible PHY chips) or to PHY GND (when a PDI1394P25 is an alternate device).
TPA0+	Cable	37	B5	I/O	Twisted-pair cable A differential signal terminals. Board traces from each pair of positive and negative differential signal terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA0–	Cable	36	B6	I/O	
TPB0+	Cable	35	C6	I/O	Twisted-pair cable B differential signal terminals. Board traces from each pair of positive and negative differential signal terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB0–	Cable	34	A7	I/O	
TPBIAS0	Cable	38	A6	I/O	Twisted-pair bias output. This provides the 1.86 V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection. These terminals must be decoupled with a 0.3 μF–1 μF capacitor to ground.
XI XO	Crystal	59 60	E2 E3	—	Crystal oscillator inputs. These terminals connect to a 24.576 MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used. Can also be driven by an external clock generator (leave XO unconnected in this case and start supplying the external clock before resetting the PDI1394P25). For more information, refer to Section 17.5

6.0 BLOCK DIAGRAM



7.0 FUNCTIONAL SPECIFICATION

The PDI1394P25 requires only an external 24.576 MHz crystal as a reference. An external clock can be connected to XI instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216 MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded Strobe and Data information. A 49.152 MHz clock signal, supplied to the associated LLC for synchronization of the two chips, is used for resynchronization of the received data. The Power Down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL and disables all circuits except the cable bias detectors at the TPB terminals. The port transmitter circuitry and the receiver circuitry are also disabled when the port is disabled, suspended, or disconnected.

The PDI1394P25 supports an optional isolation barrier between itself and its LLC. When the $\overline{ISO}$ input terminal is tied high, the LLC interface outputs behave normally. When the $\overline{ISO}$ terminal is tied low, internal differentiating logic is enabled, and the outputs are driven such that they can be coupled through a capacitive or transformer galvanic isolation barrier as described in *IEEE 1394a section 5.9.4*. To operate with single capacitor (bus holder) isolation, the $\overline{ISO}$ on the PHY terminal must be tied high. For more details on using single capacitor isolation, please refer to the Philips Isolation Application Note AN2452.

Data bits to be transmitted through the cable ports are received from the LLC on two, four or eight parallel paths (depending on the requested transmission speed). They are latched internally in the PDI1394P25 in synchronization with the 49.152 MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304/196.608/393.216 Mbps (referred to as S100, S200, and S400 speed, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial

data bits are split into two-, four- or eight-bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152 MHz system clock and sent to the associated LLC.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission (speed signaling). In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage (cable bias detection).

The PDI1394P25 provides a 1.86 V nominal bias voltage at the TPBIAS terminal for port termination. The PHY contains two independent TPBIAS circuits. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 0.3 μF–1 μF.

The line drivers in the PDI1394P25 operate in a high-impedance current mode, and are designed to work with external 112 Ω line-termination resistor networks in order to match the 110 Ω cable impedance. One network is provided at each end of all twisted-pair cable connections. Each network is composed of a pair of series-connected 56 Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B terminals is coupled to ground through a parallel R-C network with recommended values of 5 kΩ and 220 pF. The values of the external line termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents. This current setting resistor has a value of 6.34 kΩ ±1%.

When the power supply of the PDI1394P25 is removed while the twisted-pair cables are connected, the PDI1394P25 transmitter and receiver circuitry presents a high impedance to the cable in order to not load the TPBIAS voltage on the other end of the cable.

The TEST0 terminal is used to set up various manufacturing test conditions. For normal operation, it should be connected to ground.

The TESTM terminal is used in manufacturing tests of the PDI1394P25. For normal use, it may be tied to either PHY V_{DD} (for compatability with other vendors' pin-compatible PHY chips) or to PHY GND (when a PDI1394P25 is an alternate device).

The BRIDGE terminal is used to set the default value of the Bridge_Aware bits i the Page 7 (Vendor Dependent) register. Tying BRIDGE low directly (or through a 1 kΩ resistor to accommodate other vendors' pin-compatible chips), defaults the Bridge_Aware field to "00" indicating a "non-bridge device." Tying BRIDGE high, defaults the Bridge_Aware bit to "11" indicating a "1394.1 bridge compliant" device. Writing to the Bridge_Aware field overrides the default setting from the BRIDGE terminal. The Bridge_Aware field is reported in the self-ID packet at bit positions 18 and 19.

Four package terminals, used as inputs to set the default value for four configuration status bits in the self-ID packet, should be hard-wired high or low as a function of the equipment design. The PC0–PC2 terminals are used to indicate the default power-class status for the node (the need for power from the cable or the ability to supply power to the cable). See Table 21 for power class encoding. The C/LKON terminal is used as an input to indicate that the node is a contender for bus manager.

The PHY supports suspend/resume as defined in the IEEE 1394a specification. The suspend mechanism allows pairs of directly connected ports to be placed into a low power state while maintaining a port-to-port connection between 1394 bus segments. While in a low power state, a port is unable to transmit or receive data transaction packets. However, a port in a low power state is capable of detecting connection status changes and detecting incoming TPBIAS. When the PDI1394P25's port is suspended, all circuits except the bias-detection circuits are powered down, resulting in significant power savings. The TPBIAS circuit monitors the value of incoming TPA pair common-mode voltage when local TPBIAS is inactive. Because this circuit has an internal current source and the connected node has a current sink, the monitored value indicates the cable connection status. This monitor is called connect-detect.

Both the cable bias-detect monitor and TPBIAS connect-detect monitor are used in suspend/resume signaling and cable connection detection. For additional details of suspend/resume operation, refer to the 1394a specification. The use of suspend/resume is recommended for new designs.

The port transmitter and receiver circuitry is disabled during power down (when the PD input terminal is asserted high), during reset (when the $\overline{\text{RESET}}$ input terminal is asserted low), when no active cable is connected to the port, or when controlled by the internal arbitration logic. The port twisted-pair bias voltage circuitry is disabled during power down, during reset, or when the port is disabled as commanded by the LLC.

The CNA (cable-not-active) terminal provides a high when the twisted-pair cable port is not receiving incoming bias (i.e., it is either disconnected or suspended), and can be used along with LPS to determine when to power-down the PDI1394P25. The CNA output is not debounced. When the PD terminal is asserted high, the CNA detection circuitry is enabled (regardless of the previous state of the ports) and a pull-down is activated on the $\overline{\text{RESET}}$ terminal so as to force a reset of the PDI1394P25 internal logic.

The LPS (link power status) terminal works with the C/LKON terminal to manage the power usage in the node. The LPS signal from the LLC is used in conjunction with the LCtrl bit (see Table 1 and Table 2) to indicate the active/power status of the LLC. The LPS signal is also used to reset, disable, and initialize the PHY-LLC interface (the state of the PHY-LCC interface is controlled solely by the LPS input regardless of the state of the LCtrl bit).

The LPS input is considered inactive if it remains low for more than 2.6 μs and is considered active otherwise. When the PDI1394P25 detects that LPS is inactive, it will place the PHY-LLC interface into a low-power reset state in which the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 μs, the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is also held in the disabled state during hardware reset. The PDI1394P25 will continue the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and LPS is again observed active, the PHY will initialize the interface and return it to normal operation.

The PHY uses the C/LKON terminal to notify the LLC to power up and become active. When activated, the C/LKON signal is a square wave of approximately 163 ns period. The PHY activates the C/LKON output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as described above, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY deasserts the C/LKON output when the LLC becomes active (both LPS active and the LCtrl bit set to 1). The PHY also deasserts the C/LKON output when a bus-reset occurs unless a PHY interrupt condition exists which would otherwise cause C/LKON to be active.

8.0 ABSOLUTE MAXIMUM RATINGS [1]

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC supply voltage		–0.5	4.0	V
V_I	DC input voltage		–0.5	V_{DD}+0.5	V
V_I–5 V	5 volt tolerant input voltage range		–0.5	5.5	V
V_O	DC output voltage range at any output		–0.5	V_{DD}+0.5	V
	Electrostatic discharge	Human Body Model	—	2	kV
		Machine Model	—	200	V
T_{amb}	Operating free-air temperature range		0	+70	°C
T_{stg}	Storage temperature range		–65	+150	°C

NOTE:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

9.0 RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	Source power node		3.0	3.3	3.6	V
		Non-source power node		2.7 [1]	3.0	3.6	V
V_{IH}	High-level input voltage, LREQ, CTL0, CTL1, D0-D7	$\overline{ISO}$ = V_{DD}, V_{DD} >= 2.7 V		2.3	—	—	V
		$\overline{ISO}$ = V_{DD}, V_{DD} >= 3.0 V		2.6	—	—	V
	High-level input voltage, C/LKON[2], PC0–PC2, $\overline{ISO}$, PD			0.7 V_{DD}	—	—	V
	$\overline{RESET}$			0.6 V_{DD}	—	—	
V_{IL}	Low-level input voltage, LREQ, CTL0, CTL1, D0–D7	$\overline{ISO}$ = V_{DD}		—	—	0.7	V
	Low-level input voltage, C/LKON[2], PC0–PC2, $\overline{ISO}$, PD,			—	—	0.2 V_{DD}	V
	$\overline{RESET}$			—	—	0.3 V_{DD}	—
I_O	Output current	TPBIAS outputs		–6	—	2.5	mA
V_{ID}	Differential input voltage amplitude	TPA, TPB cable inputs, during data reception		118	—	260	mV
		TPA, TPB cable inputs, during data arbitration		168	—	265	mV
V_{IC-100}	TPB common-mode input voltage	Speed signaling off or S100 speed signal	Source power node	1.165	—	2.515	V
			Non-source power node	1.165	—	2.015[1]	V
V_{IC-200}	TPB common-mode input voltage	S200 speed signal	Source power node	0.935	—	2.515	V
			Non-source power node	0.935	—	2.015[1]	V
V_{IC-400}	TPB common-mode input voltage	S400 speed signal	Source power node	0.523	—	2.515	V
			Non-source power node	0.523	—	2.015[1]	V
t_{PU}	Power-up reset time	Set by capacitor between $\overline{RESET}$ pin and GND		2	—	—	ms
	Receive input jitter	TPA, TPB cable inputs, S100 operation		—	—	1.08	ns
		TPA, TPB cable inputs, S200 operation		—	—	0.5	ns
		TPA, TPB cable inputs, S400 operation		—	—	0.315	ns
	Receive input skew	Between TPA and TPB cable inputs, S100 operation		—	—	0.8	ns
		Between TPA and TPB cable inputs, S200 operation		—	—	0.55	ns
		Between TPA and TPB cable inputs, S400 operation		—	—	0.5	ns
f_{XTAL}	Crystal or external clock frequency	Crystal connected according to Figure 10 or external clock input at pin XI		24.5735	24.576	24.5785	MHz

NOTES:
1. For a node that does not source power to the bus (see Section 4.2.2.2 in the IEEE 1394-1995 standard).
2. C/LKON is only an input when $\overline{RESET}$ = 0.

10.0 CABLE DRIVER

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
V_{OD}	Differential output voltage	56 Ω load	172	—	265	mV
$I_{O(diff)}$	Driver Difference current, TPA+, TPA–, TPB+, TPB– [1]	Drivers enabled, speed signaling OFF	–0.88	—	0.88	mA
I_{SP}	Common mode speed signaling output current, TPB+, TPB– [2]	200 Mbps speed signaling enabled	–4.84	—	–2.53	mA
		400 Mbps speed signaling enabled	–12.4	—	–8.10	mA
V_{OFF}	OFF state differential voltage	Drivers disabled	—	—	20	mV

NOTES:
1. Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– algebraic sum of driver currents.
2. Limits defined as one half of the algebraic sum of currents flowing out of TPB+ and TPB–.

11.0 CABLE RECEIVER

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
Z_{ID}	Differential input impedance	Drivers disabled	10	14	—	kΩ
			—	—	4	pF
Z_{IC}	Common mode input impedance	Drivers disabled	20	—	—	kΩ
			—	—	24	pF
V_{TH-R}	Receiver input threshold voltage	Drivers disabled	–30	—	30	mV
V_{TH-CB}	Cable bias detect threshold, TPBn cable inputs	Drivers disabled	0.6	—	1.0	V
V_{TH+}	Positive arbitration comparator input threshold voltage	Drivers disabled	89	—	168	mV
$V_{TH–}$	Negative arbitration comparator input threshold voltage	Drivers disabled	–168	—	–89	mV
$V_{TH–SP200}$	Speed signal input threshold	TPBIAS–TPA common mode voltage, drivers disabled 200 Mbps	49	—	131	mV
$V_{TH–SP400}$	Speed signal input threshold	TPBIAS–TPA common mode voltage, drivers disabled 400 Mbps	314	—	396	mV
I_{CD}	Connect detect output at TPBIAS pins	Drivers disabled	—	—	–76	µA

12.0 OTHER DEVICE I/O

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	See Note 1	—	56	—	mA
		See Note 2	—	40	—	mA
		See Note 3	—	38	—	mA
I_{DD-PD}	Supply current in power down mode	PD = V_{DD} in power down mode	—	150	—	µA
V_{TH}	Cable power status threshold voltage	390 kΩ resistor between cable power and CPS pin: Measured at cable power side of resistor	4.7	—	7.5	V
V_{OH}	High-level output voltage, pins CTL0, CTL1, D0–D7, SYSCLK, CNA	V_{DD} >= 2.7 V, I_{OH} = –4 mA, $\overline{ISO}$ = V_{DD}	2.4	—	—	V
		V_{DD} >= 3.0 V, I_{OH} = –4 mA, $\overline{ISO}$ = V_{DD}	2.8	—	—	V
		Annex J: I_{OH} = –9 mA, $\overline{ISO}$ = 0	V_{DD}–0.4	—	—	V
V_{OL}	Low-level output voltage, pins CTL0, CTL1, D0–D7, CNA, SYSCLK	I_{OL} = 4 mA, $\overline{ISO}$ = V_{DD}	—	—	0.4	V
		Annex J: I_{OL} = 9 mA, $\overline{ISO}$ = 0	—	—	0.4	V
V_{OH}	High-level output voltage, pin C/LKON	V_{DD} = 2.7 V, I_{OH} = –4 mA; See Note 4	2.4	—	—	V
		V_{DD} >= 3.0 V, I_{OH} = –4 mA; See Note 4	2.7	—	—	V
V_{OL}	Low-level output voltage, pin C/LKON	V_{DD} = 2.7 V, I_{OL} = 4 mA; See Note 4	—	—	0.3	V
I_{BH+}	Positive peak bus holder current, pins CTL0, CTL1, D0–D7, LREQ	$\overline{ISO}$ = V_{DD}, V_I = 0 V to V_{DD}	0.05	—	1.0	mA
I_{BH-}	Negative peak bus holder current, pins CTL0, CTL1, D0–D7, LREQ	$\overline{ISO}$ = V_{DD}, V_I = 0 V to V_{DD}	–1.0	—	–0.05	mA
I_I	Input current, pins LREQ, LPS, PD, TEST0, BRIDGE, PC0–PC2	$\overline{ISO}$ = 0 V; V_{DD} = 3.6 V	—	—	5	µA
I_{OZ}	Off-state current, pins CTL0, CTL1, D0–D7, C/LKON	VO = V_{DD} or 0 V	–5	—	5	µA
I_{RST-UP}	Pullup current, $\overline{RESET}$ input	V_I = 1.5 V or 0 V	–90	—	–20	µA
I_{RST-DN}	Pulldown current, $\overline{RESET}$ input	V_I = V_{DD}, PD = V_{DD}	.4	1.6	2.8	mA
V_{IT+}	Positive going threshold voltage, LREQ, CTL0, CTL1, D0–D7, C/LKON inputs	$\overline{ISO}$ = 0 V	V_{DD}/2 + 0.3	—	V_{DD}/2 + 0.9	V
V_{IT-}	Negative going threshold voltage, LREQ, CTL0, CTL1, D0–D7, C/LKON inputs	$\overline{ISO}$ = 0 V	V_{DD}/2 – 0.9	—	V_{DD}/2 – 0.3	V
V_{LIT+}	Positive going threshold voltage, LPS inputs	V_{LREF} = 0.42 x V_{DD}	—	—	V_{LREF}+1	V
V_{LIT-}	Negative going threshold voltage, LPS inputs	V_{LREF} = 0.42 x V_{DD}	V_{LREF}+0.2	—	—	V
V_O	TPBIAS output voltage	At rated I_O current	1.665	—	2.015	V

NOTES:
1. Transmit Max Packet (1 port transmitting max size isochronous packet (4096 bytes), sent on every isochronous interval, S400, data value of 0xCCCCCCCCh), V_{DD} = 3.3 V, T_A = 25 °C
2. Receive typical packet (1 port receiving DV packets on every isochronous interval, S100), V_{DD} = 3.3 V, TA = 25 °C
3. Idle (1 Port transmitting cycle starts) V_{DD} = 3.3 V, T_A = 25 °C
4. The C/LKON pin is able to drive an isolation circuit according to Figure 5A-20 of the IEEE-1394a-2000 standard.

13.0 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
RΘjA	Junction-to-free-air thermal resistance	Board mounted, no air flow	—	68	—	°C/W

14.0 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
	Transmit jitter	TPA, TPB	—	—	0.15	ns
	Transmit skew	Between TPA and TPB	—	—	0.10	ns
t_r	TPA, TPB differential output voltage rise time	10% to 90%; At 1394 connector	0.5	—	1.2	ns
t_f	TPA, TPB differential output voltage fall time	90% to 10%; At 1394 connector	0.5	—	1.2	ns
t_{SU}	Setup time, CTL0, CTL1, D0–D7, LREQ to SYSCLK	50% to 50%; See Figure 2	5	—	—	ns
t_H	Hold time, CTL0, CTL1, D0–D7, LREQ after SYSCLK	50% to 50%; See Figure 2	0	—	—	ns
t_D	Delay time SYSCLK to CTL0, CTL1, D0–D7	50% to 50%; See Figure 3	0.5	—	11	ns
C_L	Capacitance load value CTL0, CTL1, D0–D7, SYSCLK		—	10	—	pF
C_i	Input capacitance CTL0, CTL1, D0–D7, LREQ		—	3.3	—	pF

15.0 TIMING WAVEFORMS

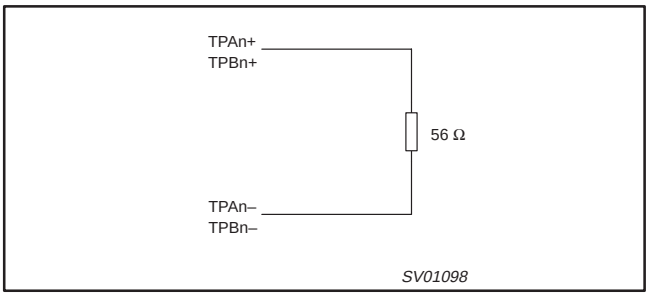


Figure 1. Test load diagram

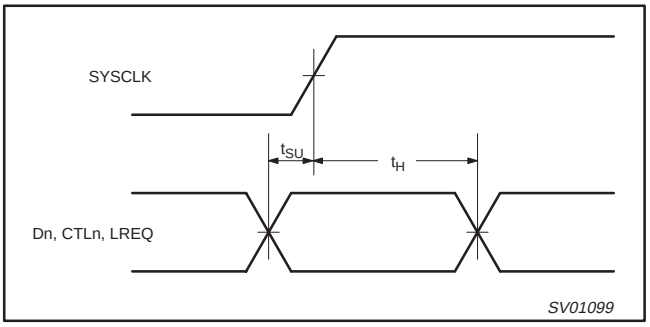


Figure 2. Dn, CTLn, LREQ input setup and hold times

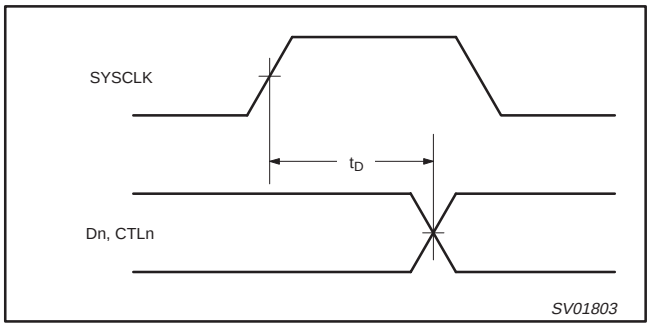


Figure 3. Dn, CTLn, output delay relative to SYSCLK

16.0 INTERNAL REGISTER CONFIGURATION

There are 16 accessible internal registers in the PDI1394P25. The configuration of the registers at addresses 0 through 7 (the base registers) is fixed, while the configuration of the registers at addresses 8h through Fh (the paged registers) is dependent upon which one of eight pages, numbered 0h through 7h, is currently selected. The selected page is set in base register 7h.

The configuration of the base registers is shown in Table 1, and corresponding field descriptions are given in Table 2. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved or Rsvd in the following register configuration tables) is read as 0, but is subject to future usage. All registers in address pages 2 through 6 are reserved.

Table 1. Base Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Rsvd	Num_Ports (0001b)			
0011	PHY_Speed (010b)			Rsvd	Delay (0001b)			
0100	LCtrl	C	Jitter (000)			Pwr_Class		
0101	RPIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Reserved							
0111	Page_Select			Rsvd	Port Select			

Table 2. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	Rd	This field contains the physical address ID of this node determined during self-ID. The physical-ID is invalid after a bus reset until self-ID has completed as indicated by an unsolicited register-0 status transfer.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power-status. This bit indicates the state of the CPS input terminal. The CPS terminal is normally tied to serial bus cable power through a 390 kΩ resistor. A 0 in this bit indicates that the cable power voltage has dropped below its threshold for ensured reliable operation.
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the PHY to attempt to become root after the next bus reset. The RHB bit is reset to 0 by a hardware reset, and is unaffected by a bus reset.
IBR	1	Rd/Wr	Initiate bus reset. This bit instructs the PHY to initiate a long (166 μs) bus reset at the next opportunity. Any receive or transmit operation in progress when this bit is set will complete before the bus reset is initiated. The IBR bit is reset to 0 after a hardware reset or a bus reset.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value is used to set the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count can be set either by a write to the register, or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh by hardware reset or after two consecutive bus resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet).
Extended	3	Rd	Extended register definition. For the PDI1394P25, this field is 111b, indicating that the extended register set is implemented.
Num_Ports	4	Rd	Number of ports. This field indicates the number of ports implemented in the PHY. For the PDI1394P25 this field is 1.
PHY_Speed	3	Rd	PHY speed capability. For the PDI1394P25, this field is 010b, indicating S400 speed capability.
Delay	4	Rd	This field is not applicable for the single-port P25 and should always read as 0001 binary.

FIELD	SIZE	TYPE	DESCRIPTION
LCtrl	1	Rd/Wr	Link-active status control. This bit is used to control the active status of the LLC as indicated during self-ID. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC is considered active only if both the LPS input is active the and LCtrl bit is set. The LCtrl bit provides a software controllable means to indicate the LLC active status in lieu of using the LPS input. The LCtrl bit is set to 1 by hardware reset and is unaffected by bus-reset. NOTE: The state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-LLC interface is operational as determined by the LPS input being active, then received packets and status information will continue to be presented on the interface, and any requests indicated on the LREQ input will be processed, even if the LCtrl bit is cleared to 0.
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the “c” field (bit 20) of the self-ID packet. This bit is set to the state specified by the C/LKON input terminal by a hardware reset and is unaffected by a bus reset.
Jitter	3	Rd	PHY repeater jitter. This field indicates the worst case difference between the fastest and slowest repeater data delay, expressed as (Jitter + 1) × 20 ns. For the PDI1394P25, this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node’s power consumption and source characteristics and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is reset to the state specified by the PC0–PC2 input terminals upon hardware reset, and is unaffected by a bus reset. See Table 21.
RPIE	1	Rd/Wr	Resuming port interrupt enable. This bit, if set to 1, enables the port event interrupt (PEI) bit to be set whenever resume operations begin on the port. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus reset. This bit, if set to 1, instructs the PHY to initiate a short (1.3 µs) arbitrated bus reset at the next opportunity. This bit is reset to 0 by a bus reset. **NOTE:** Legacy IEEE Std 1394–1995 compliant PHYs are not capable of performing short bus resets. Therefore, initiation of a short bus reset in a network that contains such a legacy device results in a long bus reset being performed.
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times-out during tree-ID start, and may indicate that the bus is configured in a loop. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. **NOTE:** If the network is configured in a loop, only those nodes which are part of the loop should generate a configuration time out interrupt. All other nodes should instead time out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus-reset.
CPSI	1	Rd/Wr	Cable-power-status interrupt. This bit is set to 1 whenever the CPS input transitions from high to low indicating that cable power may be too low for reliable operation. This bit is set to 1 by hardware reset, and set to 0 by writing a 1 to this register bit.
STOI	1	Rd/Wr	State time-out interrupt. This bit indicates that a state time-out has occurred. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
PEI	1	Rd/Wr	Port event interrupt. This bit is set to 1 on any change in the connected, bias, disabled, or fault bits for any port for which the port interrupt enable (PIE) bit is set. Additionally, if the resuming port interrupt enable (RPIE) bit is set, the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
EAA	1	Rd/Wr	Enable arbitration acceleration. This bit enables the PHY to perform the various arbitration acceleration enhancements defined in P1394a (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus reset. **NOTE:** The EAA bit should be set only if the attached LLC is P1394a compliant. If the LLC is not P1394a compliant, use of the arbitration acceleration enhancements can interfere with isochronous traffic by excessively delaying the transmission of cycle-start packets.
EMC	1	Rd/Wr	Enable multispeed concatenated packets. This bit enables the PHY to transmit concatenated packets of differing speeds in accordance with the protocols defined in P1394a. This bit is reset to 0 by hardware reset and is unaffected by bus reset. **NOTE:** The use of multispeed concatenation is completely compatible with networks containing legacy IEEE Std 1394–1995 PHYs. However, use of multispeed concatenation requires that the attached LLC be P1394a compliant.
Page_Select	3	Rd/Wr	Page_Select. This field selects the register page to use when accessing register addresses 8 through 15. This field is reset to 0 by a hardware reset and is unaffected by bus-reset.
Port_Select	4	Rd/Wr	Port_Select. This field selects the port when accessing per-port status or control (e.g., when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by hardware reset and is unaffected by bus reset. The only valid number for the PDI1394P25 is 0.

The Port Status page provides access to configuration and status information for each of a Phy's ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. The configuration of the port status page registers is shown in Table 3 and corresponding field descriptions given in Table 4. If the selected port is unimplemented, all registers in the port status page are read as 0. The only valid number for the PDI1394P25 is 0.

Table 3. Page 0 (Port Status) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	AStat		BStat		Ch	Con	Bias	Dis
1001	Peer_Speed			PIE	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

Table 4. Page 0 (Port Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
AStat	2	Rd	TPA line state. This field indicates the TPA line state of the selected port, encoded as follows: **Code** — **Arb Value** 11 — Z 01 — 1 10 — 0 00 — invalid
BStat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the ASTAT field.
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus-reset until tree-ID has completed.
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of 330ms–350ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus reset. **NOTE:** The Con bit indicates that the port is physically connected to a peer PHY, but the port is not necessarily active.
Bias	1	Rd	Debounced incoming cable bias status. A 1 indicates that the selected port is detecting incoming cable bias. The incoming cable bias must be stable for the debounce time of 41.6µs–52µs for the Bias bit to be set to 1.
Dis	1	Rd/Wr	Port disabled control. If 1, the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus reset.
Peer_Speed	3	Rd	Port peer speed. This field indicates the highest speed capability of the peer PHY connected to the selected port, encoded as follows: **Code** — **Peer Speed** 000 — S100 001 — S200 010 — S400 011–111 — invalid The Peer_Speed field is invalid after a bus reset until self-ID has completed. **NOTE:** Peer speed codes higher than 010b (S400) are defined in P1394a. However, the PDI1394P25 is only capable of detecting peer speeds up to S400.
PIE	1	Rd/Wr	Port event interrupt enable. When set to 1, a port event on the selected port will set the port event interrupt (PEI) bit and notify the link. this bit is reset to 0 by a hardware reset, and is unaffected by bus-reset.
Fault	1	Rd/Wr	Fault. This bit indicates that a resume-fault or suspend-fault has occurred on the selected port, and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend-fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus reset.

The Vendor Identification page is used to identify the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. The configuration of the Vendor Identification page is shown in Table 5, and corresponding field descriptions are given in Table 6.

Table 5. Page 1 (Vendor ID) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

Table 6. Page 1 (Vendor ID) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For the PDI1394P25, this field is 01h, indicating compliance with the P1394a specification.
Vendor_ID	24	Rd	Manufacturer's organizationally unique identifier (OUI). For the PDI1394P25, this field is 00_60_37h (Philips Semiconductors) (the MSB is at register address 1010b).
Product_ID	24	Rd	Product identifier. For the PDI1394P25, this field is 41_28_01 (the MSB is at register address 1101b).

The Vendor-Dependent page provides access to the special control features of the PDI1394P25, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page Select field in base register 7. The configuration of the Vendor-Dependent page is shown in Table 7 and corresponding field descriptions given in Table 8.

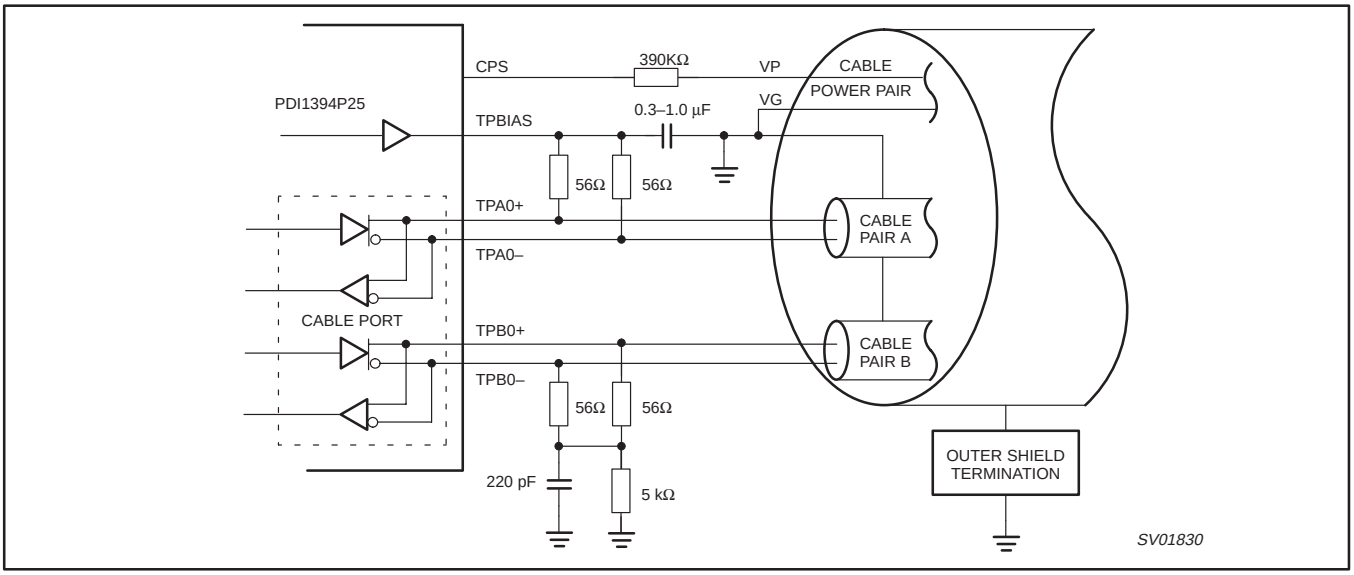
Table 7. Page 7 (Vendor-Dependent) Register Field Descriptions

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Reserved						Link_Speed	
1001	Reserved for test						Bridge_Aware	
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	Reserved for test							
1111	Reserved for test							

Table 8. Page 7 (Vendor-Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Link_Speed	2	Rd/Wr	Link speed. This field indicates the top speed capability of the attached LLC. Encoding is as follows: **Code** **Speed** 00 S100 01 S200 10 S400 11 illegal This field is replicated in the “sp” field of the self-ID packet to indicate the speed capability of the node (PHY and LLC in combination). However, this field does not affect the PHY speed capability indicated to peer PHYs during self-ID; the PDI1394P25 PHY identifies itself as S400 capable to its peers regardless of the value in this field. This field is set to 10b (S400) by hardware reset and is unaffected by bus-reset. An 11b can be written into this field, however, a 10b will be sent in the self-ID packet.
Bridge_Aware	2	Rd/Wr	Bridge_Aware. This field reports Bridge_Aware capability to all nodes via the self-ID packet. Encoding is as follows: **Code** **Meaning** 00 Non-bridge device 01 Reserved (BRAN Bridge) 10 Bridge compliant with 1394.1 (unchanged state) 11 Bridge compliant with 1394.1 (changed state) This field is replicated in bits 18 and 19 of the self-ID packet. The value of this field does not affect PHY operation. It is a reporting mechanism. The default value for this field is set by the BRIDGE pin. The BRIDGE pin is sampled during a hardware reset ($\overline{\text{RESET}}$ low). When the BRIDGE pin is low, this field is set to “00” indicating a “non-bridge device.” When the BRIDGE pin is high, this field is set to “11” indicating a “1394.1 bridge compliant” device. Writing to this field overrides the default setting by the BRIDGE pin.

17.0 APPLICATION INFORMATION



The IEEE Std 1394–1995 calls for a 250 pF capacitor, which is a non-standard component value. A 220 pF capacitor is recommended.

Figure 4. Twisted pair cable interface connections

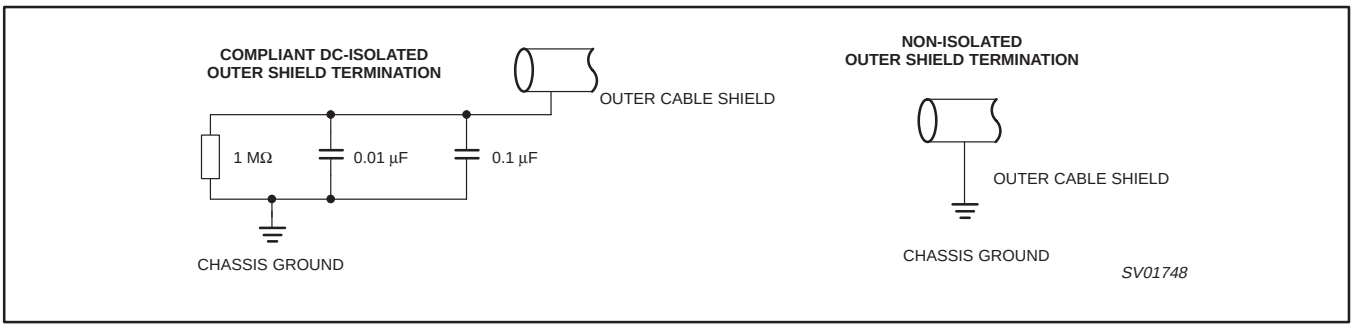
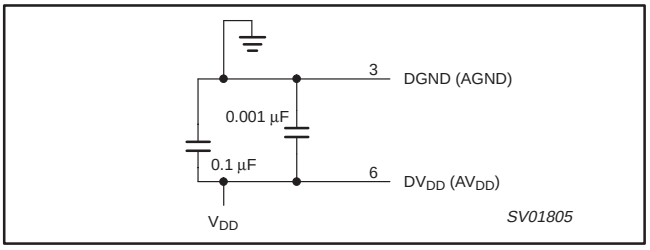


Figure 5. Cable outer shield termination methods



Use one of these networks per side for all digital power and ground pins and one per side for all analog power and ground pins. Place the network as close to the PHY as possible.

Figure 6. Power supply decoupling network

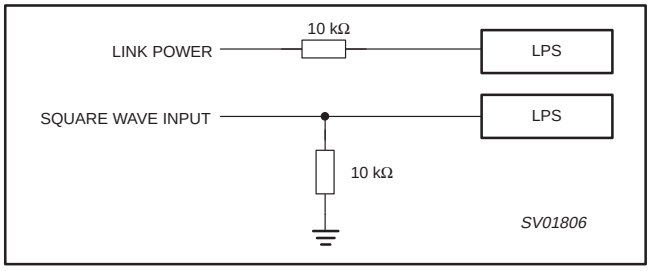


Figure 7. Non-isolated connection variations for LPS

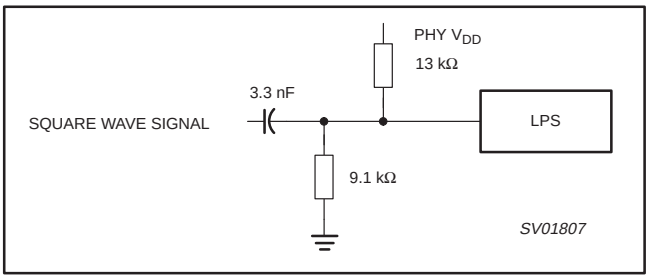


Figure 8. Isolated circuit connection for LPS

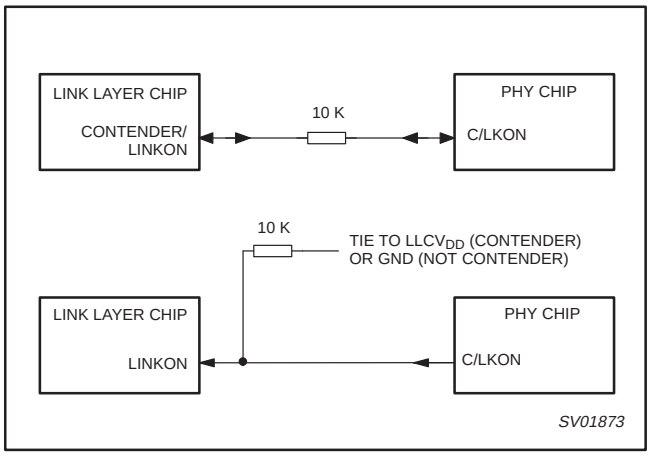
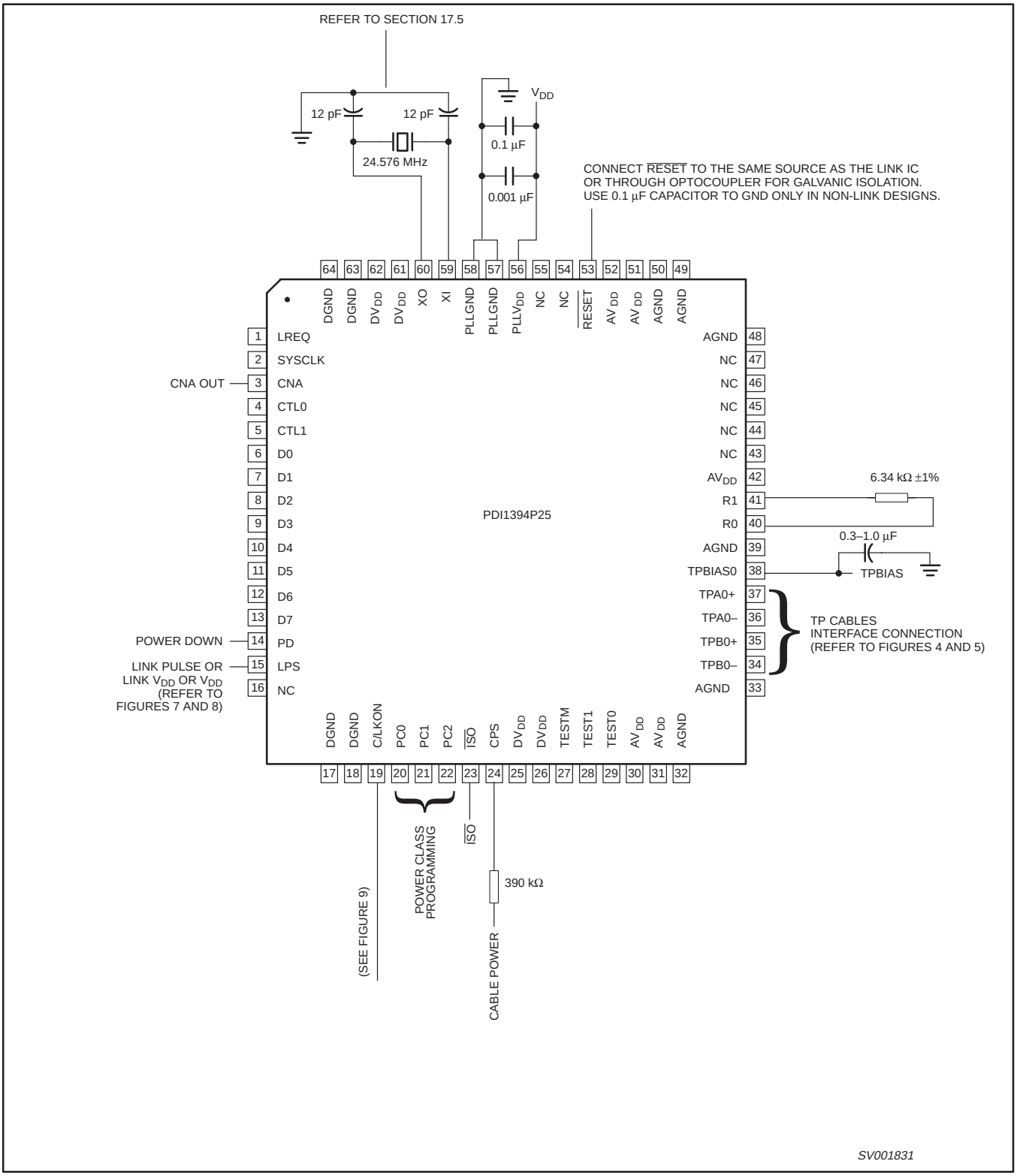


Figure 9. Three configurations for C/LKON signal in a non-isolated system

17.1 External Component Connections



See Figure 6 for recommended power and ground connections.

Figure 10. External Component Connections

17.2 $\overline{\text{RESET}}$ and Power Down

Forcing the $\overline{\text{RESET}}$ pin low resets the internal logic to the Reset Start state and deactivates SYSCLK. Returning the $\overline{\text{RESET}}$ pin high causes a Bus Reset condition on the active cable ports. For power-up (and after Power Down is asserted) $\overline{\text{RESET}}$ must be asserted low for a minimum of 2 ms from the time that the PHY power reaches the minimum required supply voltage. This is required to assure proper PLL operation before the PHY begins using the clock.

The PHY must come out of $\overline{\text{RESET}}$ simultaneously or just after the Link comes out of $\overline{\text{RESET}}$ so that the LLC/PHY handshake occurs properly. To assure that this happens, it is recommended that the same signal source originate LLC and PHY reset signals. If galvanic isolation is used, an optocoupler should be used to drive the $\overline{\text{RESET}}$ pin of the PHY. (See Philips AN2452 “IEEE 1394 bus node galvanic isolation and power supply design”.) If galvanic isolation is not used, the LCC and PHY reset pins should be connected directly together. A single capacitor on the $\overline{\text{RESET}}$ pin of the PHY as described below is recommended only in designs without an LLC device (i.e. repeater designs).

An internal pull-up resistor is connected to V_{DD}, so only an external delay capacitor is required. When using a passive capacitor on the $\overline{\text{RESET}}$ terminal to generate a power-on reset signal, the minimum reset time will be assured if the capacitor has a minimum value of 0.1 μF and also satisfies the following equation:

$$C_{min} = 0.0077 \times T + 0.085$$

where C_{min} is the minimum capacitance on the $\overline{\text{RESET}}$ terminal in μF, and T is the V_{DD} ramp time, 10%–90%, in ms.

An alternative to the passive reset is to actively drive $\overline{\text{RESET}}$ low for the minimum reset time following power on. This input is a standard logic Schmitt buffer and may also be driven by an open drain logic output buffer.

The $\overline{\text{RESET}}$ pin also has an internal n-channel pull-down transistor activated by the Power Down pin. For a reset during normal operation, a 10 μs low pulse on this pin will accomplish a full PHY reset. This pulse, as well as the 2 ms power up reset pulse, could be microprocessor controlled, in which case the external delay capacitor would not be needed. For more details on using single capacitor isolation with this pin, please refer to the Philips Isolation Application Note AN2452

The Power Down input powers down all device functions with the exception of the CNA circuit to conserve power in portable or battery-powered applications. It must be held high for at least 2 ms to assure a successful reset after power down.

17.3 Using the PDI1394P25 with a non-P1394a link layer

The PDI1394P25 implements the PHY-LLC interface specified in the P1394a Supplement. This interface is based upon the interface described in informative Annex J of IEEE Std 1394-1995, which is the interface used in older PHY devices. The PHY-LLC interface specified in P1394a is completely compatible with the older Annex J interface.

The P1394a Supplement includes enhancements to the Annex J interface that must be comprehended when using the PDI1394P25 with a non-P1394a LLC device.

- A new LLC service request was added which allows the LLC to temporarily enable and disable asynchronous arbitration accelerations. If the LLC does not implement this new service request, the arbitration enhancements should not be enabled (see the EAA bit in PHY register 5).
- The capability to perform multispeed concatenation (the concatenation of packets of differing speeds) was added in order to improve bus efficiency (primarily during isochronous transmission). If the LLC does not support multispeed concatenation, multispeed concatenation should not be enabled in the PHY (see the EMC bit in PHY register 5).
- In order to accommodate the higher transmission speeds expected in future revisions of the standard, P1394a extended the speed code in bus requests from 2 bits to 3 bits, increasing the length of the bus request from 7 bits to 8 bits. The new speed codes were carefully selected so that new P1394a PHY and LLC devices would be compatible, for speeds from S100 to S400, with legacy PHY and LLC devices that use the 2-bit speed codes. The PDI1394P25 correctly interprets both 7-bit bus requests (with 2-bit speed code) and 8-bit bus requests (with 3-bit speed codes). Moreover, if a 7-bit bus request is immediately followed by another request (e.g., a register read or write request), the PDI1394P25 correctly interprets both requests. Although the PDI1394P25 correctly interprets 8-bit bus requests, a request with a speed code exceeding S400 results in the PDI1394P25 transmitting a null packet (data-prefix followed by data-end, with no data in the packet).

17.4 Using the PDI1394P25 with a lower-speed link layer

Although the PDI1394P25 is an S400 capable PHY, it may be used with lower speed LLCs. In such a case, the LLC has fewer data terminals than the PHY, and some Dn terminals on the PDI1394P25 will be unused. Unused Dn terminals should be pulled to ground through 10 kΩ resistors.

The PDI1394P25 transfers all received packet data to the LLC, even if the speed of the packet exceeds the capability of the LLC to accept it. Some lower speed LLC designs do not properly ignore packet data in such cases. On the rare occasions that the first 16 bits of partial data accepted by such a LLC match a node’s bus and node ID, spurious header CRC or tcode errors may result.

In discussing this topic, the reader should be aware that the IEEE1394a-2000 standard (paragraph 8.3.2.4.2) made the speed maps defined in IEEE1394-1995 obsolete and defined a new field (*link_spd*) in the Configuration ROM Bus_Info_Block where the maximum speed of the node’s link layer is available. The PDI1394P25 PHY’s default maximum speed is reported in the self-ID packet. The IEEE1394a-2000 standard notes that bus managers that implement the SPEED_MAP registers as specified by IEEE Std 1394-1995 are compliant with the IEEE1394a-2000 standard but users are cautioned that the addresses utilized by these registers may be redefined in future IEEE standards. Without a bus manager-created and maintained speed map, in order to transmit at the highest speed along a path, a transmitting node must determine the *node* speed capability (lesser of link speed or PHY speed) for a target node and each of the PHY speed capabilities along the path between the source and target nodes. That is, each node would have to create a network speed map. Some designers may choose to implement a speed map in bus manager-capable nodes to maximize transmission speed when a slower-than-PHY link chip exists in a node along the transmission path. The following paragraphs are presented for use with products that utilize speed maps.

During bus initialization following a bus-reset, each PHY transmits a self-ID packet that indicates, among other information, the speed capability of the PHY. The bus manager (if one exists) may build a speed-map from the collected self-ID packets. This speed-map gives the highest possible speed that can be used on the node-to-node communication path between every pair of nodes in the network. However, as explained below, the speed reported in the self-ID packet of a PDI1394P25 PHY may be adjusted to account for a slow link chip.

In the case of a node consisting of a higher-speed PHY and a lower-speed LLC, the speed capability of the node (lesser of the PHY and LLC speed) is that of the lower-speed LLC. A sophisticated bus manager can determine the LLC speed capability by reading the configuration ROM Bus_Info_Block, or by sending asynchronous request packets at different speeds to the node and checking for an acknowledge; the speed-map may then be adjusted accordingly. The speed-map should reflect that communication to such a node must be done at the lower speed of the LLC, instead of the higher speed of the PHY. However, speed-map entries for paths that merely pass through the node's PHY, but do not terminate at that node, should not be restricted by the lower speed of the LLC.

To assist in building an accurate speed-map, the PDI1394P25 has the capability of indicating a speed other than S400 in its transmitted self-ID packet. This is controlled by the Link_Speed field in register 8 of the Vendor-Dependent page (page 7). Setting the Link_Speed field affects only the speed indicated in the self-ID packet; it has no effect on the speed signaled to peer (adjacent directly connected) PHYs during self-ID. The PDI1394P25 identifies itself as S400 capable to its peers regardless of the value in the Link_Speed field.

Generally, the Link_Speed field in register 8 of the Vendor-Dependent page should not be changed from its power-on default value of S400 unless it is determined that the speed-map (if one exists) is incorrect for path entries terminating in the local node (i.e. the node has a slower link layer chip). If the speed-map is incorrect, it can be assumed that the bus manager has used only the self-ID packet information to build the speed-map. In this case, the node may update the Link_Speed field in register 8 to reflect the lower speed capability of the LLC and then initiate another bus-reset to cause the speed-map to be rebuilt. Note that in this scenario any speed-map entries for node-to-node communication paths that pass through the local node's PHY will be restricted by the lower speed.

In the case of a leaf node (which has only one active port) the Link_Speed field in register 8 may be set to indicate the speed of the LLC without first checking the speed-map. Changing the Link_Speed field in a leaf node can only affect those paths that terminate at that node, since no other paths can pass through a leaf node. It can have no effect on other paths in the speed-map. For hardware configurations which can only be a leaf node (all ports but one are unimplemented), it is recommended that the Link_Speed field be updated immediately after power-on or hardware reset.

17.5 Crystal selection

The PDI1394P25 is designed to use an external 24.576 MHz crystal connected between the XI and XO terminals to provide the reference for an internal oscillator circuit. This oscillator in turn drives a PLL circuit that generates the various clocks required for transmission and resynchronization of data at the S100 through S400 media data rates.

A variation of less than ±100 ppm from nominal for the media data rates is required by IEEE Std 1394. Adjacent PHYs may therefore have a difference of up to 200 ppm from each other in their internal clocks, and PHYs must be able to compensate for this difference over the maximum packet length. Larger clock variations may cause resynchronization overflows or underflows, resulting in corrupted packet data.

For the PDI1394P25, the SYSCLK output may be used to measure the frequency accuracy and stability of the internal oscillator and PLL from which it is derived. The frequency of the SYSCLK output must be within ±100 ppm of the nominal frequency of 49.152 MHz.

The following are some typical specifications for crystals used with the PDI1394P25 in order to achieve the required frequency accuracy and stability:

- Crystal mode of operation: Fundamental
- Frequency tolerance at 25°C: Total frequency variation for the complete circuit is +100 ppm. A crystal with +30 ppm frequency tolerance is recommended for adequate margin.
- Frequency stability (over temperature and age): A crystal with +30 ppm frequency stability is recommended for adequate margin.

NOTE: The total frequency variation must be kept below ±100 ppm from nominal with some allowance for error introduced by board and device variations. Trade–offs between frequency tolerance and stability may be made as long as the total frequency variation is less than ±100 ppm. For example, the frequency tolerance of the crystal may be specified at 50 ppm and the temperature tolerance may be specified at 30 ppm to give a total of 80 ppm possible variation due to the crystal alone. Crystal aging also contributes to the frequency variation.

- Load capacitance: For parallel resonant mode crystal circuits, the frequency of oscillation is dependent upon the load capacitance specified for the crystal. Total load capacitance (C_L) is a function of not only the discrete load capacitors, but also board layout and circuit. It may be necessary to iteratively select discrete load capacitors until the SYSCLK output is within specification. It is recommended that load capacitors with a maximum of ±5% tolerance be used.

As an example, for a board which uses a crystal specified for 12 pF loading, load capacitors (C9 and C10 in Figure 11) of 16 pF each are appropriate for the layout of that particular board. The load specified for the crystal includes the load capacitors (C9, C10), the loading of the PHY terminals (C_{PHY}), and the loading of the board itself (C_{BD}). The value of C_{PHY} is typically about 1 pF, and C_{BD} is typically 0.8 pF per centimeter of board etch; a typical board can have 3 pF to 6 pF or more. The load capacitors C9 and C10 combine as capacitors in series so that the total load capacitance is:

$C_L = [(C9 * C10) / (C9+C10)] + C_{PHY} + C_{BD}$.

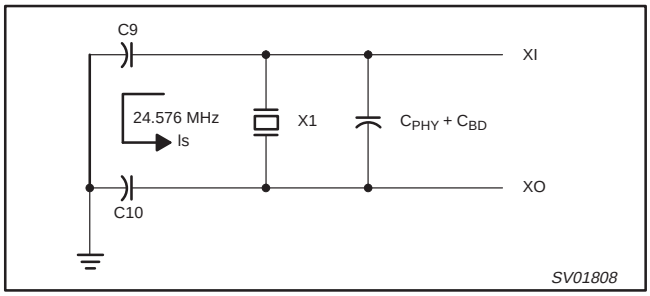


Figure 11. Load Capacitance for the PDI1394P25 PHY

NOTE: The layout of the crystal portion of the PHY circuit is important for obtaining the correct frequency, minimizing noise

introduced into the PHY's Phase Lock Loop, and minimizing any emissions from the circuit. The crystal and two load capacitors should be considered as a unit during layout. The crystal and load capacitors should be placed as close as possible to one another while minimizing the loop area created by the combination of the three components. Varying the size of the capacitors may help in this. Minimizing the loop area minimizes the effect of the resonant current (Is) that flows in this resonant circuit. This layout unit (crystal and load capacitors) should then be placed as close as possible to the PHY XI and XO terminals to minimize trace lengths.

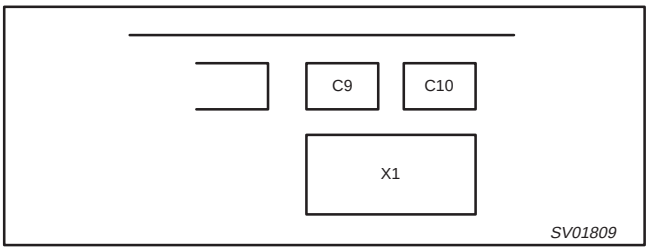


Figure 12. Recommended Crystal and Capacitor Layout

It is strongly recommended that part of the verification process for the design be to measure the frequency of the SYSCLK output of the PHY. This should be done with a frequency counter with an accuracy of 6 digits or better. If the SYSCLK frequency is more than the crystal's tolerance from 49.152 MHz, the load capacitance of the crystal may be varied to improve frequency accuracy. If the frequency is too high add more load capacitance; if the frequency is too low decrease load capacitance. Typically, changes should be done to both load capacitors (C9 and C10 above) at the same time, and both should be of the same value. Additional design details and requirements may be provided by the crystal vendor.

18.0 PRINCIPLES OF OPERATION

The PDI1394P25 is designed to operate with an LLC such as the Philips Semiconductors PDI1394L11 or PDI1394L21. The following paragraphs describe the operation of the PHY-LLC interface.

The interface to the LLC consists of the SYSCLK, CTL0–CTL1, D0–D7, LREQ, LPS, C/LKON, and $\overline{\text{ISO}}$ terminals on the PDI1394P25 as shown in Figure 13.

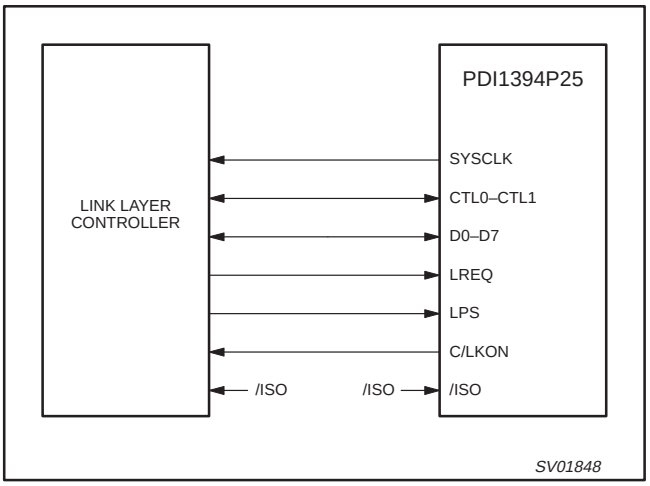


Figure 13. PHY-LLC interface

The SYSCLK terminal provides a 49.152 MHz interface clock. all control and data signals are synchronized to, and sampled on, the rising edge of SYSCLK.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the PDI1394P25 and LLC.

The D0–D7 terminals form a bidirectional data bus, which is used to transfer status information, control information, or packet data between the devices. The PDI1394P25 supports S100, S200, and S400 data transfers over the D0–D7 data bus. In S100 operation only the D0 and D1 terminals are used; in S200 operation only the D0–D3 terminals are used; and in S400 operation all D0–D7 terminals are used for data transfer. When the PDI1394P25 is in control of the D0–D7 bus, unused Dn terminals are driven low during S100 and S200 operations. When the LLC is in control of the D0–D7 bus, unused Dn terminals are ignored by the PDI1394P25.

The LREQ terminal is controlled by the LLC to send serial service requests to the PHY in order to request access to the serial bus for packet transmission, read or write PHY registers, or control arbitration acceleration.

The LPS and C/LKON terminals are used for power management of the PHY and LLC. The LPS terminal indicates the power status of the LLC, and may be used to reset the PHY-LLC interface or to disable SYSCLK. The C/LKON terminal is used to send a wake-up notification to the LLC and to indicate an interrupt to the LLC when either LPS is inactive or the PHY register L bit is zero.

The $\overline{\text{ISO}}$ terminal is used to enable the output differentiation logic on the CTL0–CTL1 and D0–D7 terminals. Output differentiation is required when an isolation barrier of the type described in Annex J of IEEE Std 1394-1995 is implemented between the PHY and LLC.

The PDI1394P25 normally controls the CTL0–CTL1 and D0–D7 bidirectional buses. The LLC is allowed to drive these buses only after the LLC has been granted permission to do so by the PHY.

There are four operations that may occur on the PHY-LLC interface: link service request, status transfer, data transmit, and data receive. The LLC issues a service request to read or write a PHY register, to request the PHY to gain control of the serial bus in order to transmit a packet, or to control arbitration acceleration.

The PHY may initiate a status transfer either autonomously or in response to a register read request from the LLC.

The PHY initiates a receive operation whenever a packet is received from the serial bus.

The PHY initiates a transmit operation after winning control of the serial-bus following a bus request by the LLC. The transmit operation is initiated when the PHY grants control of the interface to the LLC.

The encoding of the CTL0–CTL1 bus is shown in Table 9 and Table 10.

Table 9. CTL encoding when PHY has control of the bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	No activity (this is the default mode)
0	1	Status	Status information is being sent from the PHY to the LLC
1	0	Receive	An incoming packet is being sent from the PHY to the LLC
1	1	Grant	The LLC has been given control of the bus to send an outgoing packet

Table 10. CTL encoding when LLC has control of the bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed)
0	1	Hold	The LLC is holding the bus while data is being prepared for transmission, or indicating that another packet is to be transmitted (concatenated) without arbitrating
1	0	Transmit	An outgoing packet is being sent from the LLC to the PHY
1	1	Reserved	None

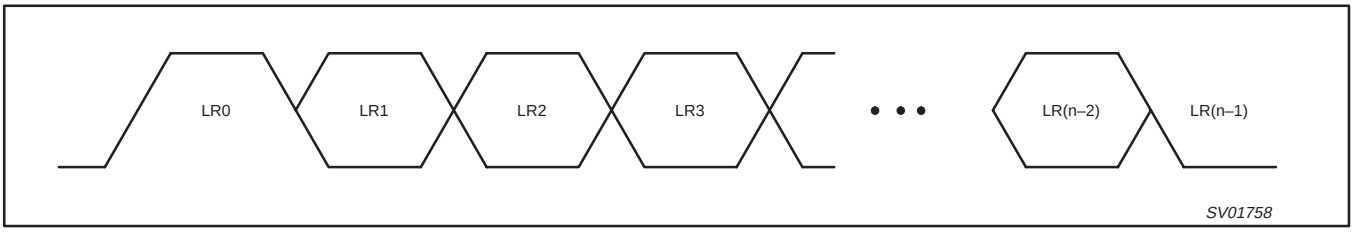


Figure 14. LREQ Request Stream

18.1 LLC service request

To request access to the bus, to read or write a PHY register, or to control arbitration acceleration, the LLC sends a serial bit stream on the LREQ terminal as shown in Figure 14.

The length of the stream will vary depending on the type of request as shown in Table 11.

Table 11. Request Stream Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request	7 or 8
Read register request	9
Write register request	17
Acceleration control request	6

Regardless of the type of request, a start bit of 1 is required at the beginning of the stream, and a stop bit of 0 is required at the end of the stream. The second through fourth bits of the request stream indicate the type of the request. In the descriptions below, bit 0 is the most significant, and is transmitted first in the request bit stream. The LREQ terminal is normally low.

Encoding for the request type is shown in Table 12.

Table 12. Request Type Encoding

LR1–LR3	NAME	DESCRIPTION
000	ImmReq	Immediate bus request. Upon detection of idle, the PHY takes control of the bus immediately without arbitration
001	IsoReq	Isochronous bus request. Upon detection of idle, the PHY arbitrates for the bus without waiting for a subaction gap.
010	PriReq	Priority bus request. The PHY arbitrates for the bus after a subaction gap, ignores the fair protocol.
011	FairReq	Fair bus request. The PHY arbitrates for the bus after a subaction gap, follows the fair protocol
100	RdReg	The PHY returns the specified register contents through a status transfer.
101	WrReg	Write to the specified register.
110	AccelCtl	Enable or disable asynchronous arbitration acceleration.
111	Reserved	Reserved.

For a bus request the length of the LREQ bit stream is 7 or 8 bits, as shown in Table 13.

Table 13. Bus Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	Indicates the type of bus request. See Table 12.
4–6	Request Speed	Indicates the speed at which the PHY will send the data for this request. See Table 14 for the encoding of this field.
7	Stop Bit	Indicates the end of the transfer (always 0). If bit 6 is 0, this bit may be omitted.

The 3-bit request speed field used in bus requests is shown in Table 14.

Table 14. Bus Request Speed Encoding

LR4–LR6	DATA RATE
000	S100
010	S200
100	S400
All others	Invalid

NOTE:
The PDI1394P25 will accept a bus request with an invalid speed code and process the bus request normally. However, during packet transmission for such a request, the PDI1394P25 will ignore any data presented by the LLC and will transmit a null packet.

For a read register request, the length of the LREQ bit stream is 9 bits as shown in Table 15.

Table 15. Read Register Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	A 100 indicating this is a read register request.
4–7	Address	Identifies the address of the PHY register to be read.
8	Stop Bit	Indicates the end of the transfer (always 0).

For a write register request, the length of the LREQ bit stream is 17 bits as shown in Table 16.

Table 16. Write Register Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	A 101 indicating that this is a write register request.
4–7	Address	Identifies the address of the PHY register to be written to.
8–15	Data	Gives the data that is to be written to the specified register address.
16	Stop Bit	Indicates the end of the transfer (always 0).

For an acceleration control request, the length of the LREQ data stream is 6 bits as shown in Table 17.

Table 17. Acceleration Control Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	A 110 indicating this is an acceleration control request.
4	Control	Asynchronous period arbitration acceleration is enabled if 1, and disabled if 0.
5	Stop Bit	Indicates the end of the transfer (always 0).

For fair or priority access, the LLC sends the bus request (FairReq or PriReq) at least one clock after the PHY-LLC interface becomes idle. If the CTL terminals are asserted to the receive state (10b) by the PHY, then any pending fair or priority request is lost (cleared). Additionally, the PHY ignores any fair or priority requests if the Receive state is asserted while the LLC is sending the request. The LLC may then reissue the request one clock after the next interface idle.

The cycle master node uses priority bus request (PriReq) to send a cycle start packet. After receiving or transmitting a cycle start packet, the LLC can issue an isochronous bus request (IsoReq). The PHY will clear an isochronous request only when the bus has been won.

To send an acknowledge packet, the link must issue an immediate bus request (ImmReq) during the reception of the packet addressed to it. This is required in order to minimize the idle gap between the end of the received packet and the start of the transmitted acknowledge packet. As soon as the receive packet ends, the PHY immediately grants control of the bus to the LLC. The LLC sends an acknowledgment to the sender unless the header CRC of the received packet is corrupted. In this case, the LLC does not transmit an acknowledge, but instead cancels the transmit operation and releases the interface immediately; the LLC must not use this grant to send another type of packet. After the interface is released, the LLC may proceed with another request.

The LLC may request only one bus request at a time. Once the LLC issues any request for bus access (ImmReq, IsoReq, FairReq, or PriReq), it cannot issue another request until the PHY indicates that the bus request was “lost” (bus arbitration lost and another packet received), or “won” (bus arbitration won and the LLC granted control). The PHY ignores new bus requests while a previous bus request is pending. All bus requests are cleared upon a bus reset.

For write register requests, the PHY loads the specified data into the addressed register as soon as the request transfer is complete. For read register requests, the PHY returns the contents of the addressed register to the LLC at the next opportunity through a status transfer. If a received packet interrupts the status transfer, then the PHY continues to attempt the transfer of the requested register until it is successful. A write or read register request may be made at any time, including while a bus request is pending. Once a read register request is made, the PHY ignores further read register requests until the register contents are successfully transferred to the LLC. A bus reset does not clear a pending read register request.

The PDI1394P25 includes several arbitration acceleration enhancements which allow the PHY to improve bus performance and throughput by reducing the number and length of inter-packet gaps. These enhancements include autonomous (fly-by) isochronous packet concatenation, autonomous fair and priority packet concatenation onto acknowledge packets, and accelerated fair and priority request arbitration following acknowledge packets. Then enhancements are enabled when the EAA bit in PHY register 5 is set.

The arbitration acceleration enhancements may interfere with the ability of the cycle master node to transmit the cycle start packet under certain circumstances. The acceleration control request is therefore provided to allow the LLC to temporarily enable or disable the arbitration acceleration enhancements of the PDI1394P25 during the asynchronous period. The LLC typically disables the enhancements when its internal cycle counter rolls over indicating that a cycle start packet is imminent, and then re-enables the enhancements when it receives a cycle start packet. The acceleration control request may be made at any time, however, and is immediately serviced by the PHY. Additionally, a bus reset or isochronous bus request will cause the enhancements to be re-enabled, if the EAA bit is set.

18.2 Status transfer

A status transfer is initiated by the PHY when there is status information to be transferred to the LLC. The PHY waits until the interface is idle before starting the transfer. The transfer is initiated by the PHY asserting Status (01b) on the CTL terminals, along with the first two bits of status information on the D[0:1] terminals. The PHY maintains CTL = Status for the duration of the status transfer. The PHY may prematurely end a status transfer by asserting something other than Status on the CTL terminals. This occurs if a packet is received before the status transfer completes. The PHY continues to attempt to complete the transfer until all status information has been successfully transmitted. There is at least one idle cycle between consecutive status transfers.

The PHY normally sends just the first four bits of status to the LLC. These bits are status flags that are needed by the LLC state machines. The PHY sends an entire 16-bit status packet to the LLC after a read register request, or when the PHY has pertinent information to send to the LLC or transaction layers. The only defined condition where the PHY automatically sends a register to the LLC is after self-ID, where the PHY sends the physical-ID register that contains the new node address. All status transfers are either 4 or 16 bits unless interrupted by a received packet. The status flags are considered to have been successfully transmitted to the LLC immediately upon being sent, even if a received packet subsequently interrupts the status transfer. Register contents are considered to have been successfully transmitted only when all 8 bits of the register have been sent. A status transfer is retried after being interrupted only if any status flags remain to be sent, or if a register transfer has not yet completed.

The definition of the bits in the status transfer is shown in Table 18, and the timing is shown in Figure 15.

The sequence of events for a status transfer is as follows:

- Status transfer initiated. the PHY indicates a status transfer by asserting status on the CTL lines along with the status data on the D0 and D1 lines (only 2 bits of status are transferred per cycle). Normally (unless interrupted by a receive operation), a status transfer will be either 2 or 8 cycles long. A 2-cycle (4 bit) transfer occurs when only status information is to be sent. An 8-cycle (16 bit) transfer occurs when register data is to be sent in addition to any status information.
- Status transfer terminated. The PHY normally terminates a status transfer by asserting idle on the CTL lines. If a bus reset is pending, the PHY may also assert Grant on the CTL line immediately following a complete status transfer.

Table 18. Status Bits

BIT(S)	NAME	DESCRIPTION
0	Arbitration Reset Gap	Indicates that the PHY has detected that the bus has been idle for an arbitration reset gap time (as defined in the IEEE 1394–1995 standard). This bit is used by the LLC in the busy/retry state machine.
1	Subaction gap	Indicates that the PHY has detected that the bus has been idle for a subaction gap time (as defined in the IEEE 1394–1995 standard). This bit is used by the LLC to detect the completion of an isochronous cycle.
2	Bus reset	Indicates that the PHY has entered the bus reset state.
3	Interrupt	Indicates that a PHY interrupt event has occurred. An interrupt event may be a configuration time-out, a cable-power voltage falling too low, a state time-out, or a port status change.
4–7	Address	This field holds the address of the PHY register whose contents are being transferred to the LLC.
8–15	Data	This field holds the register contents.

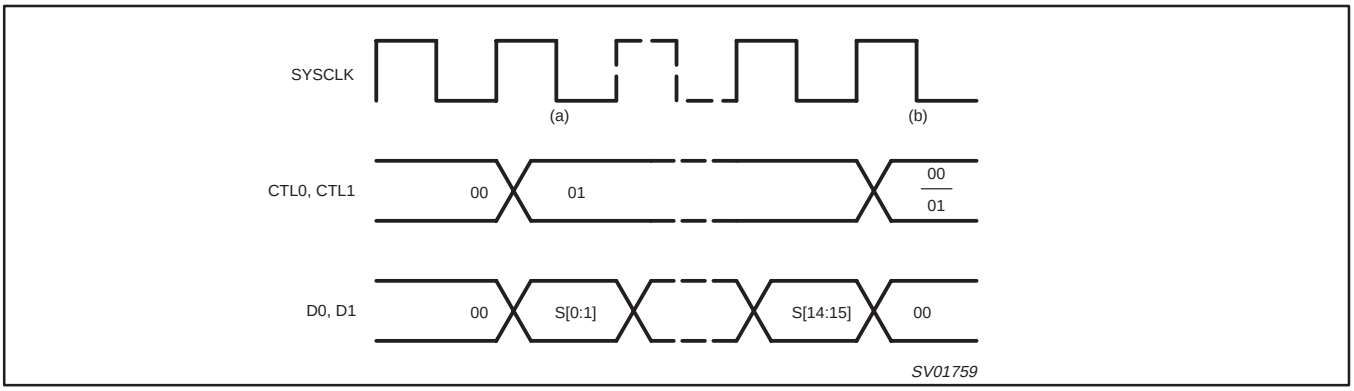


Figure 15. Status Transfer Timing

18.3 Receive

Whenever the PHY detects the data-prefix state on the serial bus, it initiates a receive operation by asserting Receive on the CTL terminals and a logic 1 on each of the D terminals (“data-on” indication). The PHY indicates the start of a packet by placing the speed code (encoded as shown in Table 19) on the D terminals, followed by packet data. The PHY holds the CTL terminals in the Receive state until the last symbol of the packet has been transferred. The PHY indicates the end of packet data by asserting Idle on the CTL terminals. All received packets are transferred to the LLC. Note that the speed code is part of the PHY-LLC protocol and is not included in the calculation of CRC or any other data protection mechanisms.

Table 19. Speed Code for the Receiver

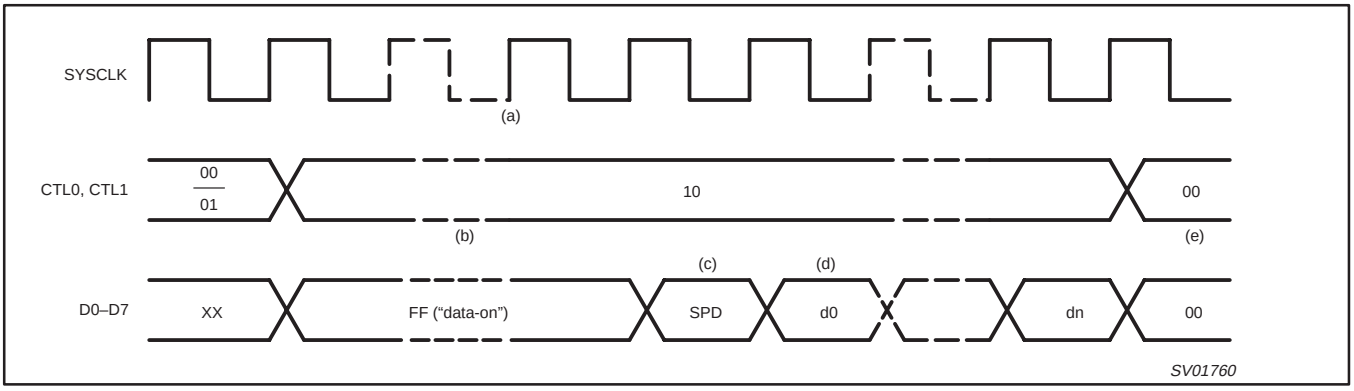
D0–D7	DATA RATE
0000 0000	S100
0100 0000	S200
0101 0000	S400
1111 1111	“data-on” indication

It is possible for the PHY to receive a null packet, which consists of the data-prefix state on the serial bus followed by the data-end state, without any packet data. A null packet is transmitted whenever the packet speed exceeds the capability of the receiving PHY, or whenever the LLC immediately releases the bus without transmitting any data. In this case, the PHY will assert Receive on the CTL terminals with the “data-on” indication (all 1’s) on the D terminals, followed by Idle on the CTL terminals, without any speed code or data being transferred. In all cases, in normal operation, the PDI1394P25 sends at least one “data-on” indication before sending the speed code or terminating the receive operation.

The PDI1394P25 also transfers its own self-ID packet, transmitted during the self-ID phase of bus initialization to the LLC. This packet is transferred to the LLC just as any other received self-ID packet.

The sequence of events for a normal packet reception is as follows:

- Receive operation initiated. The PHY indicates a receive operation by asserting Receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation may interrupt a status transfer operation that is in progress so that the CTL lines may change from status to receive without an intervening idle.
- Data-on indication. The PHY may assert the data-on indication code on the D lines for one or more cycles preceding the speed code.
- Speed code. the PHY indicates the speed of the received packet by asserting a speed code on the D lines for one cycle immediately preceding packet data. The link decodes the speed code on the first Receive cycle for which the D lines are not the data-on code. If the speed code is invalid, or indicates a speed higher than that which the link is capable of handling, the link should ignore the subsequent data.
- Receive data. Following the data-on indication (if any) and the speed code, the PHY asserts packet data on the D lines with receive on the CTL lines for the remainder of the receive operation.
- Receive operation terminated. The PHY terminates the receive operation by asserting the idle on the CTL lines. The PHY asserts at least one cycle of idle following a receive operation.



NOTE: SPD = Speed code; see Table 19; d0–dn = Packet data.

Figure 16. Normal Packet Reception Timing

The sequence of events for a null packet reception is as follows:

- Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation may interrupt a status transfer operation that is in progress so that the CTL lines may change from status to receive without an intervening idle.
- Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles.
- Receive operation terminated. The PHY terminates the receive operation by asserting Idle on the CTL lines. The PHY shall assert at least one cycle of Idle following a receive operation.

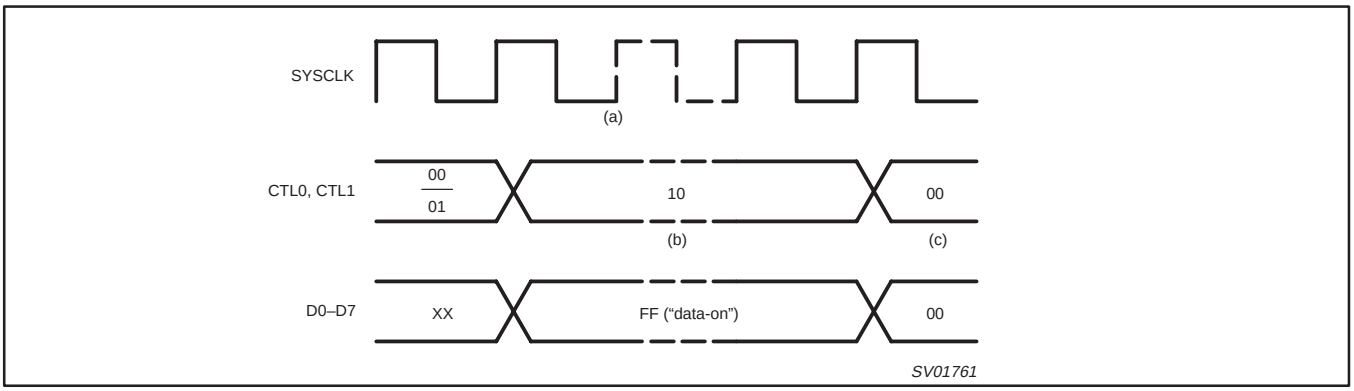


Figure 17. Null Packet Reception Timing

18.4 Transmit

When the LLC issues a bus request through the LREQ terminal, the PHY arbitrates to gain control of the bus. If the PHY wins arbitration for the serial bus, the PHY-LLC interface bus is granted to the link by asserting the Grant state (11b) on the CTL terminals for one SYSCLK cycle, followed by Idle for one clock cycle. The LLC then takes control of the bus by asserting either Idle (00b), Hold (01b), or Transmit (10b) on the CTL terminals. Unless the LLC is immediately releasing the interface, the link may assert the Idle state for at most one clock before it must assert either Hold or Transmit on the CTL terminals. The Hold state is used by the LLC to retain control of the bus while it prepares data for transmission. The LLC may assert Hold for zero or more clock cycles (i.e., the LLC need not assert Hold before Transmit). The PHY asserts data-prefix on the serial bus during this time.

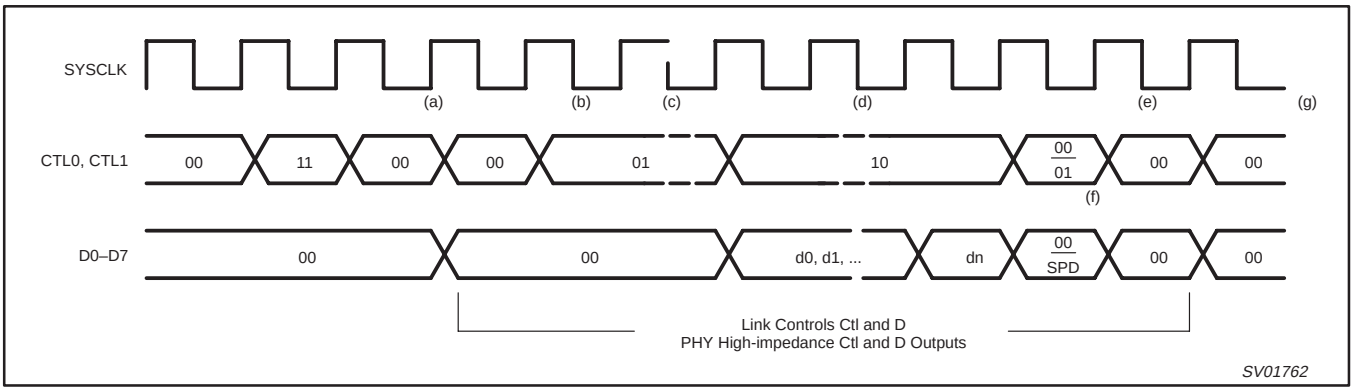
When the LLC is ready to send data, the LLC asserts Transmit on the CTL terminals as well as sending the first bits of packet data on the D lines. The Transmit state is held on the CTL terminals until the last bits of data have been sent. The LLC then asserts either Hold or Idle on the CTL terminals for one clock cycle and then asserts Idle for one additional cycle before releasing the interface bus and putting the CTL and D terminals in a high-impedance state. The PHY then regains control of the interface bus.

The Hold state asserted at the end of packet transmission indicates to the PHY that the LLC requests to send another packet (concatenated packet) without releasing the serial bus. The PHY responds to this concatenation request by waiting the required minimum packet separation time and then asserting Grant as before. This function may be used to send a unified response after sending an acknowledge, or to send consecutive isochronous packets during a single isochronous period. Unless multi-speed concatenation is enabled, all packets transmitted during a single bus ownership must be of the same speed (since the speed of the packet is set before the first packet). If multi-speed concatenation is enabled (when the EMSC bit of PHY register 5 is set), the LLC must specify the speed code of the next concatenated packet on the D terminals when it asserts Hold on the CTL terminals at the end of a packet. The encoding for this speed code is the same as the speed code that precedes received packet data as given in Table 19.

After sending the last packet for the current bus ownership, the LLC releases the bus by asserting Idle on the CTL terminals for two clock cycles. The PHY begins asserting Idle on the CTL terminals one clock after sampling Idle from the link. Note that whenever the D and CTL terminals change direction between the PHY and the LLC, there is an extra clock period allowed so that both sides of the interface can operate on registered versions of the interface signals.

The sequence of events for a normal packet transmission is as follows:

- Transmit operation initiated. The PHY asserts grant on the CTL lines followed by Idle to hand over control of the interface to the link so that the link may transmit a packet. The PHY releases control of the interface (i.e., it 3-States the CTL and D outputs) following the idle cycle.
- Optional idle cycle. The link may assert at most one idle cycle preceding assertion of either hold or transmit. This idle cycle is optional; the link is not required to assert Idle preceding either hold or transmit.
- Optional hold cycles. The link may assert hold for up to 47 cycles preceding assertion of transmit. These hold cycle(s) are optional; the link is not required to assert hold preceding transmit.
- Transmit data. When data is ready to be transmitted, the link asserts transmit on the CTL lines along with the data on the D lines.
- Transmit operation terminated. The transmit operation is terminated by the link asserting hold or idle on the CTL lines the link asserts hold to indicate that the PHY is to retain control of the serial bus in order to transmit a concatenated packet. the link asserts idle to indicate that packet transmission is complete and the PHY may release the serial bus. The link then asserts Idle for one more cycle following this cycle of hold or idle before releasing the interface and returning control the the PHY.
- Concatenated packet speed-code. If multi-speed concatenation is enabled in the PHY, the link shall assert a speed-code on the D lines when it asserts Hold to terminate packet transmission. This speed-code indicates the transmission speed for the concatenated packet that is to follow. The encoding for this concatenated packet speed-code is the same as the encoding for the received packet speed-code (see Table 19). the link may not concatenate an S100 packet onto any higher speed packet.
- After regaining control of the interface, the PHY shall assert at least one cycle of idle before any subsequent status transfer, receive operation, or transmit operation.



NOTE: SPD = Speed code; see Table 19; d0–dn = Packet data.

Figure 18. Normal Packet Transmission Timing

The sequence of events for a cancelled/null packet transmission is as follows:

- Transmit operation initiated. PHY asserts grant on the CTL lines followed by idle to hand over control of the interface to the link.
- Optional Idle cycle. The link may assert at most one idle cycle preceding assertion of hold. This idle cycle is optional; the link is not required to assert idle preceding Hold.
- Optional Hold cycles. The link may assert Hold for up to 47 cycles preceding assertion of idle. These hold cycle(s) are optional; the link is not required to assert hold preceding Idle.
- Null transmit termination. The null transmit operation is terminated by the link asserting two cycles of idle on the CTL lines and then releasing the interface and returning control to the PHY. Note that the link may assert Idle for a total of 3 consecutive cycles if it asserts the optional first idle cycle but does not assert hold. It is recommended that the link assert 3 cycles of Idle to cancel a packet transmission if no hold cycles are asserted. This ensures that either the link or PHY controls the interface in all cycles.
- After regaining control of the interface, the PHY shall assert at least one cycle of Idle before any subsequent status transfer, receive operation, or transmit operation.

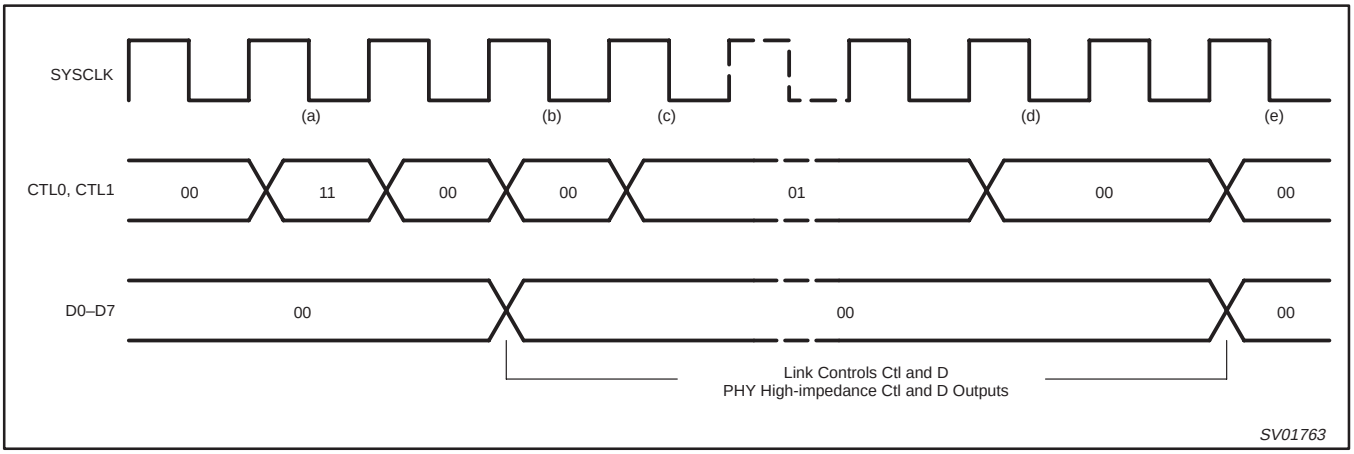


Figure 19. Cancelled/Null Packet Transmission

18.5 Interface reset and disable

The LLC controls the state of the PHY-LLC interface using the LPS signal. The interface may be placed into a reset state, a disabled state, or be made to initialize and then return to normal operation. When the interface is not operational (whether reset, disabled, or in the process of initialization) the PHY cancels any outstanding bus request or register read request, and ignores any requests made via the LREQ line. Additionally, any status information generated by the PHY will not be queued and will not cause a status transfer upon restoration of the interface to normal operation.

The LPS signal may be either a level signal or a pulsed signal, depending upon whether the PHY–LLC interface is a direct connection or is made across an isolation barrier. When an isolation barrier exists between the PHY and LLC (whether of the Philips bus-holder type or Annex J type) the LPS signal must be pulsed. In a direct connection, the LPS signal may be either a pulsed or a level signal. Timing parameters for the LPS signal are given in Table 20.

Table 20. LPS Timing Parameters

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_{LPSL}	LPS low time (when pulsed) (see Note 1)	0.09	2.60	µS
T_{LPSH}	LPS high time (when pulsed) (see Note 1)	0.021	2.60	µS
	LPS duty cycle (when pulsed) (see Note 2)	20	55	%
T_{LPS_RESET}	Time for PHY to recognize LPS deasserted and reset the interface	2.60	2.68	µS
$T_{LPS\_DISABLE}$	Time for PHY to recognize LPS deasserted and disable the interface	26.03	26.11	µS
$T_{RESTORE}$	Time to permit optional isolation circuits to restore during an interface reset	15	23[3]	µS
$T_{CLK\_ACTIVATE}$	Time for SYSCLK to be activated from reassertion of LPS	—	60	nS

NOTES:
1. The specified T_{LPSL} and T_{LPSH} times are worst–case values appropriate for operation with the PDI1394P25. These values are broader than those specified for the same parameters in the P1394a Supplement (i.e., an implementation of LPS that meets the requirements of P1394a will operate correctly with the PDI1394P25).
2. A pulsed LPS signal must have a duty cycle (ratio of T_{LPSH} to cycle period) in the specified range to ensure proper operation when using an isolation barrier on the LPS signal (e.g., as shown in Figure 8)
3. The maximum value for $T_{RESTORE}$ does not apply when the PHY–LLC interface is disabled, in which case an indefinite time may elapse before LPS is reasserted. Otherwise, in order to reset but not disable the interface it is necessary that the LLC ensure that LPS is deasserted for less than $T_{LPS\_DISABLE}$.

The LLC requests that the interface be reset by deasserting the LPS signal and terminating all bus and request activity. When the PHY observes that LPS has been deasserted for T_{LPS_RESET}, it resets the interface. When the interface is in the reset state, the PHY sets its CTL and D outputs in the logic 0 state and ignores any activity on the LREQ signal. The timing for interface reset is shown in Figure 20 and Figure 21.

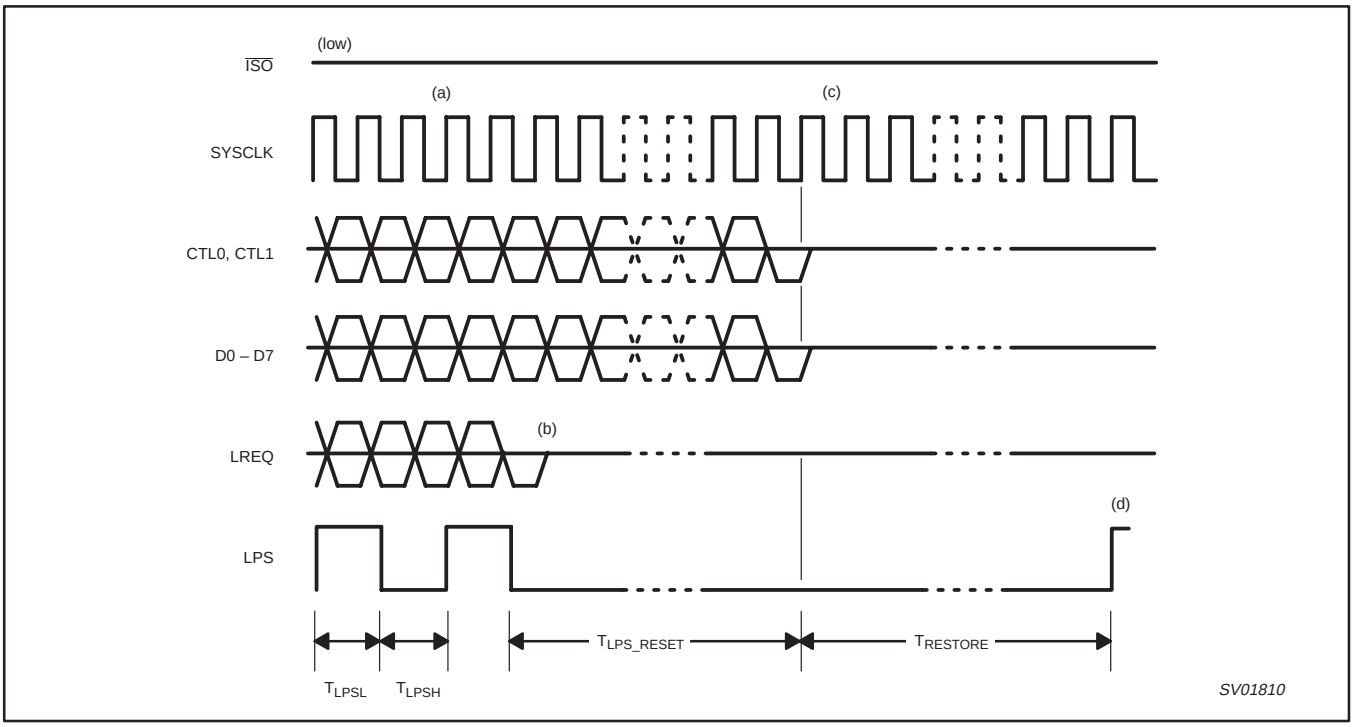


Figure 20. Interface Reset, $\overline{ISO}$ Low

The sequence of events for resetting the PHY-LLC interface when it is in the differentiated mode of operation ($\overline{ISO}$ terminal is low) is as follows:

1. Normal operation. Interface is operating normally, with LPS active, SYSCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line.
2. LPS deasserted. The LLC deasserts the LPS signal and, within 1.0 ms, terminates any request or interface bus activity, and places its LREQ, CTL, and D outputs into a high-impedance state (the LLC should terminate any output signal activity such that signals end in a logic 0 state).
3. Interface reset. After T_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and places its CTL and D outputs into a high-impedance state (the PHY will terminate any output signal activity such that signals end in a logic 0 state). The PHY-LLC interface is now in the reset state.
4. Interface restored. After the minimum $T_{RESTORE}$ time, the LLC may again assert LPS active. (The minimum $T_{RESTORE}$ interval provides sufficient time for the biasing networks used in Annex J type isolation barrier circuits to stabilize and reach a quiescent state if the isolation barrier has somehow become unbalanced.) When LPS is asserted, the interface will be initialized as described on the next page.

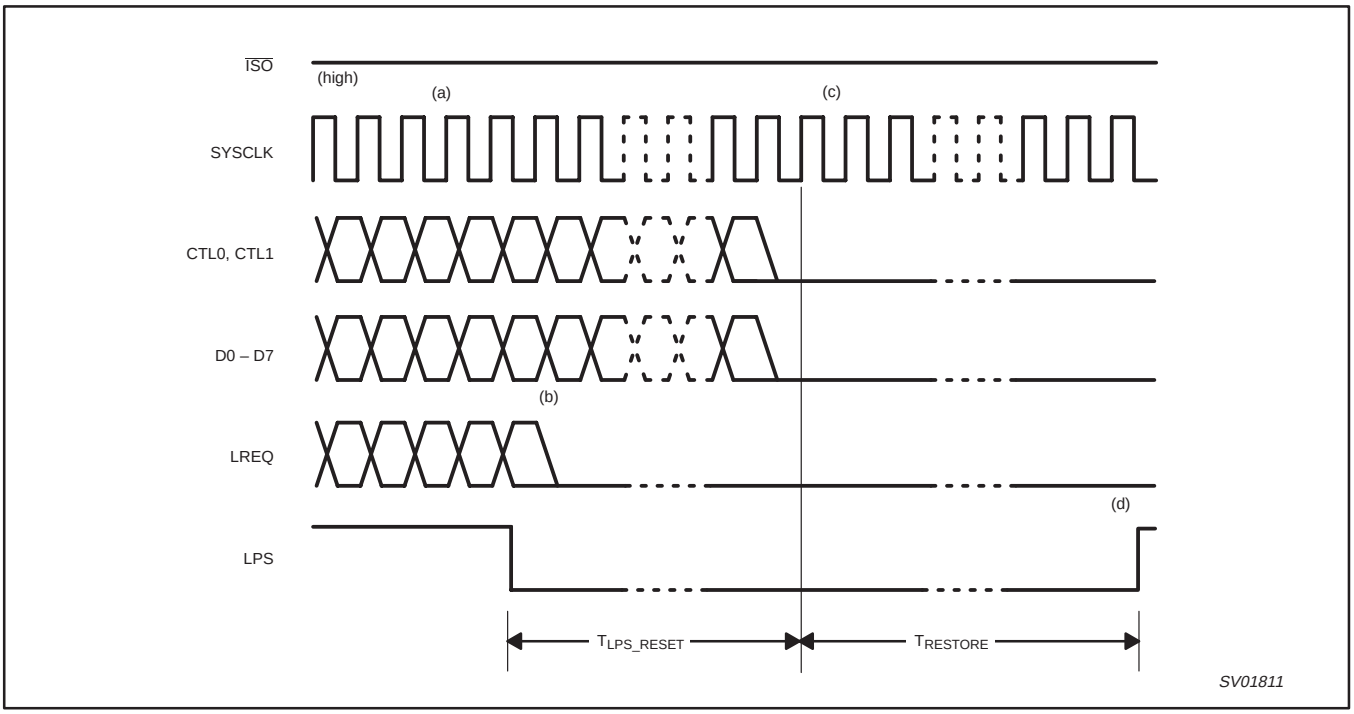


Figure 21. Interface Reset, $\overline{ISO}$ High

The sequence of events for resetting the PHY-LLC interface when it is in the nondifferentiated mode of operation ($\overline{ISO}$ terminal is high) is as follows:

1. Normal operation. Interface is operating normally, with LPS asserted, SYSCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line. In the above diagram, the LPS signal is shown as a non-pulsed level signal. However, it is permissible to use a pulsed signal for LPS in a direct connection between the PHY and LLC; a pulsed signal is required when using an isolation barrier (whether of the Philips Bus Holder type or Annex J type).
2. LPS deasserted. The LLC deasserts the LPS signal and, within 1.0 ms, terminates any request or interface bus activity, places its CTL and D outputs into a high-impedance state, and drives its LREQ output low.
3. Interface reset. After T_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and drives its CTL and D outputs low. The PHY-LLC interface is now in the reset state.
4. Interface restored. After the minimum $T_{RESTORE}$ time, the LLC may again assert LPS active. (The minimum $T_{RESTORE}$ interval provides sufficient time for the biasing networks used in Annex J type isolation barrier circuits to stabilize and reach a quiescent state if the isolation barrier has somehow become unbalanced.) When LPS is asserted, the interface will be initialized as described below.

If the LLC continues to keep the LPS signal deasserted, it requests that the interface be disabled. The PHY disables the interface when it observes that LPS has been deasserted for $T_{LPS\_DISABLE}$. When the interface is disabled, the PHY sets its CTL and D outputs as stated above for interface reset, but also stops SYSCLK activity. The interface is also placed into the disabled condition upon a hardware reset of the PHY. The timing for interface disable is shown in Figure 22 and Figure 23.

When the interface is disabled, the PHY will enter a low-power state if none of its ports is active.

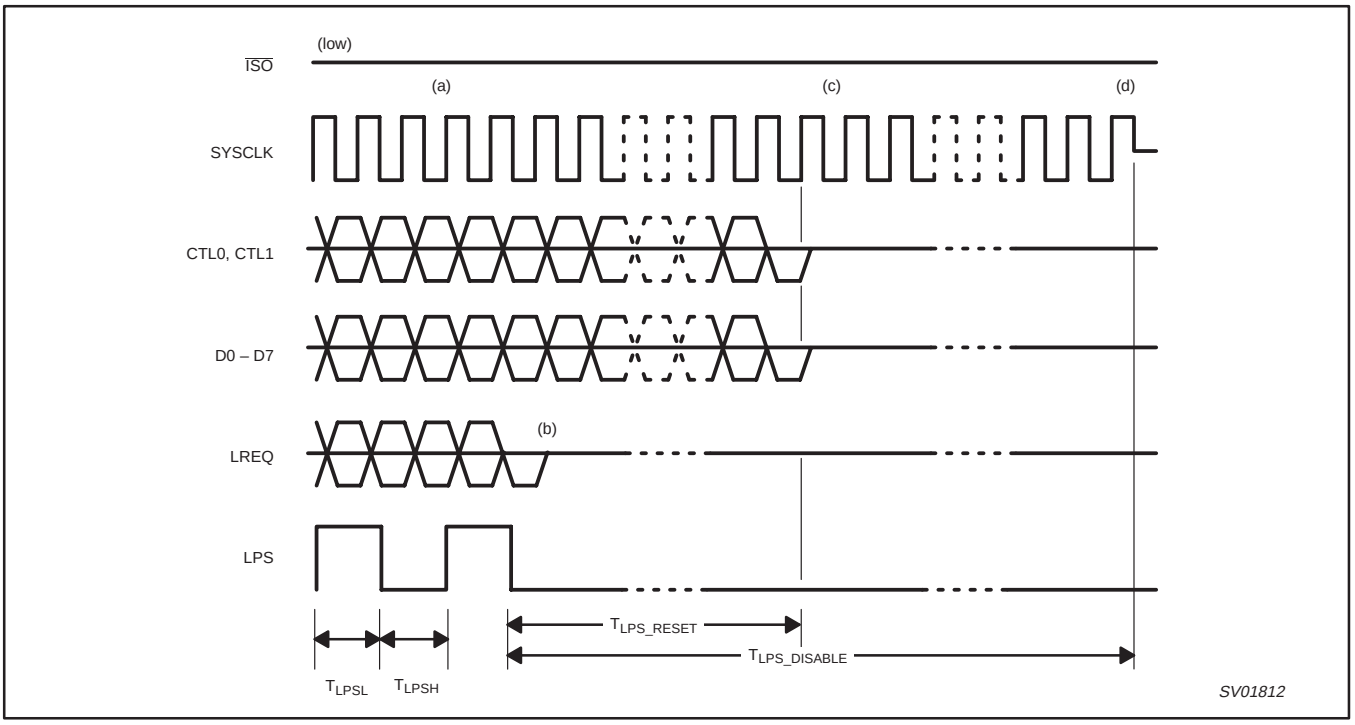


Figure 22. Interface Disable, $\overline{ISO}$ Low

The sequence of events for disabling the PHY-LLC interface when it is in the differentiated mode of operation ($\overline{ISO}$ terminal is low) is as follows:

1. Normal operation. Interface is operating normally, with LPS active, SYSCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line.
2. LPS deasserted. The LLC deasserts the LPS signal and, within 1 ms, terminates any request or interface bus activity, and places its LREQ, CTL, and D outputs into a high-impedance state (the LLC should terminate any output signal activity such that signals end in a logic 0 state).
3. Interface reset. After T_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and places its CTL and D outputs into a high-impedance state (the PHY will terminate any output signal activity such that signals end in a logic 0 state). The PHY-LLC interface is now in the reset state.
4. Interface disabled. If the LPS signal remain inactive for $T_{LPS\_DISABLE}$ time, the PHY terminates SYSCLK activity by placing the SYSCLK output into a high-impedance state. The PHY-LLC interface is now in the disabled state.

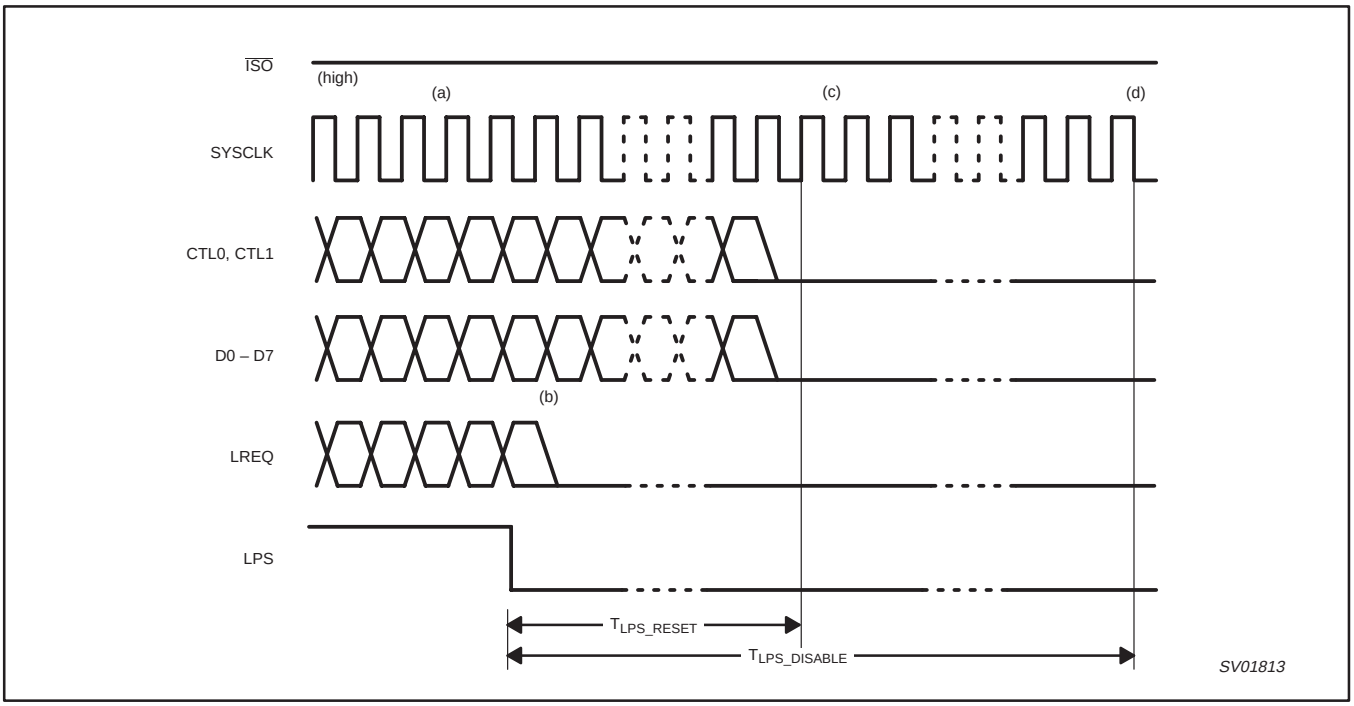


Figure 23. Interface Disable, $\overline{ISO}$ High

The sequence of events for disabling the PHY-LLC interface when it is in the non-differentiated mode of operation ($\overline{ISO}$ terminal is high) is as follows:

1. Normal operation. Interface is operating normally, with LPS active, SYSCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line.
2. LPS deasserted. The LLC deasserts the LPS signal and, within 1.0 ms, terminates any request or interface bus activity, places its CTL and D outputs into a high-impedance state, and drives its LREQ output low.
3. Interface reset. After T_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and drives its CTL and D outputs low. The PHY-LLC interface is now in the reset state.
4. Interface disabled. If the LPS signal remain inactive for $T_{LPS\_DISABLE}$ time, the PHY terminates SYSCLK activity by driving the SYSCLK output low. The PHY-LLC interface is now in the disabled state.

After the interface has been reset, or reset and then disabled, the interface is initialized and restored to normal operation when LPS is reasserted by the LLC. The timing for interface initialization is shown in Figure 24 and Figure 25.

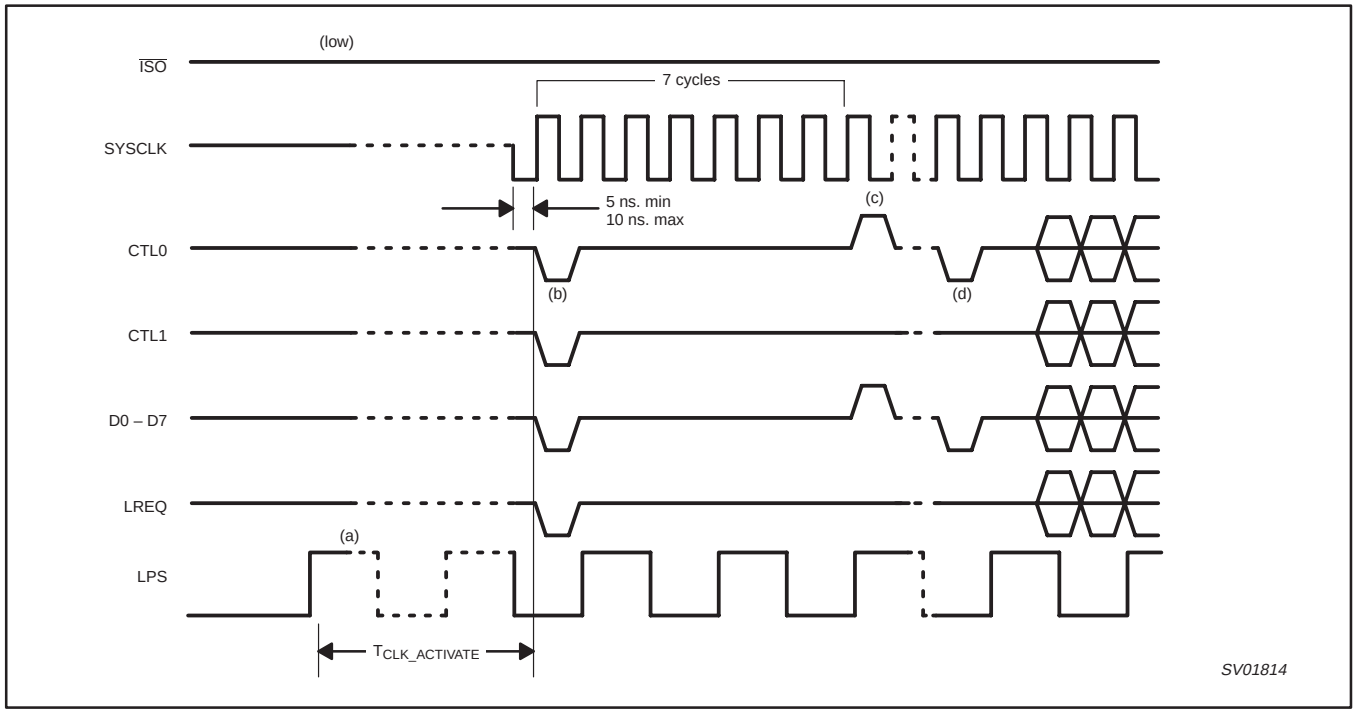


Figure 24. Interface Initialization, $\overline{ISO}$ Low

The sequence of events for initialization of the PHY-LLC interface when the interface is in the differentiated mode of operation ($\overline{ISO}$ terminal is low) is as follows:

1. LPS reasserted. After the interface has been in the reset or disabled state for at least the minimum $T_{RESTORE}$ time, the LLC causes the interface to be initialized and restored to normal operation by re-activating the LPS signal. (In the above diagram, the interface is shown in the disabled state with SYSCLK high-impedance inactive. However, the interface initialization sequence described here is also executed if the interface is merely reset but not yet disabled.)
2. SYSCLK activated. If the interface is disabled, the PHY re-activates its SYSCLK output when it detects that LPS has been reasserted. SYSCLK will be restored within 60 ns. The PHY commences SYSCLK activity by driving the SYSCLK output low for half a cycle. Thereafter, the SYSCLK output is a 50% duty cycle square wave with a frequency of 49.152 MHz +100 ppm (period of 20.345 ns). Upon the first full cycle of SYSCLK, the PHY drives the CTL and D terminals low for one cycle. The LLC is also required to drive its CTL, D, and LREQ outputs low during one of the first six cycles of SYSCLK (in the above diagram, this is shown as occurring in the first SYSCLK cycle).
3. Receive indicated. Upon the eighth SYSCLK cycle following reassertion of LPS, the PHY asserts the Receive state on the CTL lines and the data-on indication (all ones) on the D lines for one or more cycles (because the interface is in the differentiated mode of operation, the CTL and D lines will be in the high-impedance state after the first cycle).
4. Initialization complete. The PHY asserts the Idle state on the CTL lines and logic 0 on the D lines. This indicates that the PHY-LLC interface initialization is complete and normal operation may commence. The PHY will now accept requests from the LLC via the LREQ line.

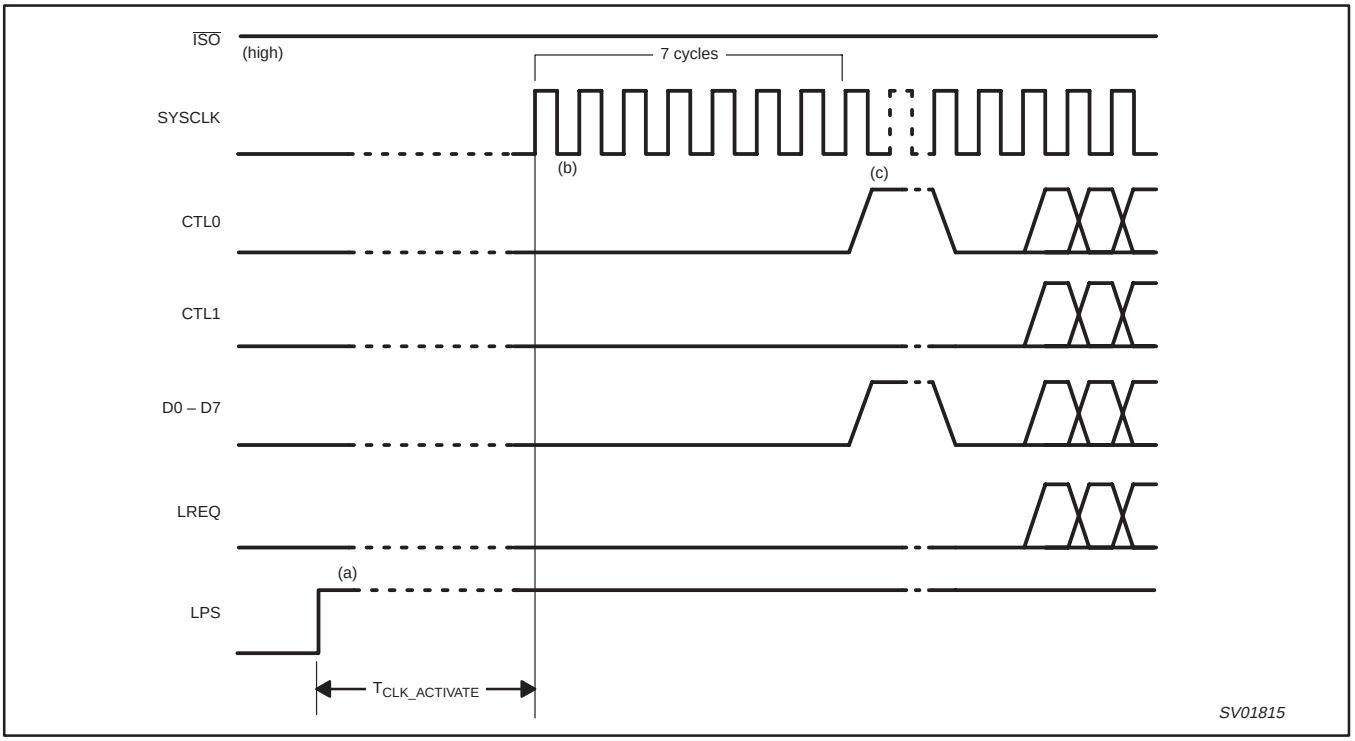


Figure 25. Interface Initialization, $\overline{ISO}$ High

The sequence of events for initialization of the PHY-LLC interface when the interface is in the non-differentiated mode of operation ($\overline{ISO}$ terminal is high) is as follows:

1. LPS reasserted. After the interface has been in the reset or disabled state for at least the minimum $T_{RESTORE}$ time, the LLC causes the interface to be initialized and restored to normal operation by reasserting the LPS signal. (In the above diagram, the interface is shown in the disabled state with SYSCLK low inactive. However, the interface initialization sequence described here is also executed if the interface is merely reset but not yet disabled.)
2. SYSCLK activated. If the interface is disabled, the PHY re-activates its SYSCLK output when it detects that LPS has been reasserted. SYSCLK will be restored within 60 ns. The SYSCLK output is a 50% duty cycle square wave with a frequency of 49.152 MHz +100 ppm (period of 20.345 ns). During the first seven cycles of SYSCLK, the PHY continues to drive the CTL and D terminals low. The LLC is also required to drive its CTL and D outputs low for one of the first six cycles of SYSCLK but to otherwise place its CTL and D outputs in a high-impedance state. The LLC continues to drive its LREQ output low during this time.
3. Receive indicated. Upon the eighth SYSCLK cycle following reassertion of LPS, the PHY asserts the Receive state on the CTL lines and the data-on indication (all ones) on the D lines for one or more cycles.
4. Initialization complete. The PHY asserts the Idle state on the CTL lines and logic 0 on the D lines. This indicates that the PHY-LLC interface initialization is complete and normal operation may commence. The PHY will now accept requests from the LLC via the LREQ line.

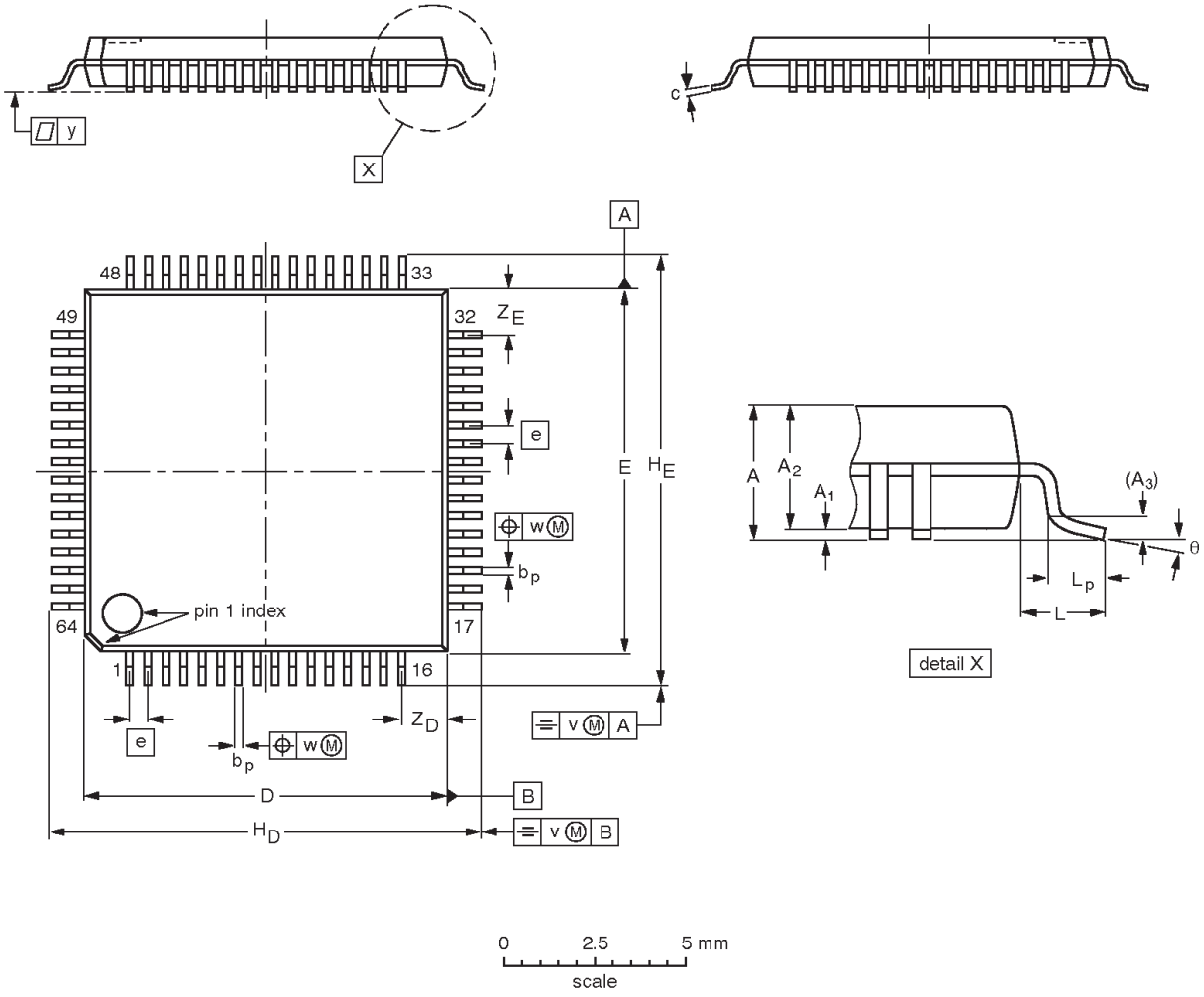
19.0 POWER-CLASS PROGRAMMING

The PC0–PC2 terminals are programmed to set the default value of the power-class indicated in the pwr field (bits 21–23) of the transmitted self-ID packet. Descriptions of the various power-classes are given in Table 21. The default power-class value is loaded following a hardware reset, but is overridden by any value subsequently loaded into the Pwr_Class field in register 4.

Table 21. Power Class Descriptions

PC0–PC2	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self powered, and provides a minimum of 15 W to the bus.
010	Node is self powered, and provides a minimum of 30 W to the bus.
011	Node is self powered, and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus and is using up to 3 W.
101	Node is powered from the bus and uses up to 3 W. No additional power is needed to enable the link.
110	Node is powered from the bus and uses up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and uses up to 3 W. An additional 7 W is needed to enable the link.

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

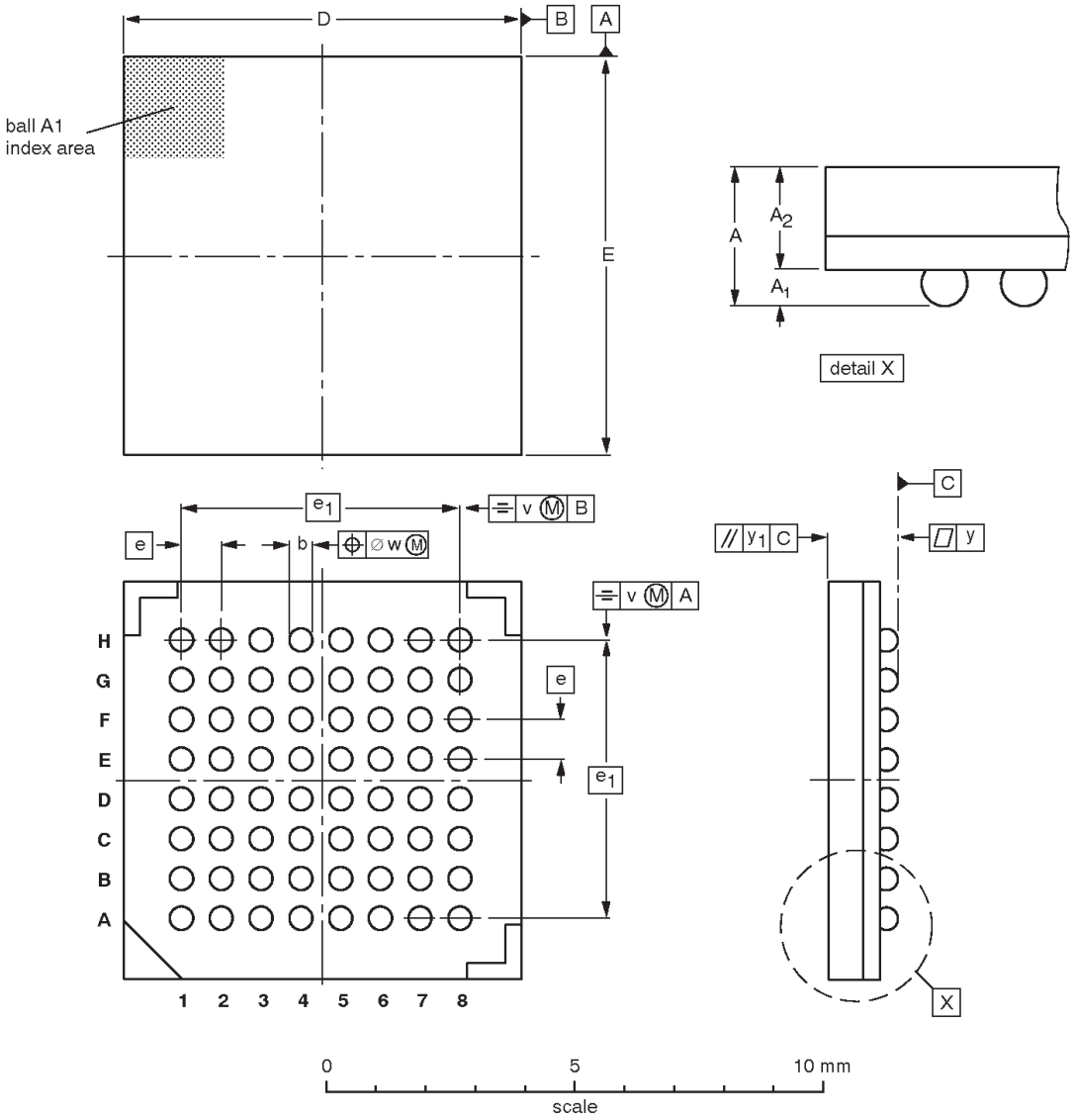
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2	136E10	MS-026				~~99-12-27~~ 00-01-19

LFBGA64: plastic low profile fine-pitch ball grid array package; 64 balls; body 8 x 8 x 1.05 mm **SOT534-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	v	w	y	y_1
mm	1.50	0.41 0.31	1.2 0.9	0.51 0.41	8.1 7.9	8.1 7.9	0.8	5.6	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT534-1						~~99-12-02~~ 00-03-04

NOTES

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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