DATA SHEET

PDI1394P11
3-port physical layer interface

Product specification
Supersedes data of 1998 Sep 24

1999 Apr 09

Philips
Semiconductors

PHILIPS

3-port physical layer interface PDI1394P11

1.0 FEATURES

- 3 cable interface ports
- Supports 100Mb/s and 200Mb/s transfers
- Interfaces to any 1394 standard Link Layer Controller
- 5V tolerant I/Os with Bus Holders
- Single 3.3V supply voltage
- Arbitrated (short) Bus Reset (1394a feature)

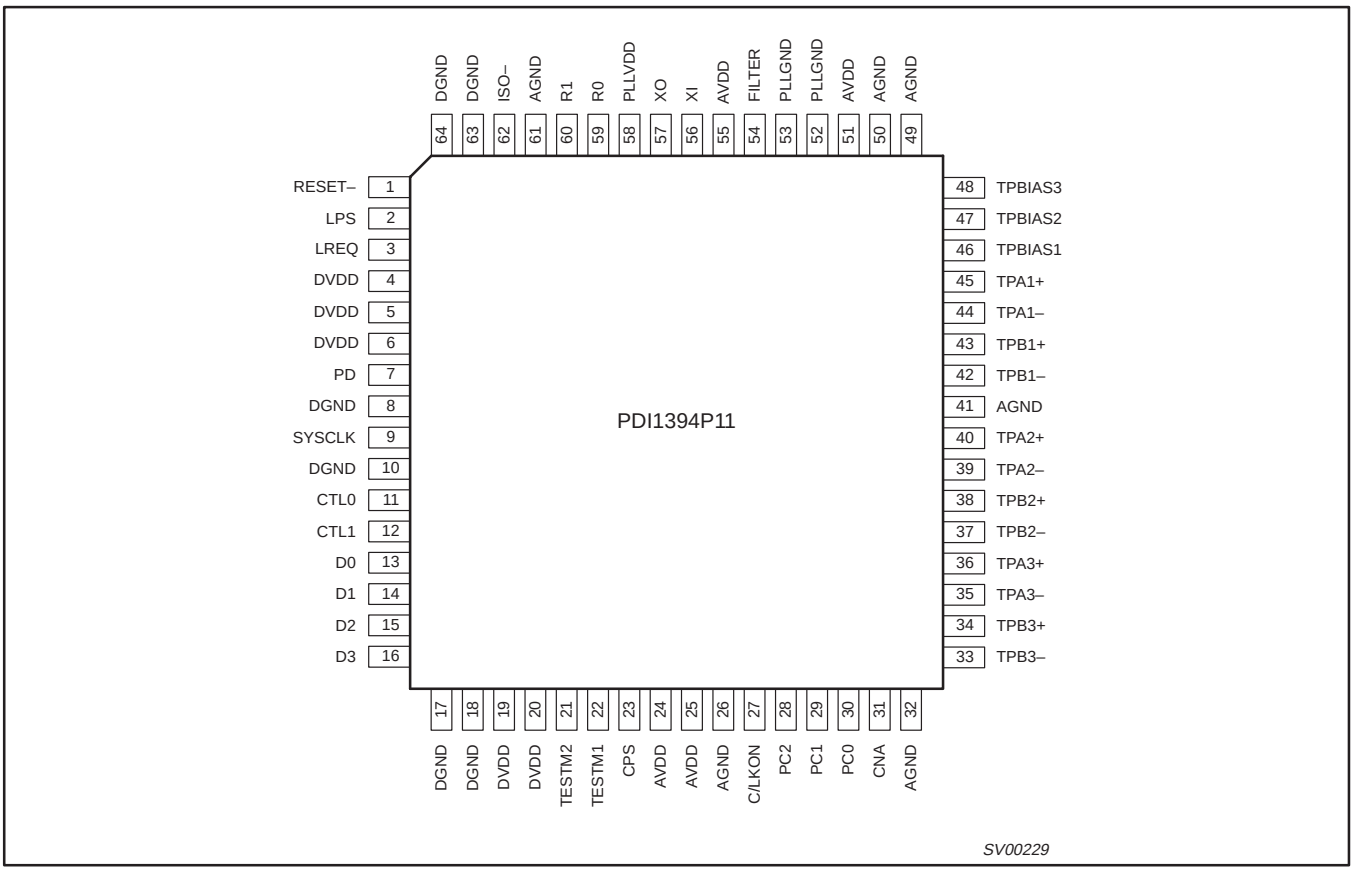
2.0 DESCRIPTION

The Philips Semiconductors PDI1394P11 is an IEEE1394-1995 compliant Physical Layer interface. The PDI1394P11 provides the analog physical layer functions needed to implement a three port node in a cable-based IEEE 1394–1995 network. Additionally, the device manages bus initialization and arbitration cycles, as well as transmission and reception of data bits. The Link Layer Controller interface is compatible with both 3V and 5V Link Controllers. While providing a maximum transmission data rate of 200 Mb/s, the PDI1394P11 is compatible with current 100 Mb/s Physical Layer ICs. The PDI1394P11 is available in the LQFP64 package.

3.0 ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
64-pin plastic LQFP	0°C to +70°C	PDI1394P11 BD	PDI1394P11 BD	SOT314-2

4.0 PIN CONFIGURATION

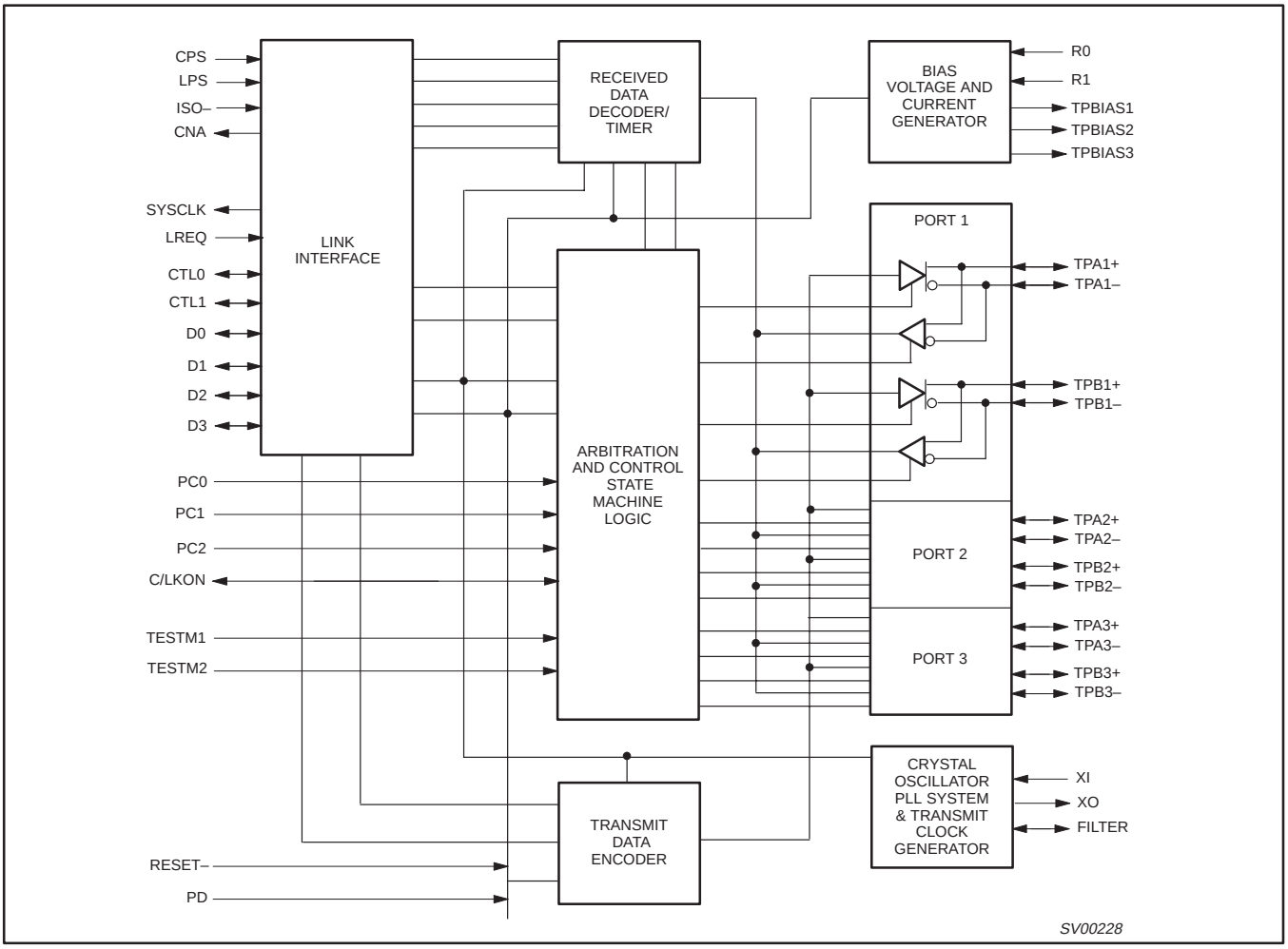


5.0 PIN DESCRIPTION

PIN NUMBER	PIN SYMBOL	I/O	NAME AND FUNCTION
1	RESET–	I*	Power up reset, active LOW
2	LPS	I*	Link Layer Controller (LLC) power status
3	LREQ	I*	Link request from controller
4	DVDD	I*	Should be connected to the LLC V_{DD} supply when a 5V LLC is connected to the Phy, and should be connected to the Phy DVDD when a 3V LLC is used.
5, 6, 19, 20	DVDD	I	Digital circuit power
7	PD	I*	Device power down input
8, 10, 17, 18, 63, 64	DGND	–	Digital circuit ground
9	SYSCLK	O*	49.152 MHz clock to link controller
11, 12	CTL[0:1]	I/O*	Link interface bi-directional control signals
13, 14, 15, 16	D[0:3]	I/O*	Link interface bi-directional data signals
22, 21	TESTM[1:2]	I*	Test/Mode Control pins 11 =1394–1995 mode 10 = 1394a mode 00/01 = Reserved
23	CPS	I	Cable power status
24, 25, 51, 55	AVDD	–	Analog circuit power
26, 32, 41, 49, 50, 61	AGND	–	Analog circuit ground
27	C/LKON	I/O*	Bus/Isochronous Resource Manager capable input, or LINK-ON signal output
30, 29, 28	PC[0:2]	I*	Power class bits 0 through 2 inputs
31	CNA	O*	Cable Not Active output
36, 40, 45	TPA[1:3]+	I/O	Port n cable pair A, positive signal
35, 39, 44	TPA[1:3]–	I/O	Port n cable pair A, negative signal
34, 38, 43	TPB[1:3]+	I/O	Port n cable pair B, positive signal
33, 37, 42	TPB[1:3]–	I/O	Port n cable pair B, negative signal
46, 47, 48	TPBIAS[1:3]	O	Cable termination voltage supplies
52, 53	PLLGND	–	PLL circuit ground
54	FILTER	I/O	PLL external filter capacitor
56	XI	I	Crystal oscillator connection
57	XO	O	Crystal oscillator connection
58	PLLVDD	–	PLL circuit power
59, 60	R[0:1]	–	External current setting resistor
62	ISO–	I*	Link interface isolation status input

NOTE:
* Indicates 5V tolerant structure.

6.0 BLOCK DIAGRAM



7.0 FUNCTIONAL SPECIFICATION

The PDI1394P11 is an IEEE1394–1995 High Performance Serial Bus Specification compliant physical layer interface device. It provides an interface between an attached link layer controller and three 1394 cable interface ports. In addition to the interface function, the PDI1394P11 performs bus initialization and arbitration functions as well as monitoring line conditions and connection status.

7.1 Clocking

The PDI1394P11 utilizes a stable internal reference clock of 196.608 MHz. The reference clock is generated using an external 24.576 MHz crystal and an internal Phase Locked Loop (PLL). The PLL clock is divided down to 49.152 MHz and 98.304 MHz clock signals. The 49.152 MHz clock is used for internal logic and provided as an output to clock a link layer controller. The 196.608 MHz and 98.304 MHz clocks are used for synchronization of the transmitted strobe and data information.

7.2 Port Interfaces

The PDI1394P11 provides the transceiver functions needed to implement a three port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. In addition to transmission and reception of packet data, the line transceivers monitor conditions on the cable to determine connection status, data speed, and bus arbitration states.

The PDI1394P11 receives data to be transmitted over the bus from two or four parallel data paths to the Link Controller, D[0:3]. These data paths are latched and synchronized with the 49.152 MHz clock. The parallel bit paths are combined serially, encoded and transmitted at either 98.304 Mb/s or 196.608 Mb/s, depending whether the transaction is a 100 Mb/s or 200 Mb/s transfer, respectively. The transmitted data is encoded as data-strobe information, with the data information being transmitted on the TPB cable pairs and the strobe information transmitted on the TPA cable pairs.

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair and the strobe information is received on the TPB cable pair. The combination of the data and strobe signals is decoded to recover the receive clock signal and the serial data stream. The serial data stream is converted to two or four parallel bit streams, resynchronized to the internal 49.152 MHz clock and sent to the

associated link controller. The received data is also transmitted out the other active cable ports.

The cable status, bus initialization and arbitration states are monitored through the cable interface using differential comparators. The outputs of these comparators are used by internal logic to determine cable and arbitration status. The TPA channel monitors the incoming cable common-mode voltage value during arbitration to determine the speed of the next packet transmission. The TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage, indicating the cable connection status.

The PDI1394P11 provides a nominal 1.85 V for driver load termination. This bias voltage, when seen through a cable by a remote receiver, is used to sense the presence of an active connection. The value of this bias voltage has been chosen to allow inter-operability between transceiver chips operating from either 5 V nominal supplies, or 3.3 V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor.

8.0 RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	DC supply voltage	Source/non-source power node	3.0	3.3	3.6	V
V_{IH}	High level input voltage	CMOS inputs	2.0		5.5	V
V_{IL}	Low level input voltage	CMOS inputs			0.8	V
$V_{ID–100}$	Differential input voltage	Cable inputs, 100Mbit operation	142		260	mV
$V_{ID–200}$	Differential input voltage	Cable inputs, 200Mbit operation	132		260	mV
$V_{ID–ARB}$	Differential input voltage	Cable inputs, during arbitration	171		262	mV
$V_{IC–100}$	Common mode voltage	TPB cable inputs, 100Mbit or speed signaling OFF, source power node	1.165		2.515	V
		TPB cable inputs, 100Mbit or speed signaling OFF, non–source power node	1.165		2.015	
$V_{IC–200SP}$	Common mode voltage	TPB cable inputs, 200Mbit or speed signaling, source power node	0.935		2.515	V
		TPB cable inputs, 200Mbit or speed signaling, non–source power node	0.935		2.015	
	Receive input jitter	TPA, TPB cable inputs, 100Mbit operation			±1.08	ns
		TPA, TPB cable inputs, 200Mbit operation			±0.5	ns
	Receive input skew	Between TPA and TPB cable inputs, 100Mbit operation			±0.8	ns
		Between TPA and TPB cable inputs, 200Mbit operation			±0.55	ns
I_{OL}/I_{OH}	Output current, I_{OL}/I_{OH}	SYSCLK	–16		16	mA
		Control, Data, CNA, C/LKON	–12		12	
I_O	Output current	TPBIAS outputs	–3		1.3	mA
f_{XTAL}	Crystal frequency	Parallel resonant fundamental mode crystal	24.5735	24.576	24.5785	MHz
T_{amb}	Operating ambient temperature range in free air		0		+70	°C

9.0 ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC supply voltage		–0.3	4.6	V
V_I	DC input voltage[3]	Inputs CPS, TPAn, TPBn, FILTER, XI	–0.5	V_{DD}+0.5	V
$V_{I,5t}$	DC input voltage	5V tolerant digital inputs RESET–, LPS, LREQ, PD, CTL[0:1], D[0:3], TESTM[2:1], C/LKON, PC[0:2], ISO–	–0.5	5.5	V
V_O	DC output voltage[3]		–0.5	V_{DD}+0.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
I_{OK}	DC output diode current	$V_O < 0$ or $V_O > V_{DD}$	–	±50	mA
T_{stg}	Storage temperature range		–65	+150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

10.0 CABLE DRIVER

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
V_{OD}	Differential output voltage	56 Ω load	172		265	mV
$I_{O(diff)}$	Difference current, TPA+, TPA–, TPB+, TPB–	Driver enabled, speed signaling OFF	–1.05[1]		1.05[1]	mA
I_{SP}	Common mode speed signaling current, TPB+, TPB–	200Mbit speed signaling enabled	+2.53[2]		+4.84[2]	mA
V_{OFF}	OFF state common mode voltage	Drivers disabled			20	mV

NOTES:
1. Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– algebraic sum of driver currents.
2. Limits defined as one half of the algebraic sum of currents flowing into TPB+ and TPB–.

11.0 CABLE RECEIVER

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
I_{IC}	Common mode input current	Driver disabled	–20		20	µA
Z_{ID}	Differential input impedance	Driver disabled	15			kΩ
					6	pF
Z_{IC}	Common mode input impedance	Driver disabled	20			kΩ
					24	pF
V_{TH}	Receiver input threshold voltage		–60		60	mV
V_{TH}	Cable bias detect threshold, TPBn cable inputs	Driver disabled	0.6		1.0	V

12.0 OTHER DEVICE I/O

SYMBOL	PARAMETER	TEST CONDITION		LIMITS			UNIT
				MIN	TYP	MAX	
I_{DD}	Supply current	V_{DD} = 3.3 V	One port transmitting One port receiving One port not connected		60		mA
		V_{DD} = 3.6 V				175	mA
		V_{DD} = 3.6 V	Power-down mode	1.5	2	5	mA
V_P	Cable Power Threshold Voltage	R_L = 400 kΩ to CPS pin		4.7		7.5	V
V_{OH}	High-level output voltage	I_{OH} = Max., V_{DD} = Min.		V_{DD} – 0.55			V
V_{OL}	Low-level output voltage	I_{OL} = Min., V_{DD} = Max.				0.5	V
I_I	Input current, LREQ, LPS, PD, TESTM[1:2]	V_I = 5.5 V or 0 V, ISO– = 0				±1.0	µA
I_{OZ}	OFF-state output current, CTLn, Dn, C/LKON I/Os, PC[0:2] inputs	V_O = 5.5 V or 0 V, ISO– = 0				±5.0	µA
I_{PU}	Pullup current, RESET– input	V_I = 1.5 V		–20	–40	–80	µA
		V_I = 0 V		–22	–45	–90	µA
I_{PD}	Pulldown current, RESET– input	V_I = V_{DD} PD = high		100	260	450	µA
	Power-up reset time, RESET– input	C = 0.1 µf		2			ms
V_{TH}^+	Positive arbitration comparator threshold voltage			89		168	mV
V_{TH}^-	Negative arbitration comparator threshold voltage			–168		–89	mV
$V_{TH–SP}$	Speed signal input threshold voltage			49		131	mV
V_{IT}^+	Positive going input threshold voltage, LREQ, CTLn, Dn inputs			V_{DD}/2 + 0.12		V_{DD}/2 + 0.66	V
V_{IT}^-	Negative going input threshold voltage, LREQ, CTLn, Dn inputs			V_{DD}/2 – 0.66		V_{DD}/2 – 0.12	V
V_O	TPBIASn output voltage			1.665	1.85	2.015	V
I_b	Absolute value of bus holding current LREQ, PD, CTLn, Dn inputs, LPS	ISO– = high, V_I = 0.5 V_{DD}			190		µA

13.0 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
RΘjA	Junction-to-free-air thermal resistance	Board mounted, no air flow		92.5		°C/W
RΘjC	Junction-to-case thermal resistance			10.4		°C/W

14.0 AC SWITCHING CHARACTERISTICS

SYMBOL	PARAMETER	MEASURED	TEST CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
	Transmit jitter	TPA, TPB				±0.25	ns
	Transmit skew	Between TPA and TPB				±0.15	ns
t_r	Transmit rise time	10% to 90%	R_L= 56Ω, C_L= 10 pF			2.2	ns
t_f	Transmit fall time	90% to 10%	R_L= 56Ω, C_L= 10 pF			2.2	ns
t_{su}	Dn, CTLn, LREQ input setup time to SYSCLK	50% to 50%	See Figure 1	5			ns
t_H	Dn, CTLn, LREQ input hold time from SYSCLK	50% to 50%	See Figure 1	2			ns
t_D	Delay time, SYSCLK to Dn, CTLn	50% to 50%	See Figure 2	2		13	ns

15.0 SWITCHING WAVEFORMS

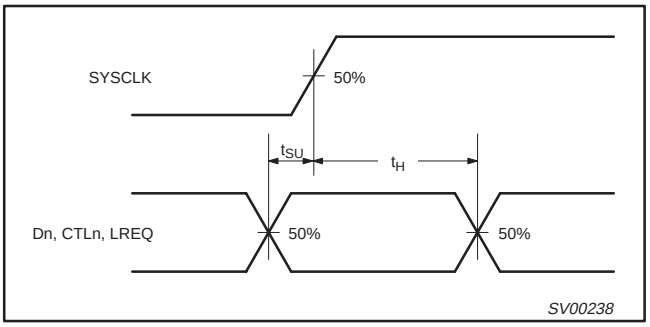


Figure 1. Dn, CTLn, LREQ input setup and hold times

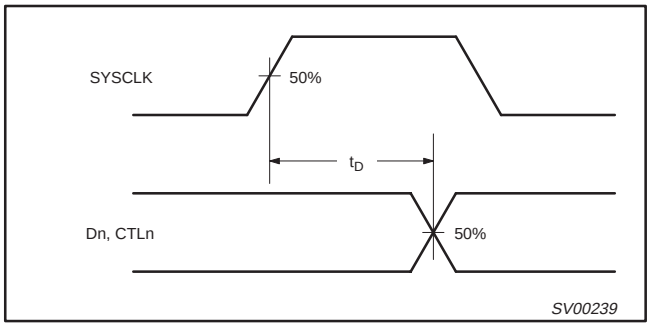


Figure 2. Dn, CTLn, output delay relative to SYSCLK

16.0 INTERNAL REGISTER CONFIGURATION

The accessible internal registers of this device are listed in the following tables:

ADDRESS	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	GC					
0010	SPD		Reserved		NP			
0011	AStat1		BSTAT1		Ch1	Con1	Reserved	
0100	AStat2		BSTAT2		Ch2	Con2	Reserved	
0101	AStat3		BSTAT3		Ch3	Con3	Reserved	
0110	Loopint	CPSint	CPS	IR	Reserved			C
0111	Reserved				PC2	PC1	PC0	C
1000	Reserved							
1001	Reserved							ISBR

The keys are listed as follows:

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	Rd	The address of the local node determined during the Self-ID.
R	1	Rd	Indicates that the local node is the root.
CPS	1	Rd	Cable power Status (CPS input).
RHB	1	Rd/Wr	Root hold-OFF bit. Instructs the local node to try to become the root during the next bus reset.
IBR	1	Rd/Wr	Initiate Bus Reset. Instructs the PDI1394P11 to initiate Bus Reset at the next opportunity.
GC	6	Rd/Wr	Gap count. Used to optimize the gap times based on the size of the network. See 1394 standard for details.
SPD	2	Rd	Indicates the top signaling speed of the local ports.
NP	4	Rd	The number of ports on this device, set to 0011.
AStat(n)	2	Rd	The line state of TPA of port n: 11 = Z 01 = 1 10 = 0 00 = invalid data state. Power up reset initializes to this line state. Also this line state is output during transmit and receive operations. The line state outputs are generally valid during arbitration and idle conditions on the bus.
BStat(n)	2	Rd	The line state of TPB of port n. The encoding is the same as AStat(n).
Ch(n)	1	Rd	If = 1, then port n is a child, otherwise it is a parent.
Con(n)	2	Rd	If = 1, then port n is connected, otherwise it is disconnected.
Loopint	1	Rd/Wr	Indicates that the PDI1394P11 times out in tree ID, waiting for child signal from two or more ports. The Loopint can be cleared by writing a “0” to this bit, but if the loop configuration has not been corrected, it will promptly return to a “1”.
CPSint	1	Rd/Wr	Indicates that the cable power has dropped too low for guaranteed reliable operation. It can be cleared by writing a “0” to the bit, but it will immediately return if CPS is still LOW.
CPS	1	Rd/Wr	Cable Power Status is also included in this register to expedite handling the CPSint.
IR	1	Rd/Wr	Indicates that the last bus reset was initiated in the PDI1394P11. This bit is also included in the self ID packet.
C	1	Rd	If set, this node is a contender for the role of bus or Isochronous Resource Manager.
PC2	1	Rd	The least significant power class bit
PC1	1	Rd	The middle power class bit
PC0	1	Rd	The most significant power class bit
ISBR	1	Rd/Wr	Initiate Short Bus Reset. Instructs the PDI1394P11 to initiate an arbitrated short bus reset. See Section 17.1.

17.0 APPLICATION INFORMATION

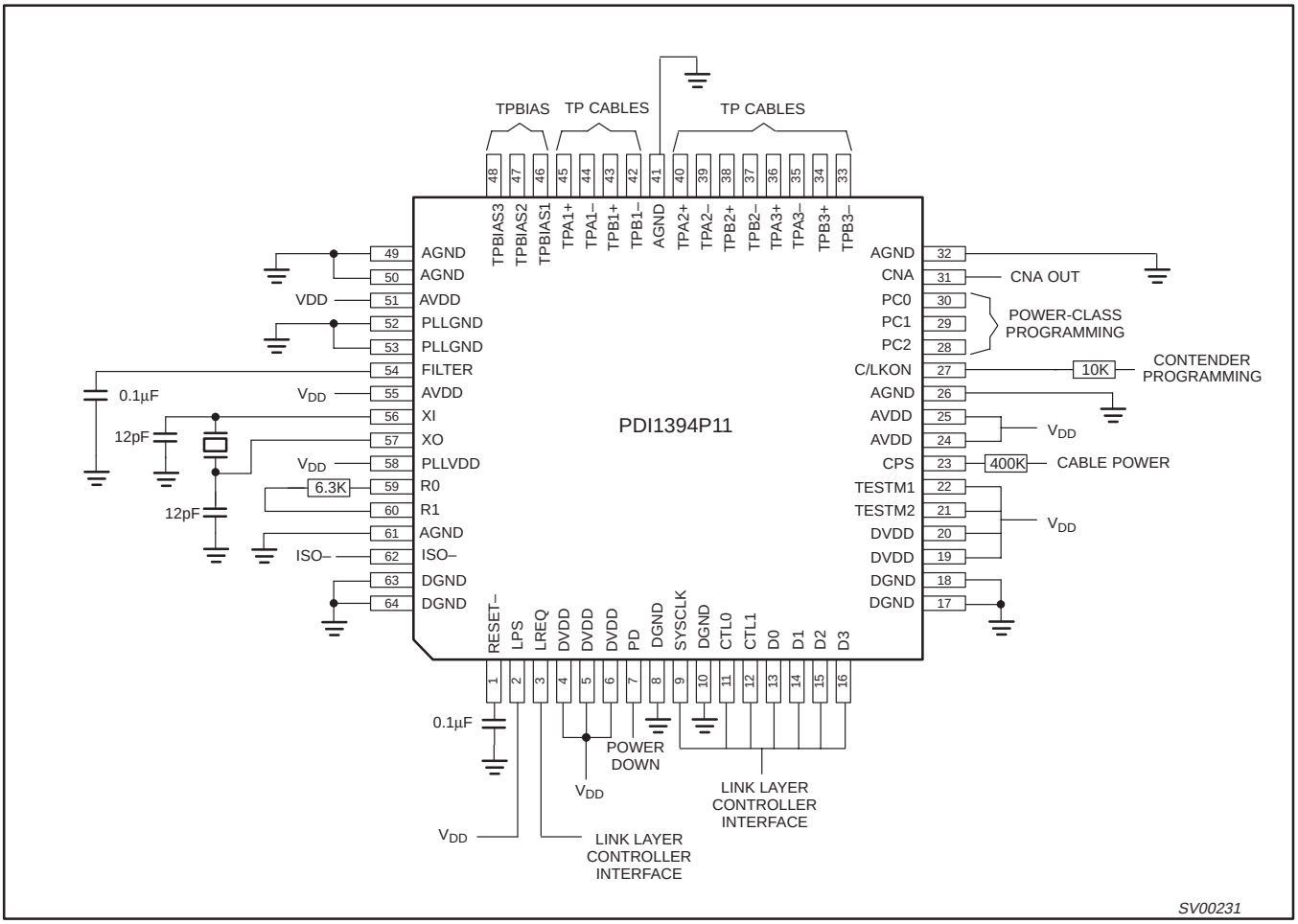


Figure 3. External Component Connections

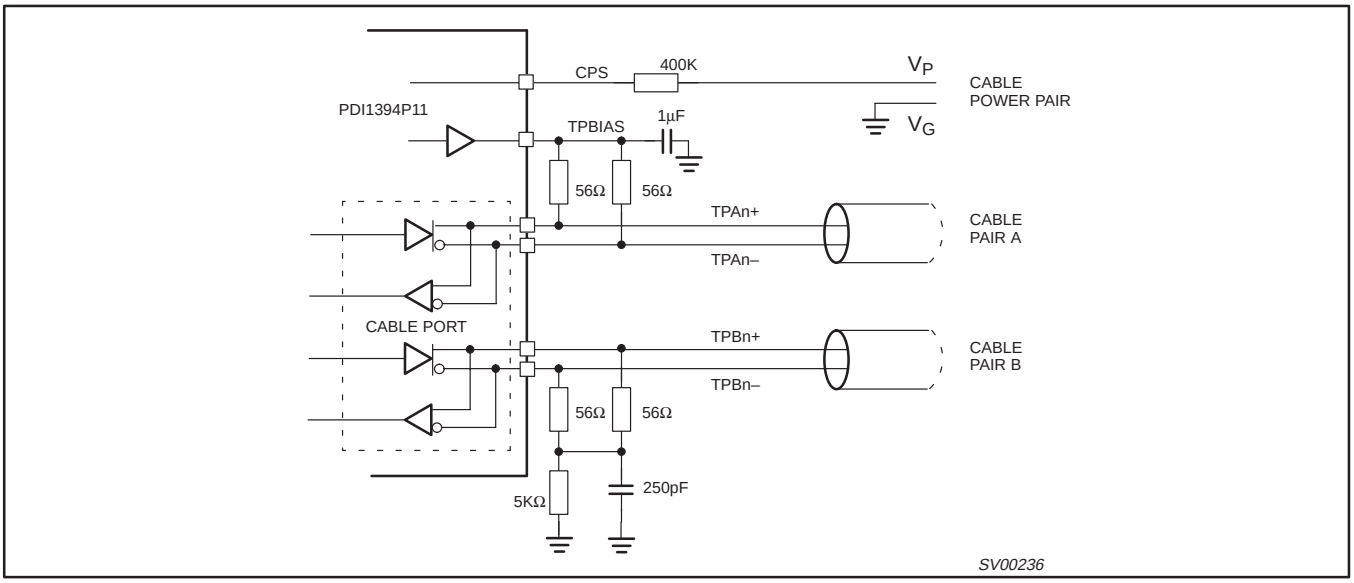


Figure 4. Twisted pair cable interface connections

17.1 Arbitrated (short) Bus Reset

A 1394-1995 software initiated bus reset assumes that the state of the bus is unknown when reset occurs and requires that the reset be long enough to permit the longest transaction to finish and still complete reset (167µs min. to 250µs max.). The total duration of bus initialization is longer than the nominal isochronous cycle time (125µs) and may disrupt two isochronous periods. This compels device designers to add additional buffer depth to preserve the smooth flow of isochronous data from the perspective of their application. If a node that initiates a reset arbitrates for control of the bus prior to asserting reset, arbitration time can be shortened significantly (1.3µs min. to 80µs max.). This 1394a concept is known as Arbitrated (short) Bus Reset, and is incorporated in the PDI1394P11.

The TESTM2 (pin 21) pins is used to enable Arbitrated (short) Bus Reset mode. In 1394-1995 mode, this pin is tied high. In this mode, an arbitrated bus reset cannot be initiated from this node and will be treated as a “long” bus reset if initiated by another node. In accordance with the 1394-1995 spec, all bus resets on the entire bus will be “long”.

To enable Arbitrated (short) Bus Reset mode, set TESTM2 low. With the part in this mode, writing a 1 to the ISBR (Initiate Short Bus Reset) bit (bit 7) of Phy register 9 initiates an arbitrated bus reset. This mode also allows the Phy to recognize arbitrated bus resets initiated by other nodes. Non-arbitrated bus resets can still be initiated from this node and are recognized and processed correctly when initiated by another node.

17.2 Setting the CPS Trip Point

The Cable Power Status (CPS) pin (pin 23) is used to monitor the cable power. When cable power voltage has dropped too low for reliable operation, internal circuitry trips, which clears the CPS bits in the Phy registers (bit 7 of register 0, and bit 2 of register 6). This action causes a cable power status interrupt which sets the CPSint bit in the Phy registers (bit 1 of register 6). This bit can be cleared by a hardware reset or by writing a 0 to the CPSint bit. However, if the CPS input is still low, another cable-power status interrupt immediately occurs. The cable voltage at which these events occur is adjustable on the PDI1394P11.

The external resistor (R) needed to set the CPS trip voltage (V_{cable}) to a desired voltage can be calculated using the following equation:

$$R = \frac{(V_{cable} - 1.85V)}{10\mu A}$$

The external and internal circuitry associated with the CPS pin is illustrated in Figure 5.

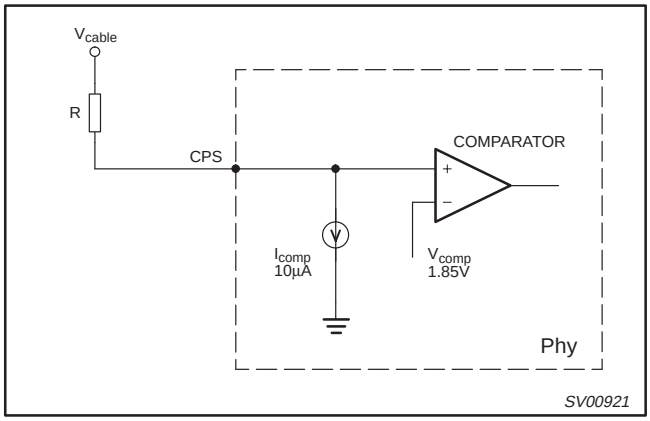


Figure 5.

Some typical threshold voltage values and their associated resistor values are shown in Table 1.

Table 1. Typical threshold voltage values

V_{cable} (V)	R (kΩ)	V_{cable} DETECTOR TOLERANCE % WITH:	
		R of 5%	R of 2%
5	315	6.8	4.4
6	415	7.3	4.8
7	515	7.8	5.2
8	615	8.3	5.6
9	715	8.8	6.0

18.0 EXTERNAL COMPONENTS AND CONNECTIONS

18.1 Logic Reset input (RESET–, pin 1)

Forcing this pin low causes a Bus Reset condition on the active cable ports, and resets the internal logic to the Reset Start state. SYSCLK remains active. An internal pull-up resistor is provided that is connected to V_{DD}, so only an external delay capacitor is required. This input is a standard logic buffer and may also be driven by an open drain logic output buffer. The RESET pin also has a n-channel pull-down transistor activated by the PD (Power Down) pin.

18.2 Link Power Status input (LPS, pin 2)

In a non-isolated implementation a 10kΩ resistor is connected to the V_{DD} supplying the link layer controller to monitor the link's power status. In an isolated implementation a square wave with a minimum frequency of 500 kHz can be applied to the LPS pin to indicate the pin is powered. If the link is not powered on the Control I/O's (pins 11,12), Data I/O's (pins 13 – 16) and SYSCLK output (pin 9) are disabled, and the PDI1394P11 will perform only the basic repeater functions required for network initialization and operation.

18.3 Link Request input (LREQ, pin 3)

LREQ is a signal from the link layer controller used to request the PDI1394P11 to perform some service. This pin supports an optional isolation barrier.

18.4 Power Down input (PD, pin 7)

This input powers down all device functions with the exception of the CNA circuit to conserve power in portable or battery powered applications. It must be held high for at least 3.5ms to assure a successful reset after power down. This pin supports an optional isolation barrier.

18.5 System Clock output (SYSCLK, pin 9)

Provides a 49.152 MHz clock signal, synchronized with the data transfers, to the link layer controller. This pin supports an optional isolation barrier.

18.6 Control I/Os (CTL[0:1], pins[11,12])

These are bi-directional signals used in the communication between the PDI1394P11 and the link layer controller that control passage of information between the two devices. These pins support an optional isolation barrier.

18.7 Data I/Os (D[0:3], pins [13,14,15,16])

These are bi-directional information signals used in the communication between the PDI1394P11 and the link layer controller. These pins support an optional isolation barrier.

18.8 Test Mode control and ISBR mode inputs (TESTM[1:2], pins[22,21])

These two logic signals are used in manufacturing to enable production line testing of the PDI1394P11. For normal use these should be tied to V_{DD}. To enable ISBR (Arbitrated (short) bus reset) mode, set TESTM1 high and TESTM2 low. See section 17.1 for more information on ISBR mode.

18.9 Cable Power Status input (CPS, pin 23)

This is normally connected to the cable power through an external resistor. The circuit drives an internal comparator which is used to detect the presence of cable power. This information is maintained in an internal register and is available to the link layer controller through a register read. See section 17.2 for information on setting the CPS trip point.

18.10 Bus or Isochronous Resource Manager Capable input or Link-On output (C/LKON, pin 27)

This is a bi-directional pin that is used as an input to specify, in the Self-ID packet, that the node is Bus or Isochronous Resource Manager Capable. As an output it signals the reception of a Link-On message by supplying a 6.114 MHz signal. The bit value programming is done by tying the pin through a 10kΩ resistor to a high (V_{DD}) or low (GND). The use of the series resistor allows the Link-On to override the input value when necessary.

18.11 Power Class bits 0 through 2 inputs (PC[0:2], pins [30,29,28])

Used as inputs to set the bit values of the three Power Class bits in the self-ID packet (bits 21, 22 and 23). These bits can be programmed by tying the pins high to V_{DD} or low to GND.

18.12 Cable Not Active output (CNA, pin 31)

This pin outputs the cable connection status. If all ports are disconnected this pin outputs a high. If any port has a cable connected then this pin outputs a low.

18.13 Twisted Pair I/O's (TPA[1:3]+, pins [45, 40, 36], TPA[1:3]–, pins [44,39,35], TPB[1:3]+, pins [43,38,34], TPB[1:3]–, pins [42, 37, 33])

These pins send and receive differential data over the twisted pair cables. Two series connected external 56 Ω cable termination resistors are required at each twisted pair. Each unused TPB pin must be tied through a 5kΩ resistor to ground. The TPA pins can be left floating.

18.14 Twisted Pair Bias outputs (TPBIAS[1:3], pins [46, 47, 48])

These outputs provide the 1.86 V nominal bias voltage needed for proper operation of the twisted pair cable drivers, and for signaling to the remote nodes that there is a valid cable connection. Three TPBIAS outputs are provided for separate connection to each of the three TPA twisted pairs to provide electrical isolation. A 1μF capacitor to ground must be connected to each TPBIAS pin whether it is used or not.

18.15 PLL Filter (FILTER, pin 54)

This pin is connected to an external filter capacitor used in a lag-lead filter for a PLL frequency multiplier running off of the crystal oscillator.

18.16 Oscillator crystal (XI, pin 56 & XO, pin 57)

These pins connect to a 24.576 MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used, the suggested values of 12 pF are appropriate for one specified for 15 pF loads.

18.17 Current setting resistor (R[0:1], pins [59,60])

An internal reference voltage is applied across the resistor connected between these two pins to set the internal operating and the cable driver output currents. A low TCR (<150ppm/°C temperature coefficient) with a value of 6.34 kΩ ±1% should be used to meet the 1394 standard output voltage limits.

18.18 Isolation Barrier disable (ISO–, pin 62)

When ISO– is high, busholder circuits are enabled on the LREQ, PD, and LPS input pins and on the CTL, and Data bidirectional pins. This mode also allows isolation using a single 1nF capacitor per signal line. When ISO– is low, busholder circuits are disabled and isolation can be realized by using the scheme explained in Annex J of the 1394–1995 spec.

18.19 Supply filters (AVDD, pins [24, 25, 51, 55], DVDD, pins [5,6,19,20], and PLLVDD, pin 58)

A combination of decoupling capacitors is suggested for each supply group, such as paralleled 10 µF and 0.1 µF. The high frequency 0.1 µF capacitors should be mounted as close as possible to the PDI1394P11 device supply leads. These supply lines are separated on the IC to provide noise isolation. They should be tied together at a low impedance point on the circuit board. Individual filter networks are desirable.

Details of a phy-link Interface supporting an optional isolation barrier are provided in Annex J of the 1394 standard.

19.0 PRINCIPLES OF OPERATION

The PDI1394P11 is designed to operate with a link layer controller. These devices use an interface such as described in Annex J of the 1394 standard. The following describes the operation of the phy-link interface.

19.1 Data Transfer and Clock rates

The PDI1394P11 supports 100/200 Mbit/s data transfer, and has four bi-directional data lines D[0:3] crossing the interface. In 100 Mbit/s operation only D[0:1] pins are used, in 200 Mbit/s operations all D[0:3] pins are used for data transfer. The unused D[n] pins are driven low. In addition there are two bi-directional control lines CTL[0:1], the 50 MHz SYSCLK line from the phy to the link, and the link request line LREQ from the link to the phy. The PDI1394P11 has control of all the bi-directional pins. The link is allowed to drive these pins only after it has been given permission by the phy. The dedicated LREQ request pin is used by the link for any activity which it wishes to initiate.

When the phy has control of the bus the CTL[0:1] lines are encoded as follows:

CTL [0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	No activity is occurring (this is the default mode).
01	Status	Status information is being sent from the phy to the link.
10	Receive	An incoming packet is being sent from the phy to the link.
11	Grant	The link has been given control of the bus to send an outgoing packet.

When the link has control of the bus (phy permission) the CTL[0:1] lines are encoded as follows:

CTL [0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	The link releases the bus (transmission has been completed).
01	Hold	The link is holding the bus while data is being prepared for transmission or sending another packet without arbitrating.
10	Transmit	An outgoing packet is being sent from the link to the phy.
11	NA	None

19.2 Request

When the link layer controller wishes to request the bus, or access a register that is located in the PDI1394P11, a serial stream of information is sent across the LREQ line. The length of the stream will vary depending on whether the transfer is a bus request, a read command, or a write command. Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream, and a stop bit of 0 is required at the end of the stream. Bit 0 is the most significant, and is transmitted first. The LREQ line will be required to idle low (logic level 0).

19.2.1 Link Layer Controller Bus Request

For a Bus Request, the length of the LREQ data stream is 7 bits as follows:

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1)
1–3	Request Type	Indicates the type of bus request (see the table below for the encoding of this field)
4–5	Request Speed	This should be 00 for PDI1394P11's 100 Mbit/s speed and 01 for 200 Mbit/s speed.
6	Stop Bit	Indicates the end of the transfer (always 0)

19.2.2 Link Layer Controller Requests Read Register Access

For a Read Register Request, the length of the LREQ data stream is 9 bits as follows:

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1)
1–3	Request Type	Always a 100 indicating that this is a read register request
4–7	Address	The address of the phy register to be read
8	Stop Bit	Indicates the end of the transfer (always 0)

19.2.3 Link Layer Controller Requests Write Register Access

For a Write Register Request, the length of the LREQ data stream is 17 bits. The details of bits are as shown below:

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1)
1–3	Request Type	Always a 101 indicating that this is a write register request
4–7	Address	The address of the phy register to be written to
8–15	Data	The data that is to be written to the specified register address
16	Stop Bit	Indicates the end of the transfer (always 0)

19.2.4 Other Requests and LREQ

The three bit Request Type field has the following possible values:

BIT(S)	NAME	DESCRIPTION
000	ImmReq	Immediate request: Upon detection of an idle, take control of the bus immediately (no arbitration)
001	IsoReq	Isochronous request: Arbitrate for the bus, no gaps
010	PriReq	Priority request: Arbitrate after a subaction gap, ignore fair protocol
011	FairReq	Fair request: Arbitrate after a subaction gap, follow fair protocol
100	RdReg	Return the specified register contents through a status transfer
101	WrReg	Write to the specified register
110, 111	Reserved	Reserved

19.3 Operation of LREQ

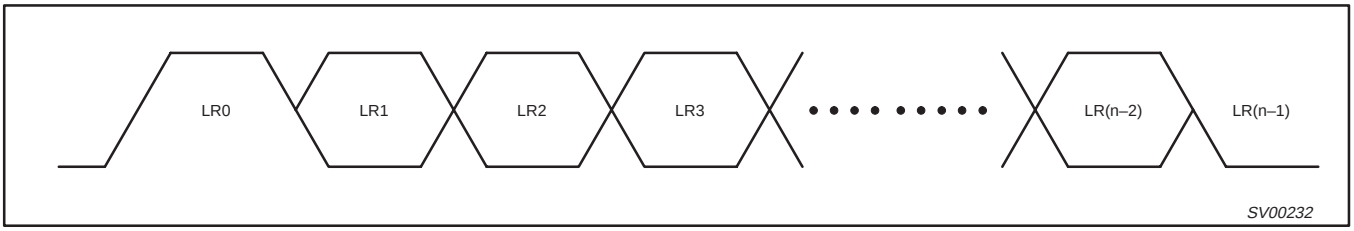


Figure 6. LREQ Input Sequence (each cell represents one SYSCLK sample time)

For fair or priority access, the link requests control of the bus at least one clock after the phy-link interface becomes idle. If the link senses that the CTL pins are in a receive state (CTL[0:1] = 10), then it will know that its request has been lost. This is true anytime during or after the link sends the bus request transfer. Additionally, the phy will ignore any fair or priority requests if it asserts the receive state while the link is requesting the bus. The link will then reissue the request one clock after the next interface idle.

The cycle master uses a normal priority request to send a cycle start message. After receiving a cycle start, the link can issue an isochronous bus request. When arbitration is won, the link proceeds with the isochronous transfer of data. The isochronous request will be cleared by the phy once the link sends another type of request or when the isochronous transfer has been completed.

The ImmReq request is issued when the link needs to send an acknowledgment after reception of a packet address to it. This request must be issued during packet reception. This is done to minimize the delays that a phy would have to wait between the end of a packet and the transmittal of an acknowledgment. As soon as the packet ends, the phy immediately grants access of the bus to the link. the link will send an acknowledgment to the sender unless the header CRC of the packet turns out to be bad. In this case, the link will release the bus immediately; it will not be allowed to send another type of packet on this grant. To guarantee this, the link will be forced to wait 160 ns after the end of the packet is received. The phy then gains control of the bus and the ack with the CRC error is sent. Then the bus is released and allowed to proceed with another request.

Although highly improbable, it is conceivable that the two separate nodes will believe that an incoming packet is intended for them. The nodes then issue a ImmReq request before checking the CRC of the packet. Since both phys will seize control of the bus at the same time, a temporary, localized collision of the bus will occur somewhere between the competing nodes. This collision would be interpreted by the other nodes on the network as being a ‘ZZ’ line state, not a bus reset. As soon as the two nodes check the CRC, the mistaken node will drop its request and the false line state will be removed. The only side effect would be the loss of the intended acknowledgment packet (this will be handled by the higher-layer protocol).

19.4 Read/Write Requests

When the link requests to read the specified register contents, the phy will send the contents of the register to the link through a status transfer. If an incoming packet is received while the phy is transferring status information to the link, the phy will continue to attempt to transfer the contents of the register until it is successful.

For write requests, the phy will load the data field into the appropriately addresses register as soon as the transfer has been completed. The link will be allowed to request read or write operations at any time.

19.5 Status

A status transfer is initiated by the phy when it has status information to transfer to the link. The phy will wait until the interface is idle before starting the transfer. The transfer is initiated by asserting the following on the control pins: CTL[0:1] = 01 along with the first two bits of status information on the D[0:1] pins. The phy maintains CTL[0:1] = 01 for the duration of status transfer. The phy may prematurely end a status transfer by asserting something other than CTL[0:1] = 01 on the control pins. This could be caused by an incoming packet from another node. The phy will continue to attempt to complete the transfer until the information has been successfully transmitted. There must be at least one idle cycle in between consecutive status transfers.

The phy normally sends just the first four bits of status to the link. These bits are status flags which are needed by the link state machines. The phy sends an entire status packet to the link after a request transfer which contains a read request, or when the phy has pertinent information to send to the link or transaction layers. The only defined condition when the phy automatically sends a register to the link is after self-ID, when it sends the physical-ID register which contains the new node address.

The definition of the bits in the status transfer are shown below.

20.0 STATUS REQUEST, LENGTH OF STREAM: 16 BITS

BIT(S)	NAME	DESCRIPTION
0	Arbitration reset gap	Indicates that the phy has detected that the bus has been idle for an arbitration reset gap time (this time is defined in the P1394 standard). This bit is used by the link in its busy/retry state machine.
1	Subaction gap	Indicates that the phy has detected that the bus has been idle for a subaction gap time (this time is defined in the P1394 standard). This bit is used by the link to detect the completion of an isochronous cycle.
2	Bus Reset	Indicates that the phy has entered the bus reset state.
3	State Time out or CPS	Indicates that the phy stayed in a particular state for too long a period, which is usually the effect of a loop in the cable topology, or that the cable power has dropped below the threshold for reliable operation.
4–7	Address	These bits hold the address of the phy register whose contents will be transferred to the link.
8–15	Data	The data that is to be sent to the link.

21.0 STATUS TRANSFER TIMING

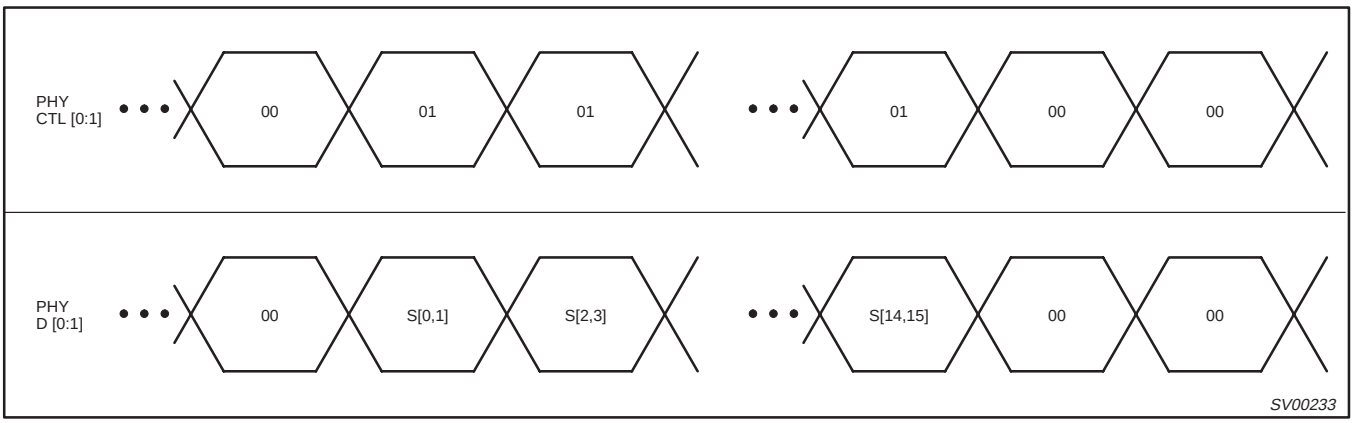


Figure 7. Status Transfer Timing

22.0 TRANSMIT

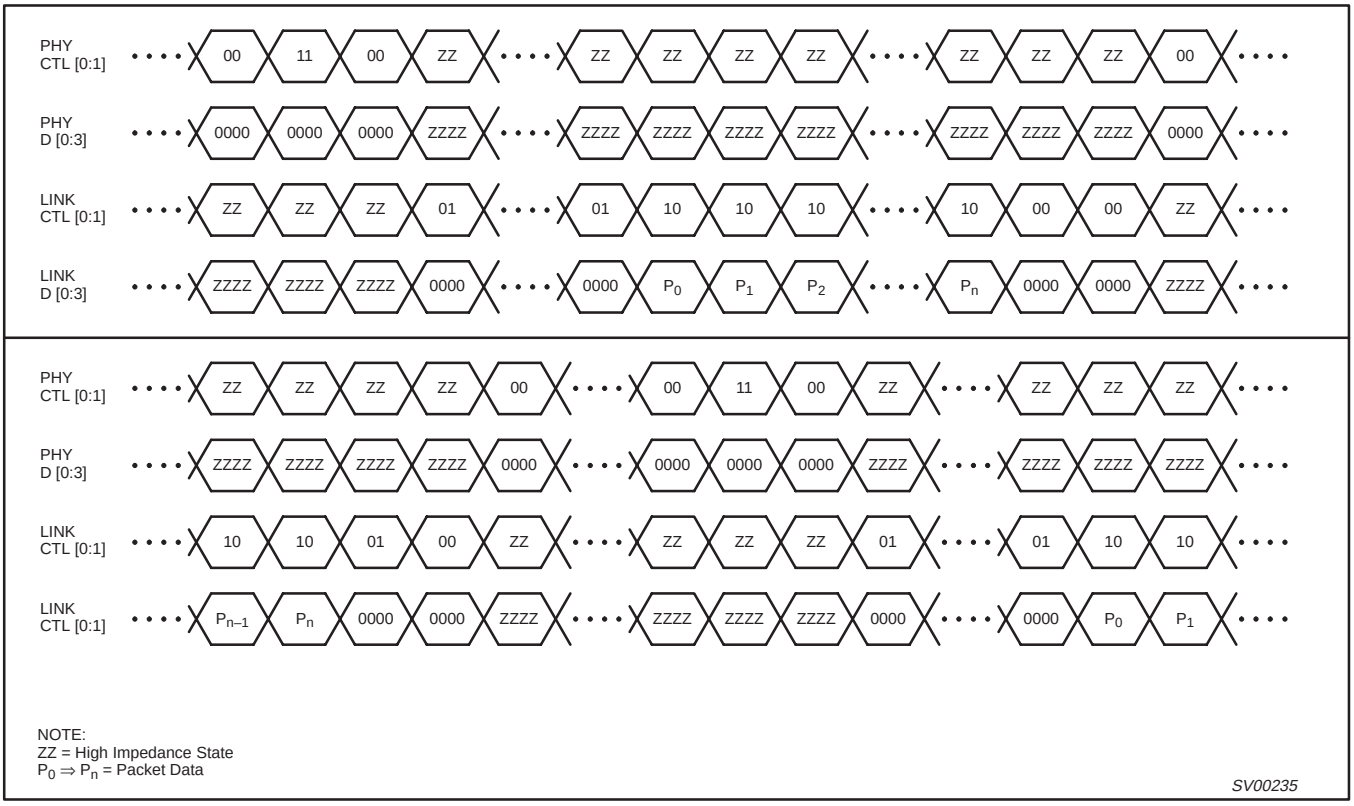
When the link wants to transmit information, it will first request access to the bus through the LREQ pin. Once the phy receives this request, it will arbitrate to gain control of the bus. When the phy wins ownership of the serial bus, it will grant the bus to the link by asserting the 'transmit' state on the CTL pins for at least one SYSCLK cycle, followed by idle for one clock cycle.

The link will take control of the bus by asserting either 'hold' or 'transmit' on the CTL lines. 'hold' is used by the link to keep control of the bus if it needs some time to prepare the data for transmission. The phy will keep control of the bus for the link by asserting a 'data-prefix' state on the bus. It is not necessary for the link to use 'hold' if it is ready to transmit as soon as bus ownership is granted.

When the link is prepared to send data, it will assert 'transmit' on the CTL lines as well as sending the first four bits of the packet on the D[0:3] lines (assuming 200 Mb/s). The 'transmit' state is held on the CTL pins until the last bits of data have been sent. The link will then assert 'Idle' on the CTL lines for one clock cycle after which it releases control of the interface.

However, there will be times when the link will need to send another packet without releasing the bus. For example, the link may want to send consecutive isochronous packets or it may want to attach a response to an acknowledgment. To do this, the link will assert 'hold' instead of 'Idle' when the first packet of data has been completely transmitted. 'Hold', in this case, informs the phy that the link needs to send another packet without releasing control of the bus. The phy will then wait a set amount of time before asserting 'transmit'. The link can then proceed with the transmittal of the second packet. After all data has been transmitted and the link has asserted 'Idle' on the CTL pins, the phy will assert its own 'Idle' state on the CTL lines. When sending multiple packets in this fashion, it is required that all data be transmitted at the same speed. This is required because the transmission speed is set during arbitration and since the arbitration step will be skipped, there will be no way of informing the network of a change in speed.

22.1 TRANSMIT TIMING WAVEFORMS



NOTE:
ZZ = High Impedance State
P0 => Pn = Packet data

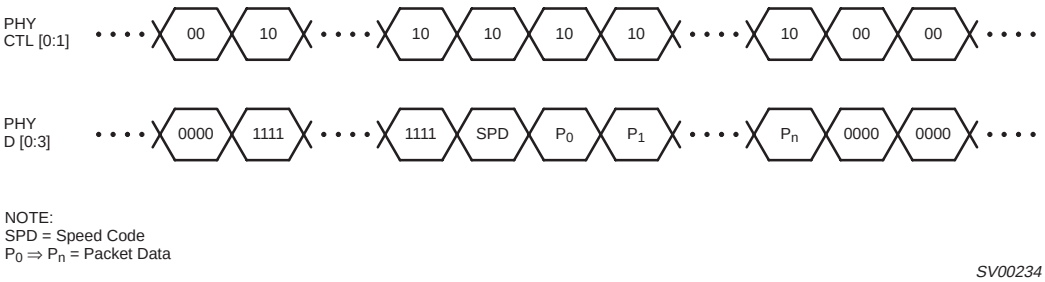
Figure 8. Transmit Timing Waveforms

23.0 RECEIVE

When data is received by the phy from the serial bus, it will transfer the data to the link for further processing. The phy will assert 'Receive' on the CTL lines and '1' on each D pin. The phy indicates the start of the packet by placing the speed code on the data bus. The phy will then proceed with the transmittal of the packet to the link on the D lines while still keeping the 'Receive' status on the CTL pins. Once the packet has been completely transferred, the phy will assert 'Idle' on the CTL pins which will complete the receive operation.

NOTE: The speed is a phy-link protocol and not included in the CRC.

23.1 RECEIVE TIMING WAVEFORMS



NOTE:
SPD = Speed Code
$P_0 \Rightarrow Pn$ = packet data

Figure 9. Receive Timing Waveforms

The speed code for the receiver is as follows:

D [0:3]	DATA RATE (Mbit/s)
00XX	100
0100	200

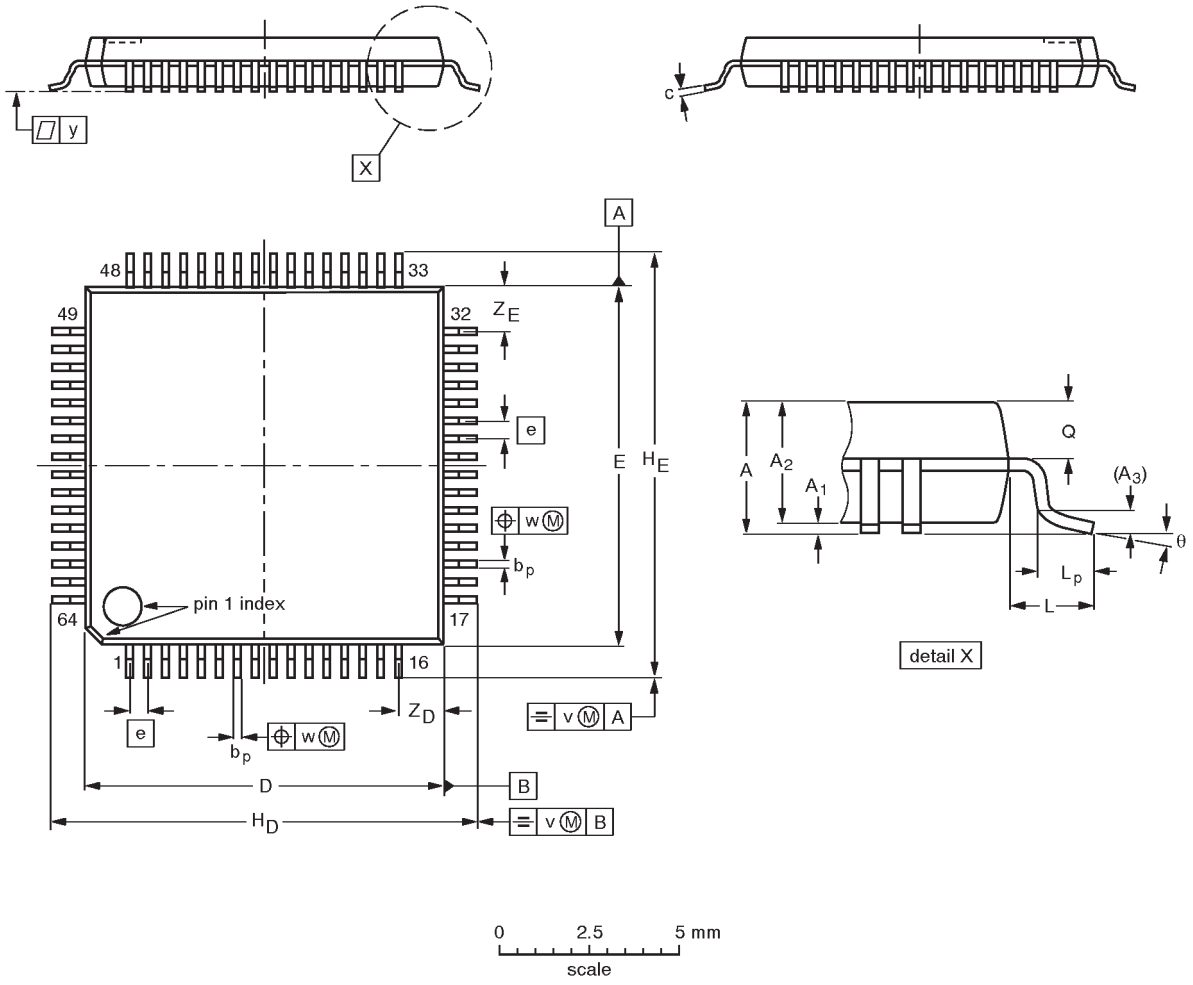
NOTE:
X transmitted as 0, ignored on receive.

24.0 POWER CLASS BITS IN SELF–ID PACKET

The settings of the PC[0:2] pins appear in the pwr field of the self–ID packet. Bit 21 is transmitted first, followed by bit 22 and then bit 23.

pwr[21:23]	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self powered, and provides a minimum of 15 W to the bus.
010	Node is self powered, and provides a minimum of 30 W to the bus.
011	Node is self powered, and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus, and is using up to 1 W.
101	Node may be powered from the bus, and is using up to 1 W. An additional 2 W is needed to enable the LLC and higher layers.
110	Node may be powered from the bus, and is using up to 1 W. An additional 5 W is needed to enable the LLC and higher layers.
111	Node may be powered from the bus, and is using up to 1 W. An additional 9 W is needed to enable the LLC and higher layers.

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-12-19

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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